

G12™-p bd4f5fs60ls33

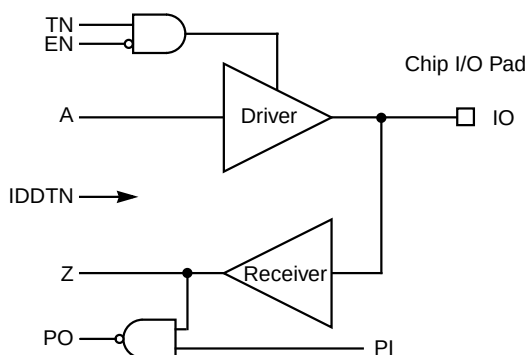
4 mA, 60 MHz, 5-Volt Tolerant, Fail-Safe I/O Buffer

Datasheet



The bd4f5fs60ls33 bidirectional buffer cell ([Figure 1](#)) provides up to 60 MHz off-chip input/output (I/O) signaling for application-specific integrated circuit (ASIC) chips implemented in the LSI Logic G12™-p 0.13 μm process technology. One application of the bd4f5fs60ls33 buffer is as a clock driver.

Figure 1 **bd4f5fs60ls33 Block Diagram**



Features and Benefits

- 60 MHz, 3.3 V I/O operation
- 5-Volt tolerant
- Fail-safe at high voltages
- Feedthrough protection
- 20 μA maximum leakage current
- Minimum 4 mA current drive into a 40 pF load at 60 MHz
- 1.8 V internal signaling for reduced power consumption
- Uses one standard I/O slot

General Description

The bd4f5fs60ls33 bidirectional I/O buffer contains a totem-pole type driver, a receiver, and test circuitry. Included level translation circuitry enables the driver to receive 1.8 V level signals from the ASIC circuitry

and produce 3.3 V level output at the I/O pad. Similarly, the receiver receives off-chip input at 3.3 volts and translates it to 1.8 volts for the internal ASIC application. Built-in NAND-tree logic gates and IDDTN control for IDDQ leakage testing enable use of the standard LSI Logic test methodology.

The buffer is 5-volt tolerant. Although the off-chip I/O signaling normally operates at 3.3 V, external circuitry may cause higher voltages, typically upwards of 5 V, to appear at the chip I/O pad. Circuit and process techniques ensure that such DC or transient voltages do not damage the buffer circuitry.

In the absence of a V_{DD} supply, the buffer is fail-safe and protected against voltage feedthrough. With high voltage applied to the chip I/O pad, the buffer can survive without degradation for up to ten years. Furthermore, with a low, maximum 20 μ A leakage current, the high voltage can not power up the ASIC through voltage feedthrough.

The following sections describe the bd4f5fs60ls33 buffer, which adheres to the general specifications in [Table 1](#).

Table 1 General Specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.97	3.3	3.63	V
T_j	Junction temperature		0	–	125	°C
ESD	Electrostatic discharge, human body model (HBM)	MIL-STD-883C, Method 3015.7 100 pF @1.5 K Ω	2000	–	–	V
	Electrostatic discharge, charged device model (CDM)	ESD DS5.3.1-1996	500	–	–	V

The final section, “[System Design Guidelines](#)”, provides layout guidelines to ensure good signal integrity for applications using the noise-sensitive, high-speed cells.

Signal Descriptions

[Table 2](#) describes the bd4f5fs60ls33 connections.

Table 2 **bd4f5fs60ls33 Connections**

Signal	Direction	Description
A	IN	Data input to driver from ASIC circuitry
EN	IN	0 = Normal mode 1 = Disable driver
IDDTN	IN	0 = Power down entire cell ¹ 1 = Normal mode
PI	IN	NAND-tree parametric test input
TN	IN	0 = Disable driver 1 = Normal mode
IO	IN/OUT	Input/output pad
PO	OUT	NAND-tree parametric test output
Z	OUT	Receiver buffer output to ASIC circuitry

1. Used for production IDDQ leakage test

Driver

The following sections describe the driver side of the I/O buffer.

Truth Table

[Table 3](#) describes the bd4f5fs60ls33 driver behavior.

Table 3 **Driver Truth Table**

IDDTN	A	TN	EN	IO
0 ¹	X ²	X	X	High Impedance
1	X	X	1	High Impedance
1	X	0	X	High Impedance
1	0	1	0	0
1	1	1	0	1

1. Factory IDDQ test setting
2. Don't care state, X = 0 or 1

Driver Specifications

DC Characteristics

Table 4 describes the bd4f5fs60ls33 driver DC characteristics.

Table 4 Driver DC Characteristics¹

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output, LOW	$I_{OL} = 4 \text{ mA}$	–	–	0.4	V
V_{OH}	Output, HIGH	$I_{OH} = -4 \text{ mA}$ $V_{DD} = 3.135 \text{ V}$	2.4	–	–	V
I_{OL}	Sink current	$V_{OL} = 0.4 \text{ V}$ maximum	4	–	–	mA
I_{OH}	Source current	$V_{OH} = 2.4 \text{ V}$ minimum	–	–	–4	mA
I_{OZ}	3-States leakage current	$0 \leq V_{PAD} \leq 5.5 \text{ V}$, $V_{DD} = 3.3 \text{ V} \pm 10\%$	–	–	20	μA
I_{LU}	Latchup current	$-2 \text{ V} < V_{PAD} < +8 \text{ V}$	–	–	± 100	mA

1. Values apply over all voltage, temperature, and process conditions.

Driver Slew Rate

In the rise/fall test, the driver drives a signal across a 40 pF load capacitor (Figure 2). Table 5 shows the observed slew rate across the load capacitor measured from 0.6 V to 2.2 V.

Figure 2 Rise/Fall Test Circuit

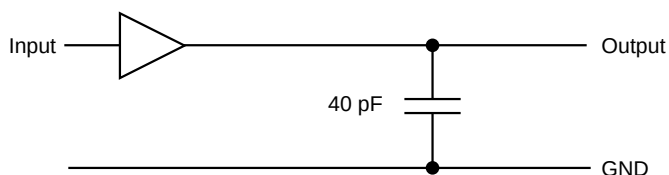


Table 5 Driver Rise/Fall Slew Rate

Min.	Typ.	Max.	Unit
500	880	1500	mV/ns

Receiver

The following sections describe the receiver side of the I/O buffer.

Truth Table

[Table 6](#) describes the bd4f5fs60ls33 receiver behavior.

Table 6 Receiver Truth Table

Inputs			Outputs	
IDDTN	IO	PI	Z	PO
0 ¹	High Impedance	1	1	0
1	0	0	0	1
1	1	0	1	1
1	1	1	1	0

1. Factory IDDQ test setting

Receiver Specifications

[Table 7](#) describes the bd4f5fs60ls33 receiver DC characteristics.

Table 7 Receiver DC Characteristics¹

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V _{IL}	Threshold, HIGH-to-LOW		1.0	–	1.50	V
V _{IH}	Threshold, LOW-to-HIGH		1.50	–	2.0	V
V _{TH} –V _{TL}	Hysteresis		320	–	–	mV
I _{LU}	Latch-up current	–2 V < V _{PAD} < +8 V	–	–	±100	mA

1. Values apply over all voltage, temperature, and process conditions

System Design Guidelines

To ensure good system-level operation, LSI Logic provides the following guidelines for placing the bd4f5fs60ls33 in the ASIC and for supplying power.

Placement

The bd4f5fs60ls33 cell requires placement on the I/O ring ([Table 8](#)) using one I/O slot.

Table 8 bd4f5fs60ls33 Dimensions on the I/O Ring

Width Along the I/O Ring	Length into the Chip
45.36 μm	371.01 μm

For correct placement of the bd4f5fs60ls33 cell, adhere to the following guidelines:

- A bd4f5fs60ls33 cell may adjoin another bd4f5fs60ls33 cell or a d4f5fsls33, bd4puf5fsls33, or bd4puodf5fsls33 cell.
- Separate the bd4f5fs60ls33 cell from any other type of I/O function by at least one I/O slot to avoid N-channel to P-channel design rule violations. If possible, use a VDD or VSS pad for the separation.
- Because its length exceeds the length of other standard I/O functions, the bd4f5fs60ls33 cell may not use a corner I/O slot.

Power

For best system-level performance, adhere to the following power guidelines:

- Use one power/ground pad pair for every four I/O cells.
- Place an I/O cell no more than four slots away from a power pad and no more than four slots away from a ground pad.

Notes

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