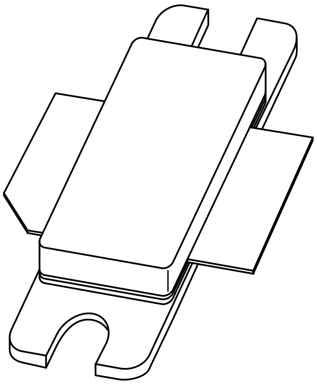
DATA SHEET



BLA1011-200
Avionics LDMOS transistor

Product specification
Supersedes data of 2001 May 15

2002 Mar 18

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

APPLICATIONS

- Avionics transmitter applications in the 1030 to 1090 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead SOT502A flange package with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

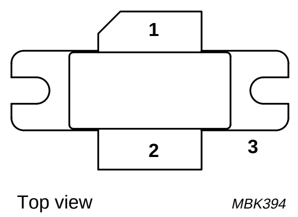


Fig.1 Simplified outline SOT502A.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
Pulsed class-AB; t_p = 50 μs; δ = 2 %	1030 to 1090	36	200	>13; typ. 15	>45; typ. 50	<50; typ. 35	<50; typ. 6

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±22	V
P_{tot}	total power dissipation	$T_h \leq 25$ °C; t_p = 50 μs; δ = 2 %	–	700	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$Z_{th\ j\text{-}h}$	thermal impedance from junction to heatsink	T_h = 25 °C; note 1	0.15	K/W

Note

1. Thermal resistance is determined under RF operating conditions; t_p = 50 μs, δ = 10 %.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 36 V	–	–	1	μA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	45	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	–	9	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	–	60	–	mΩ

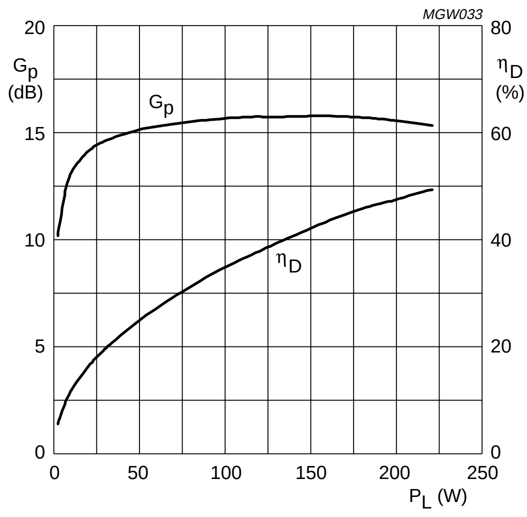
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $Z_{th\ mb\text{-}h}$ = 0.15 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
Pulsed class-AB; t_p = 50 μs; δ = 2 %	1030 to 1090	36	200	>13; typ. 15	>45; typ. 50	<50; typ. 35	<50; typ. 6

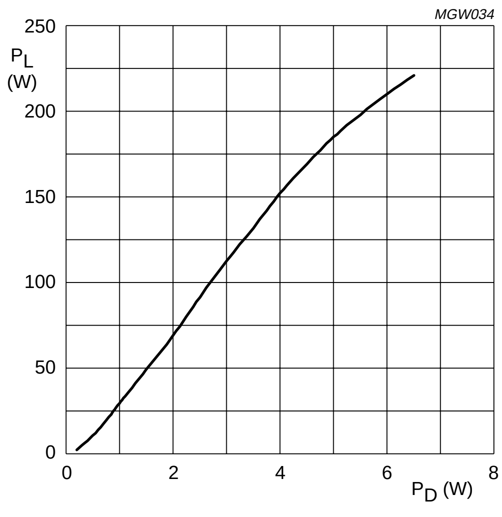
Ruggedness in class-AB operation

The BLA1011-200 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions: V_{DS} = 36 V; f = 1030 to 1090 MHz at rated load power.



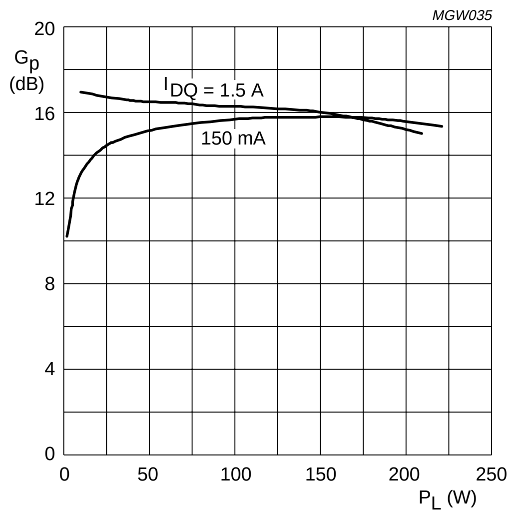
V_{DS} = 36 V; I_{DQ} = 150 mA; f = 1060 MHz;
t_p = 50 µs; δ = 2 %.

Fig.2 Power gain and efficiency as functions of load power; typical values.



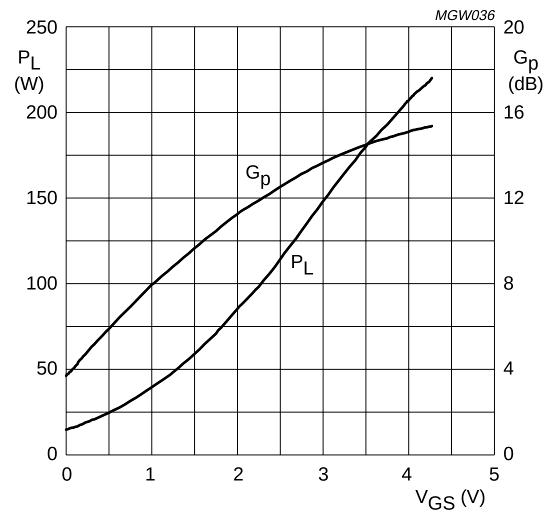
V_{DS} = 36 V; I_{DQ} = 150 mA; f = 1060 MHz;
t_p = 50 µs; δ = 2 %.

Fig.3 Load power as a function of drive power; typical values.



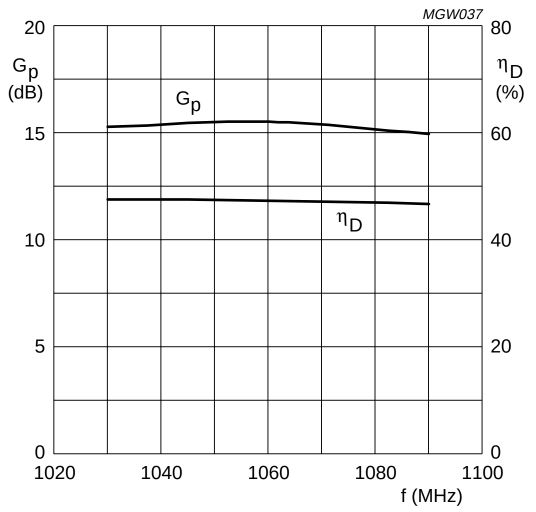
V_{DS} = 36 V; f = 1060 MHz; t_p = 50 µs; δ = 2 %.

Fig.4 Power gain as a function of load power; typical values.



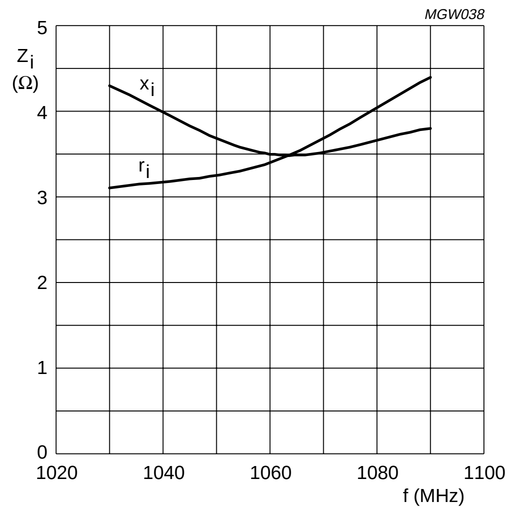
V_{DS} = 36 V; I_{DQ} = 150 mA; P_D = 5.5 W;
f = 1060 MHz; t_p = 50 µs; δ = 2 %.

Fig.5 Load power and power gain as functions of gate-source voltage; typical values.



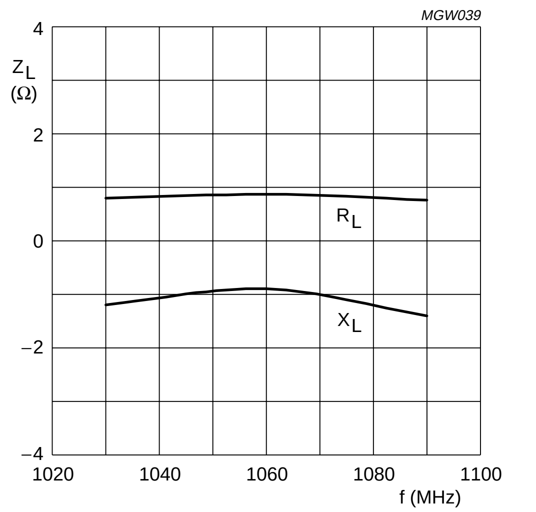
V_{DS} = 36 V; I_{DQ} = 150 mA; P_L = 200 W;
t_p = 50 µs; δ = 2 %.

Fig.6 Power gain and efficiency as functions of frequency; typical values.



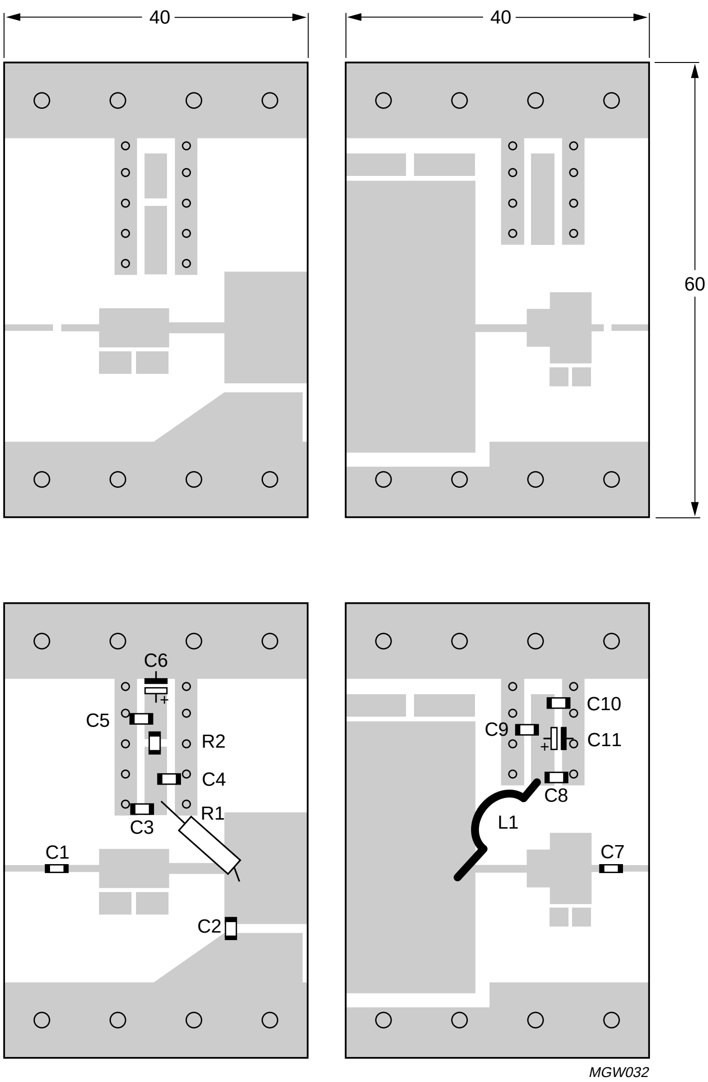
V_{DS} = 36 V; I_{DQ} = 150 mA; P_L = 200 W;
t_p = 50 µs; δ = 2 %.

Fig.7 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 36 V; I_{DQ} = 150 mA; P_L = 200 W;
t_p = 50 µs; δ = 2 %.

Fig.8 Load impedance as a function of frequency (series components); typical values.



Dimensions in mm.

The components are situated on one side of the copper-clad Duroid printed-circuit board with ε_r = 6.2 and thickness 0.64 mm.
The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 1030 to 1090 MHz test circuit.

List of components (see Fig.9)

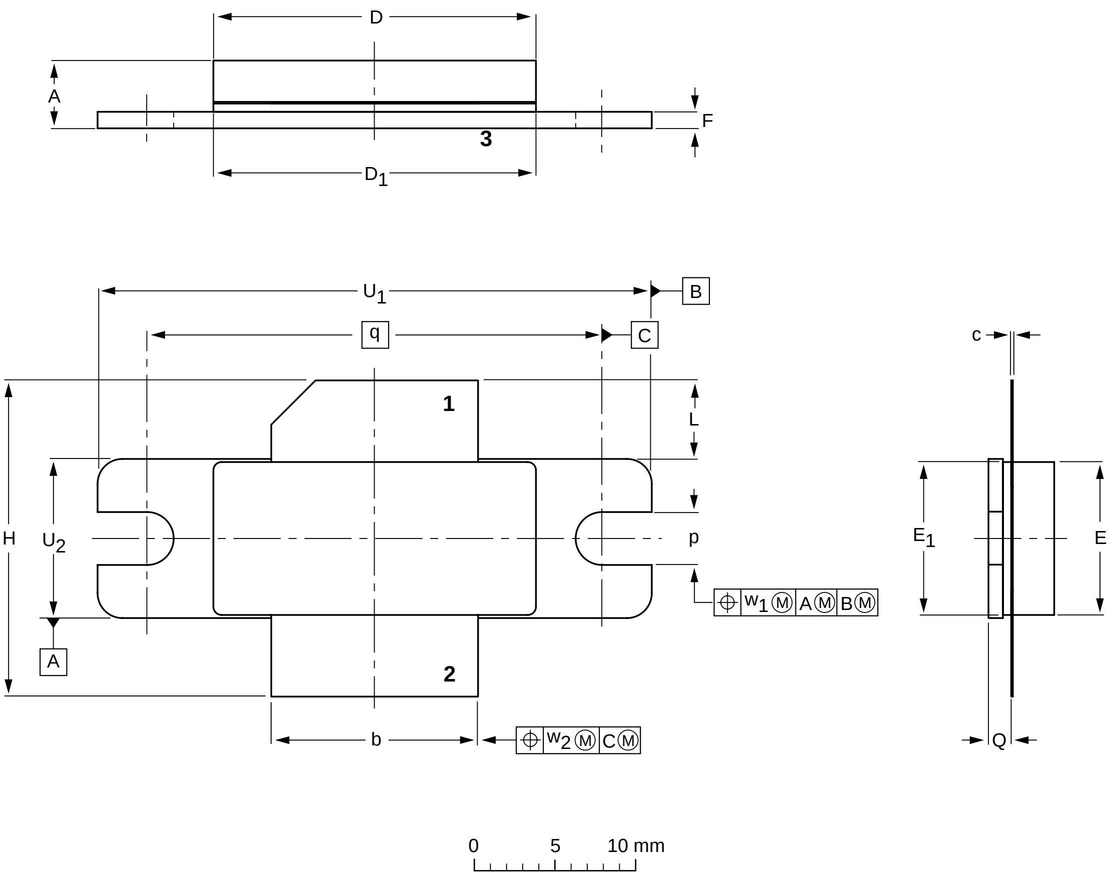
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor; note 1	39 pF	
C2	multilayer ceramic chip capacitor; note 2	4.3 pF	
C3	multilayer ceramic chip capacitor; note 1	11 pF	
C4, C7	multilayer ceramic chip capacitor; note 1	62 pF	
C5	multilayer ceramic chip capacitor; note 1	100 pF	
C6	electrolytic capacitor	47 μF; 20 V	
C8	multilayer ceramic chip capacitor; note 2	20 pF	
C9	multilayer ceramic chip capacitor; note 1	47 pF	
C10	multilayer ceramic chip capacitor; note 3	1.2 nF	
C11	electrolytic capacitor	47 μF; 63 V	
L1	Ω-shaped enamelled 1 mm copper wire		length = 38 mm
R1	metal film resistor	301 Ω	
R2	SMD0508 resistor	18 Ω	

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. American Technical Ceramics type 700 or capacitor of same quality.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						~~99-10-13~~ 99-12-28

DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
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NOTES

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