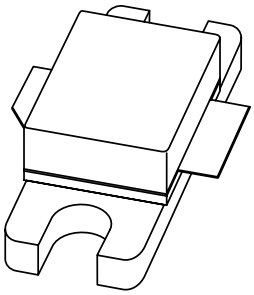
DATA SHEET



BLF2022-30
UHF power LDMOS transistor

Product specification
Supersedes data of 2002 Dec 19

2003 Feb 24

Philips
Semiconductors

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UHF power LDMOS transistor BLF2022-30

FEATURES

- Typical W-CDMA performance at a supply voltage of 28 V and I_{DQ} of 240 mA:
  - Output power = 3.5 W (AV)
  - Gain = 12.9 dB
  - Efficiency = 16.5%
  - ACPR = –45 dBc at 3.84 MHz
  - d_{im} = –42 dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (2000 to 2200 MHz)
- Internally matched for ease of use.

APPLICATIONS

- RF power amplifiers for W-CDMA base stations and multicarrier applications in the 2000 to 2200 MHz frequency range.

DESCRIPTION

30 W LDMOS power transistor for base station applications at frequencies from 2000 to 2200 MHz.

PINNING - SOT608A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

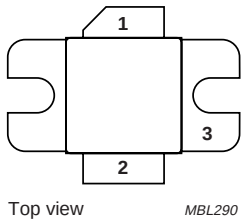


Fig.1 Simplified outline (SOT608A).

QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)	$ACLR_5$ (dBc)
2-tone, class-AB	f_1 = 2170; f_2 = 2170.1	28	240	30 (PEP)	12.6	34.3	–29.5	–
two-carrier W-CDMA test model 1, 64 channels	f_1 = 2155; f_2 = 2165	28	270	3.5 (AV)	12.9	16.5	–42	–45

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	DC drain current	–	4.5	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C; note 1	1.85	K/W

Notes

1. Thermal resistance is determined under specified RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.7 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 70 mA	4.5	–	5.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	μA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	9	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	11	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.5 A	–	2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 2.5 A	–	0.3	–	Ω
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	1.7	–	pF

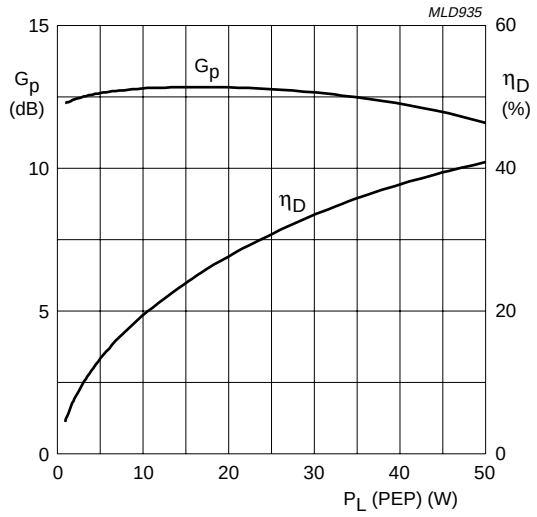
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}c}$ = 1.85 K/W; unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2170; f_2 = 2170.1	28	240	30 (PEP)	>11	>30	≤–25

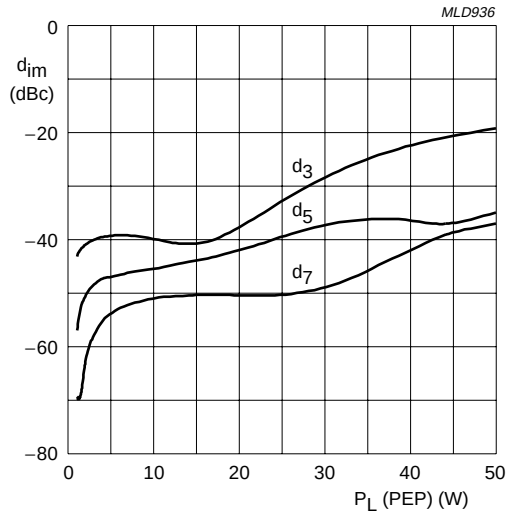
Ruggedness in class-AB operation

The BLF2022-30 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{DQ} = 240 mA; P_L = 30 W; f = 2170 MHz.



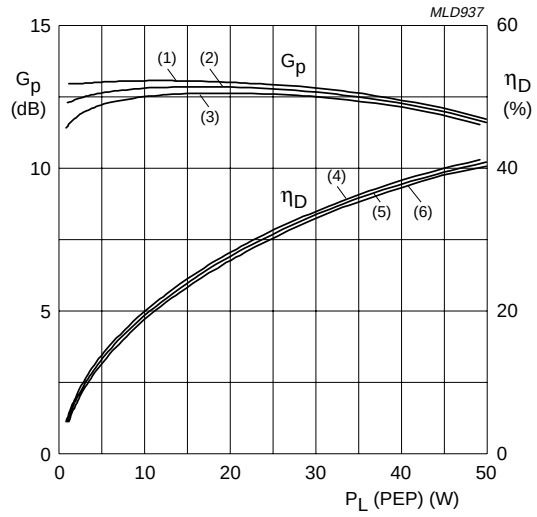
V_{DS} = 28 V; I_{DQ} = 240 mA; $T_h \leq 25$ °C;
f_1 = 2170 MHz; f_2 = 2170.1 MHz.

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



V_{DS} = 28 V; I_{DQ} = 240 mA; $T_h \leq 25$ °C;
f_1 = 2170 MHz; f_2 = 2170.1 MHz.

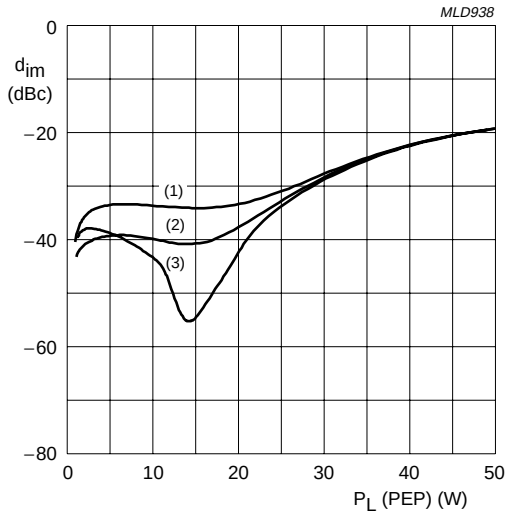
Fig.3 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 28 V; $T_h \leq 25$ °C;
f_1 = 2170 MHz; f_2 = 2170.1 MHz.

(1) I_{DQ} = 290 mA. (3) I_{DQ} = 190 mA. (5) I_{DQ} = 240 mA.
(2) I_{DQ} = 240 mA. (4) I_{DQ} = 190 mA. (6) I_{DQ} = 290 mA.

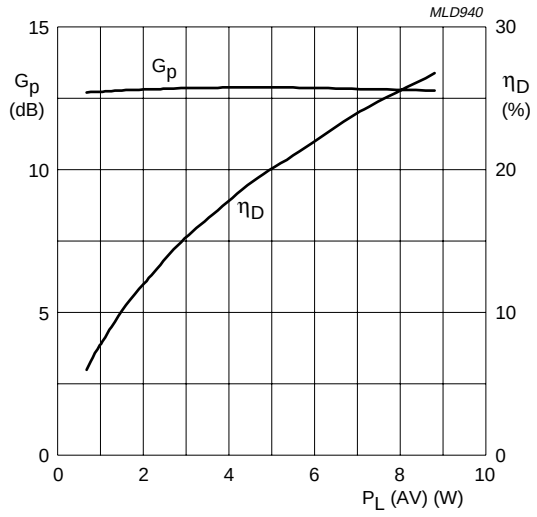
Fig.4 Power gain and drain efficiency as functions of peak envelope load power; typical values.



V_{DS} = 28 V; $T_h \leq 25$ °C;
f_1 = 2170 MHz; f_2 = 2170.1 MHz.

(1) I_{DQ} = 190 mA. (2) I_{DQ} = 240 mA. (3) I_{DQ} = 290 mA.

Fig.5 Third order intermodulation distortion as a function of peak envelope load power; typical values.

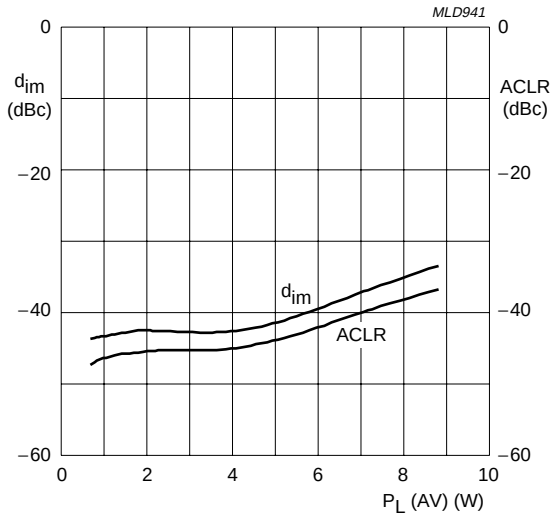


Two-carrier W-CDMA performance.

V_{DS} = 28 V; I_{DQ} = 270 mA; $T_h \leq 25$ °C; f_1 = 2170 MHz.

Input signal: 3GPP W-CDMA 64 channels with 66% clipping; peak to average power ratio: 8.5 dB at 0.01% probability on CCDF; channel spacing/bandwidth = 5 MHz / 3.84 MHz.

Fig.6 Power gain and drain efficiency as functions of average load power; typical values.

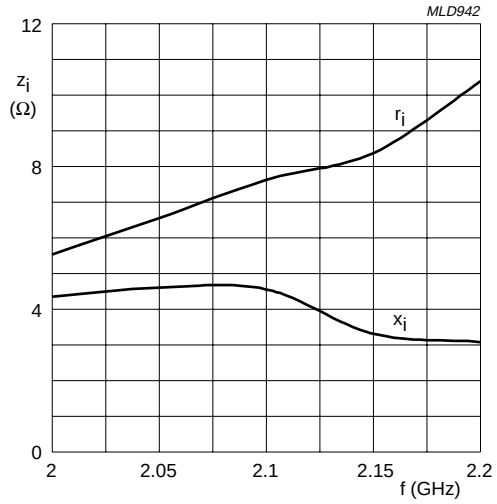


Two-carrier W-CDMA performance.

V_{DS} = 28 V; I_{DQ} = 270 mA; $T_h \leq 25$ °C; f_1 = 2155 MHz; f_1 = 2165 MHz;.

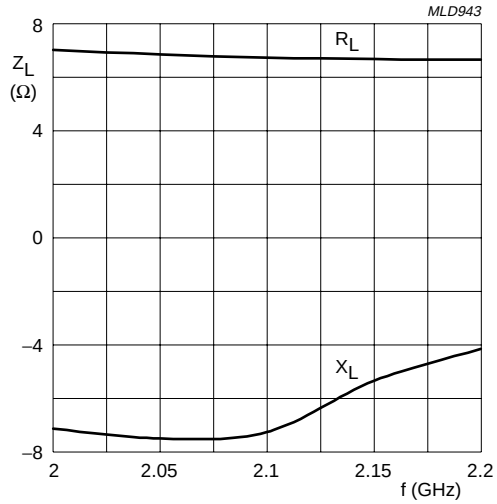
Input signal: 3GPP W-CDMA 64 channels with 66% clipping; peak to average power ratio: 8.5 dB at 0.01% probability on CCDF; channel spacing/bandwidth = 5 MHz / 3.84 MHz.

Fig.7 Intermodulation distortion and adjacent channel leakage ratio (ACLR) as functions of average load power; typical values.



V_{DS} = 28 V; I_D = 240 mA; P_L = 30 W; $T_h \leq 25$ °C.

Fig.8 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 28 V; I_D = 240 mA; P_L = 30 W; $T_h \leq 25$ °C.

Fig.9 Load impedance as a function of frequency (series components); typical values.

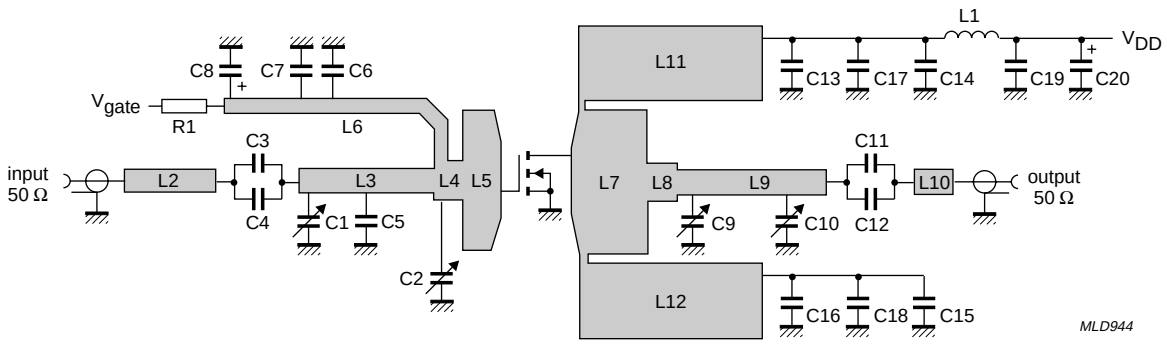


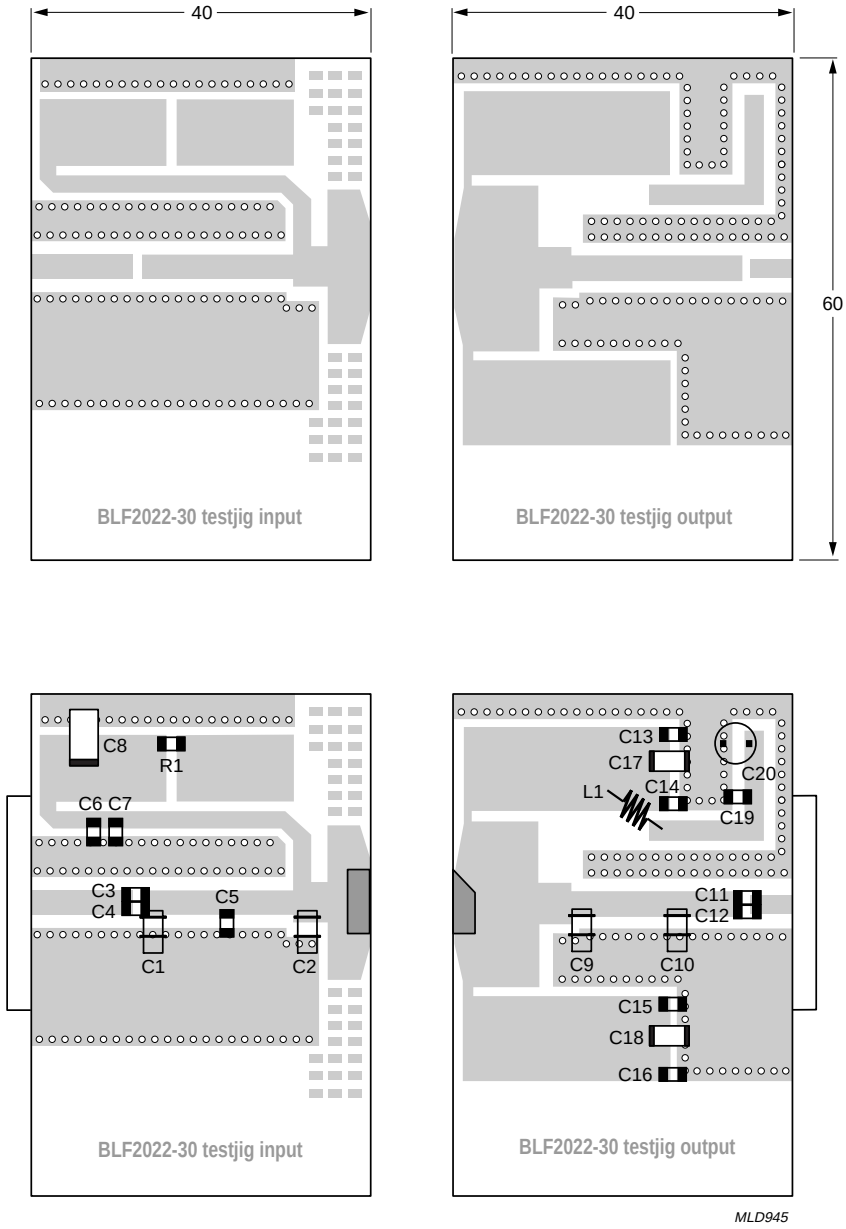
Fig.10 Class-AB test circuit.

List of components (See Figs 10 and 11)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C9, C10	Tekelec variable capacitor	0.6 to 4.5 pF		
C3, C4, C11, C12	multilayer ceramic chip capacitor; note 1	6.8 pF		
C5	multilayer ceramic chip capacitor; note 1	2.2 pF		
C6, C7, C13, C14, C15, C16	multilayer ceramic chip capacitor; note 1	12 pF		
C8	tantalum capacitor	10 μF		
C17, C18	multilayer ceramic chip capacitor	4.7 μF		TDK C4532X7R1H475M
C19	multilayer ceramic chip capacitor; note 2	1 nF		
C20	electrolytic capacitor	100 μF; 63 V		
L1	handmade		2 loops, dia. 4 mm	
L2	stripline; note 3	50 Ω	12 × 2.4 mm	
L3	stripline; note 3	43 Ω	18 × 3 mm	
L4	stripline; note 3	29 Ω	4 × 5 mm	
L5	stripline; note 3	10 Ω	5 × 18.4 mm	
L6	stripline; note 3	56 Ω	34.4 × 2 mm	
L7	stripline; note 3	9 Ω	10 × 20 mm	
L8	stripline; note 3	29 Ω	4 × 5 mm	
L9	stripline; note 3	41 Ω	20 × 3.2 mm	
L10	stripline; note 3	50 Ω	5 × 2.4 mm	
L11, L12	stripline; note 3	17 Ω	24.5 × 10 mm	

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2); thickness 0.79 mm.



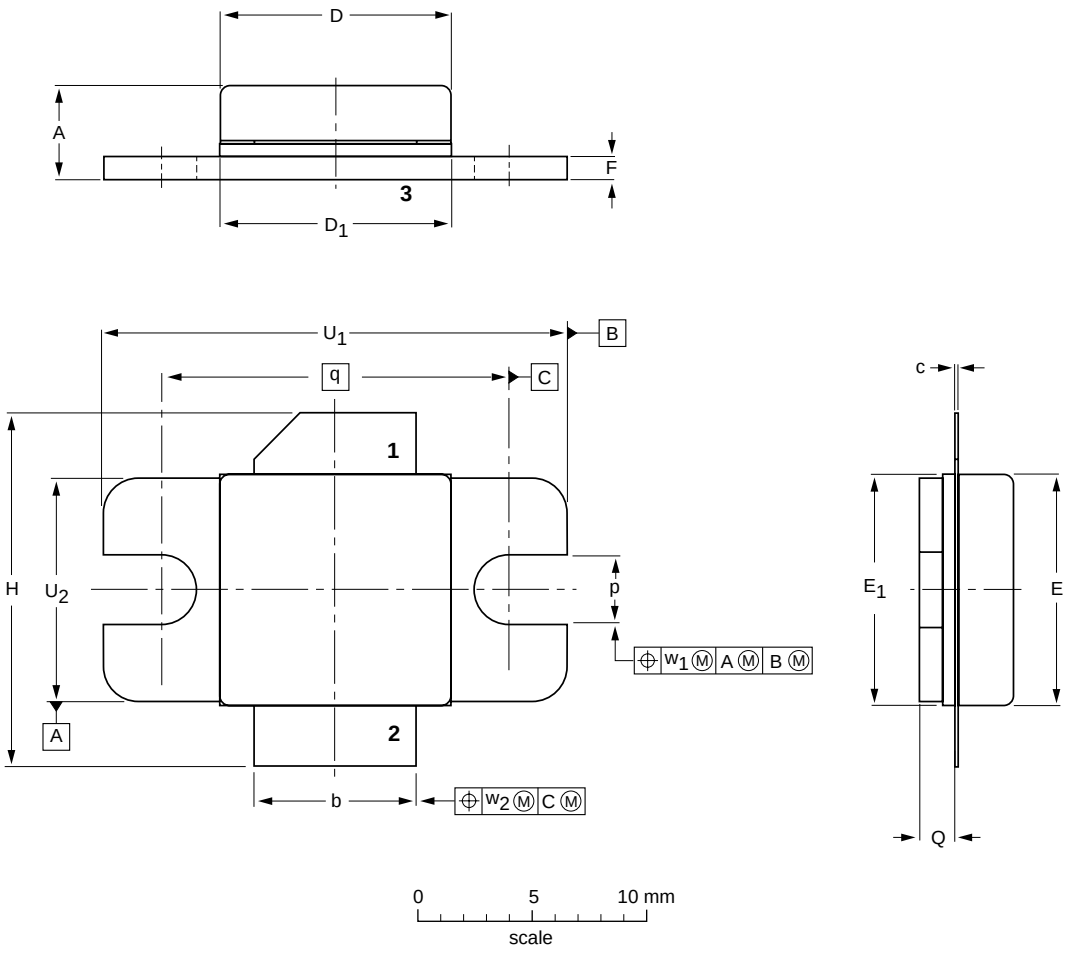
Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.11 Component layout for 2.17 GHz class-AB test circuit.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 2 leads **SOT608A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.62 3.76	7.24 6.99	0.15 0.10	10.21 10.01	10.29 10.03	10.21 10.01	10.29 10.03	1.14 0.89	15.75 14.73	3.30 2.92	1.70 1.35	15.24	20.45 20.19	9.91 9.65	0.25	0.51
inches	0.182 0.148	0.285 0.275	0.006 0.004	0.402 0.394	0.405 0.395	0.402 0.394	0.405 0.395	0.045 0.035	0.620 0.580	0.130 0.115	0.067 0.053	0.600	0.805 0.795	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT608A						~~01-02-22~~ 02-02-11

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LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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