DATA SHEET

BLF147
VHF power MOS transistor

Product specification
Supersedes data of September 1992

2001 May 23

Philips
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VHF power MOS transistor | BLF147

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to 'General' section for further information.

PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

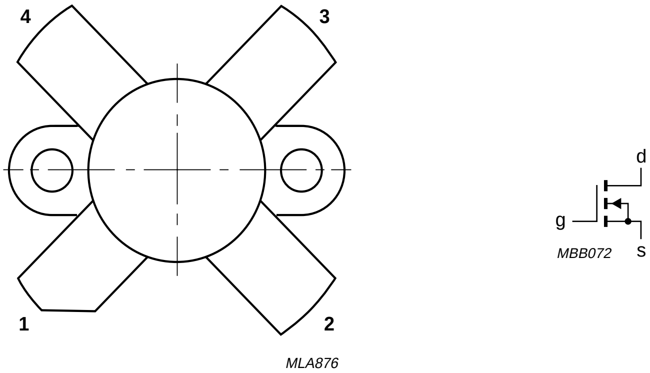


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB, class-AB	28	28	150 (PEP)	> 17	> 35	< –30	< –30
CW, class-B	108	28	150	typ. 14	typ. 70	–	–

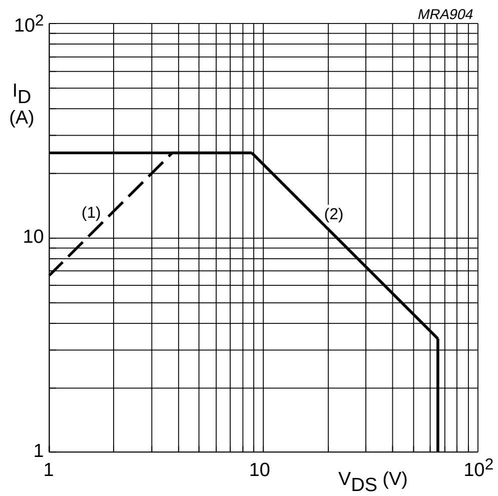
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

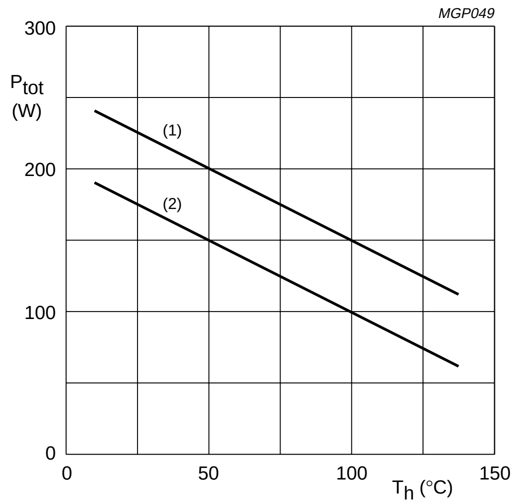
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



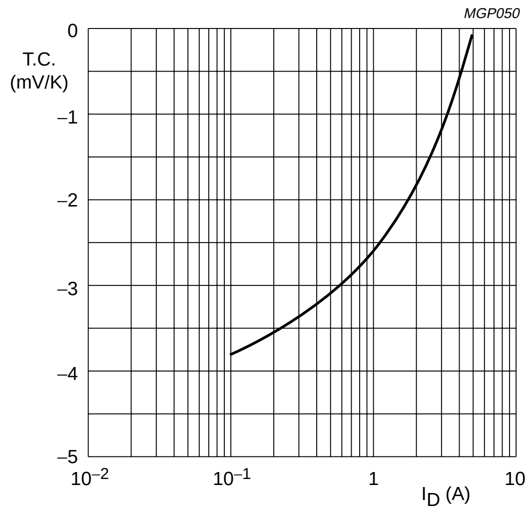
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

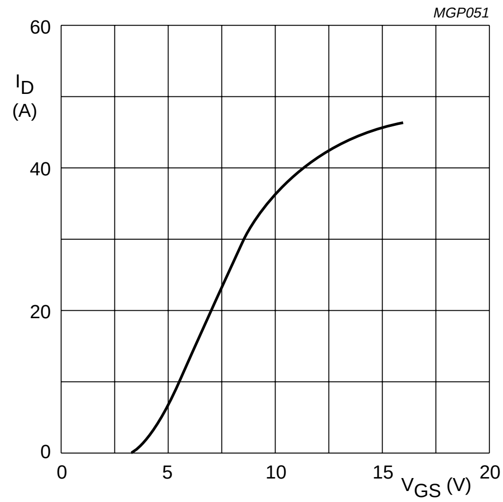
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 100 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 200 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	450	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	360	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	55	–	pF



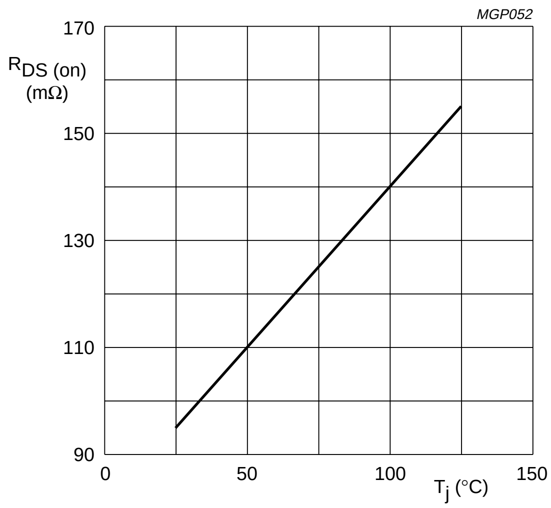
V_{DS} = 28 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



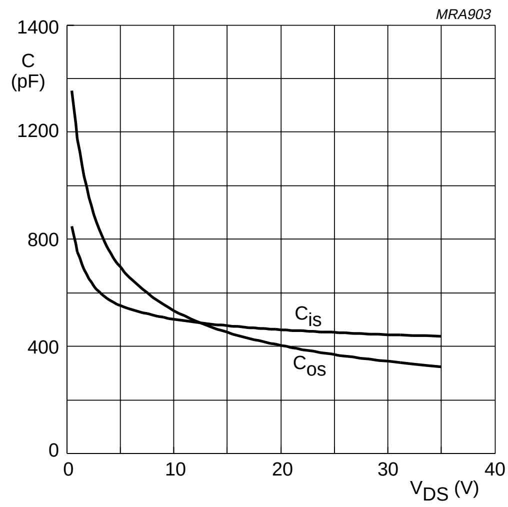
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



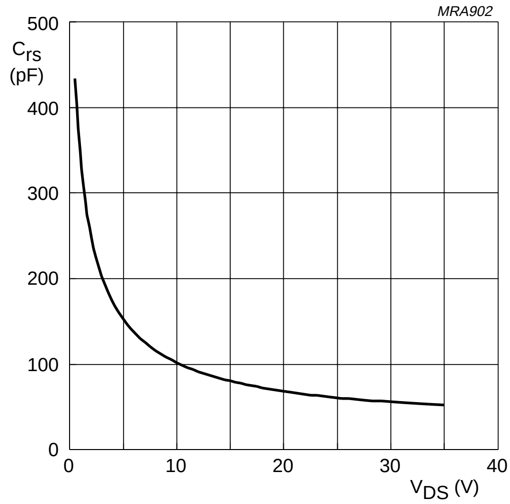
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; R_{GS} = 9.8 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (A)	G_p (dB)	η_D (%)	d_3 (dB) (note 2)	d_5 (dB) (note 2)
20 to 150 (PEP)	28	28	1	> 17 typ. 19	> 35 typ. 40	< –30 typ. –34	< –30 typ. –40

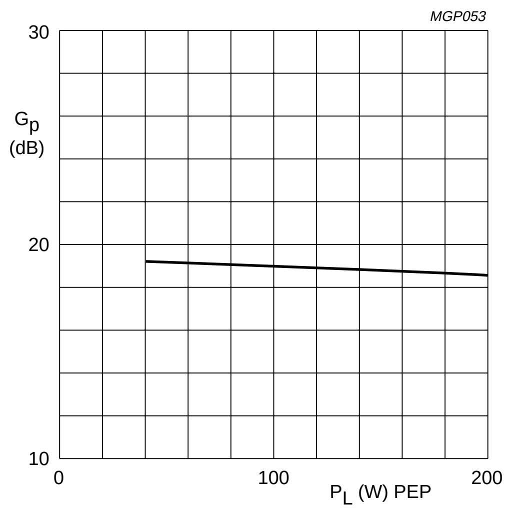
Notes

1. Optimum load impedance: 2.1 + j0 Ω.
2. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

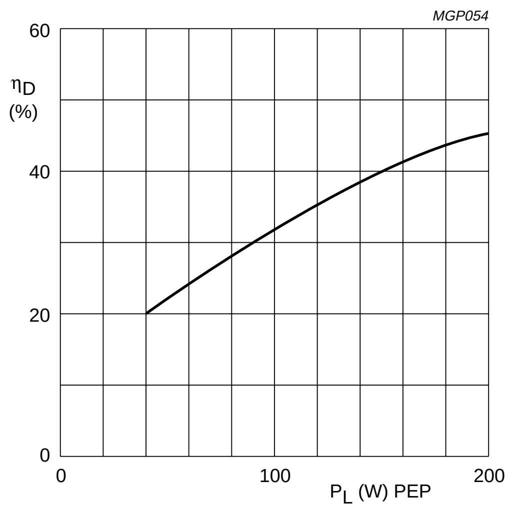
The BLF147 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 28 MHz at rated load power.



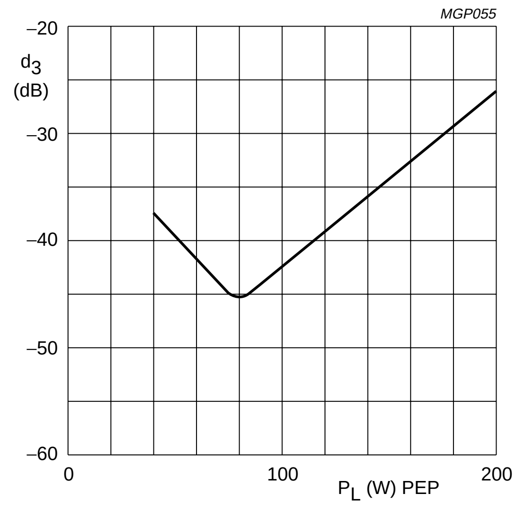
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Gain as a function of load power, typical values.



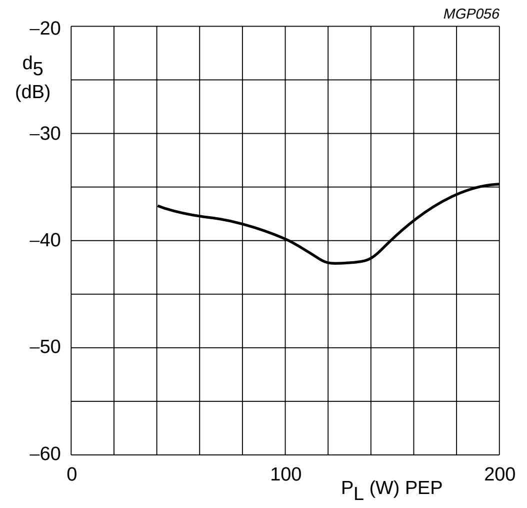
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Efficiency as a function of load power, typical values.



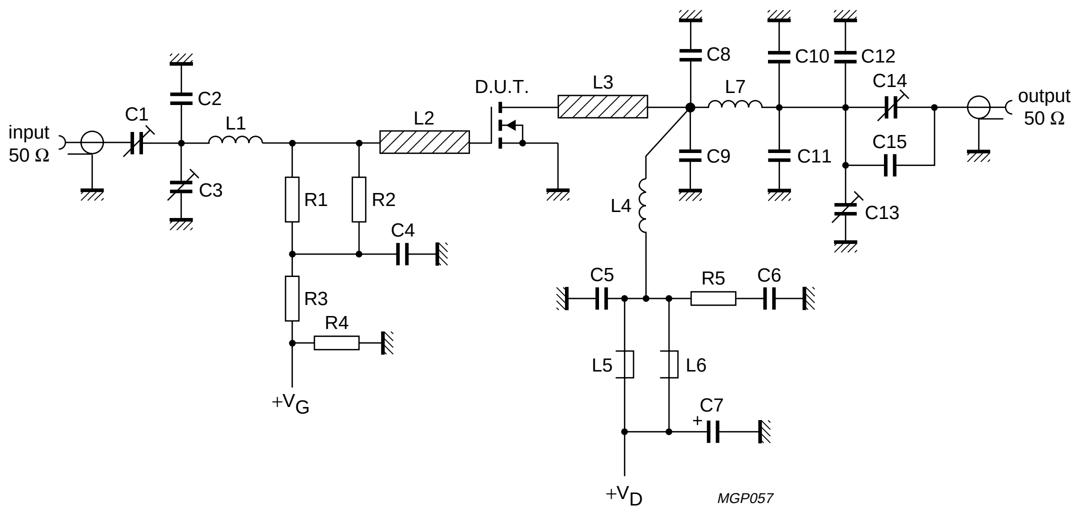
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

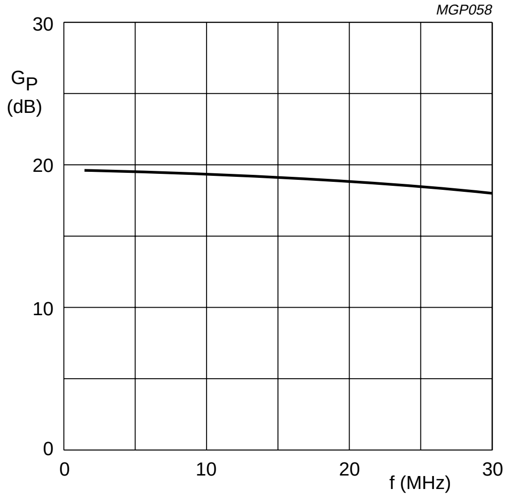
Fig.13 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C8, C9	multilayer ceramic chip capacitor (note 1)	75 pF		
C4, C5	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C6	multilayer ceramic chip capacitors in parallel	3 × 100 nF		2222 852 47104
C7	electrolytic capacitor	2.2 μF, 63 V		
C10	multilayer ceramic chip capacitor (note 1)	100 pF		
C11, C12	multilayer ceramic chip capacitor (note 1)	150 nF		
C15	multilayer ceramic chip capacitor (note 1)	240 pF		
L1	6 turns enamelled 0.7 mm copper wire	145 nH	length 5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 × 6 mm	
L4	4 turns enamelled 1.5 mm copper wire	148 nH	length 8 mm; int. dia. 10 mm; leads 2 × 5 mm	
L5, L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	3 turns enamelled 2.2 mm copper wire	79 nH	length 8 mm; int. dia. 8 mm; leads 2 × 5 mm	
R1, R2	1 W metal film resistor	19.6 Ω		2322 153 51969
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	1 MΩ		2322 151 71005
R5	1 W metal film resistor	10 Ω		2322 153 51009

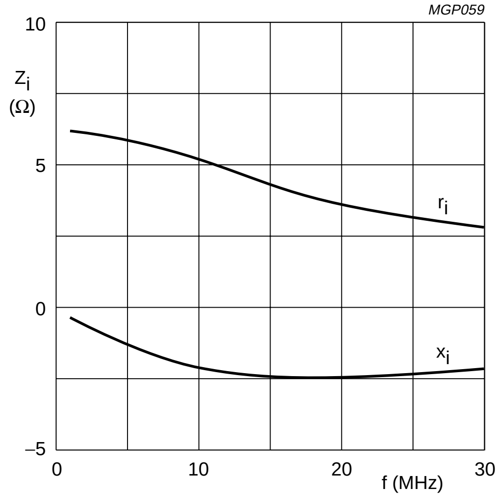
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.



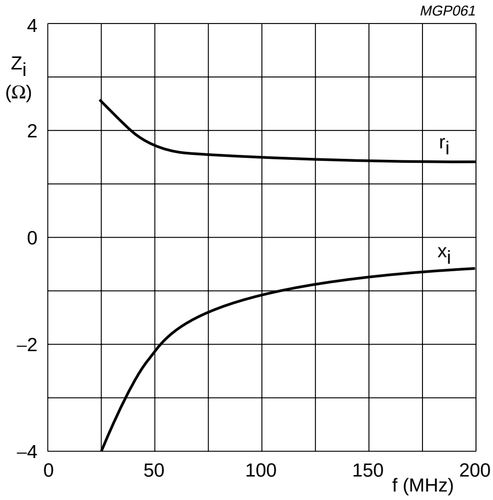
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 6.25 Ω; P_L = 150 W (PEP); R_L = 2.1 Ω.

Fig.14 Gain as a function of frequency, typical values.



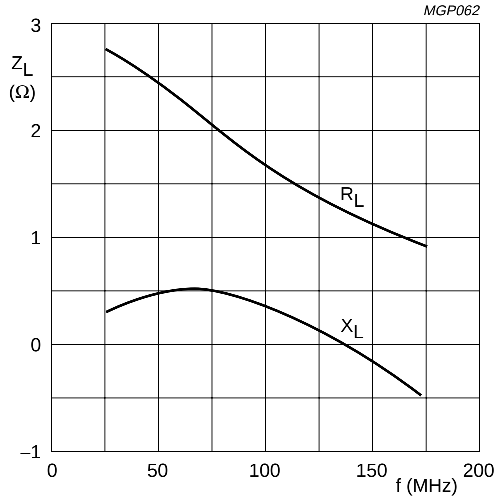
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 6.25 Ω; P_L = 150 W (PEP); R_L = 2.1 Ω.

Fig.15 Input impedance as a function of frequency (series components), typical values.



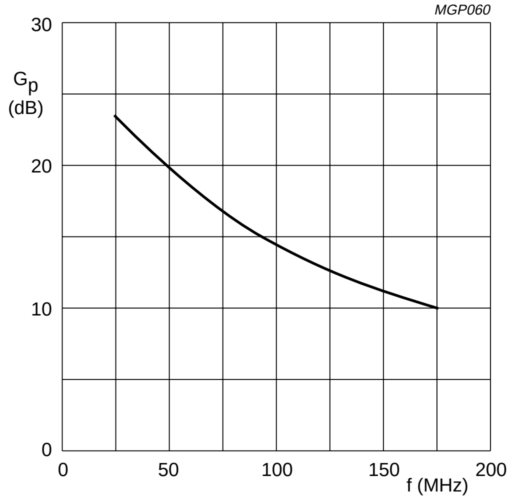
Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.16 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.17 Load impedance as a function of frequency (series components), typical values.

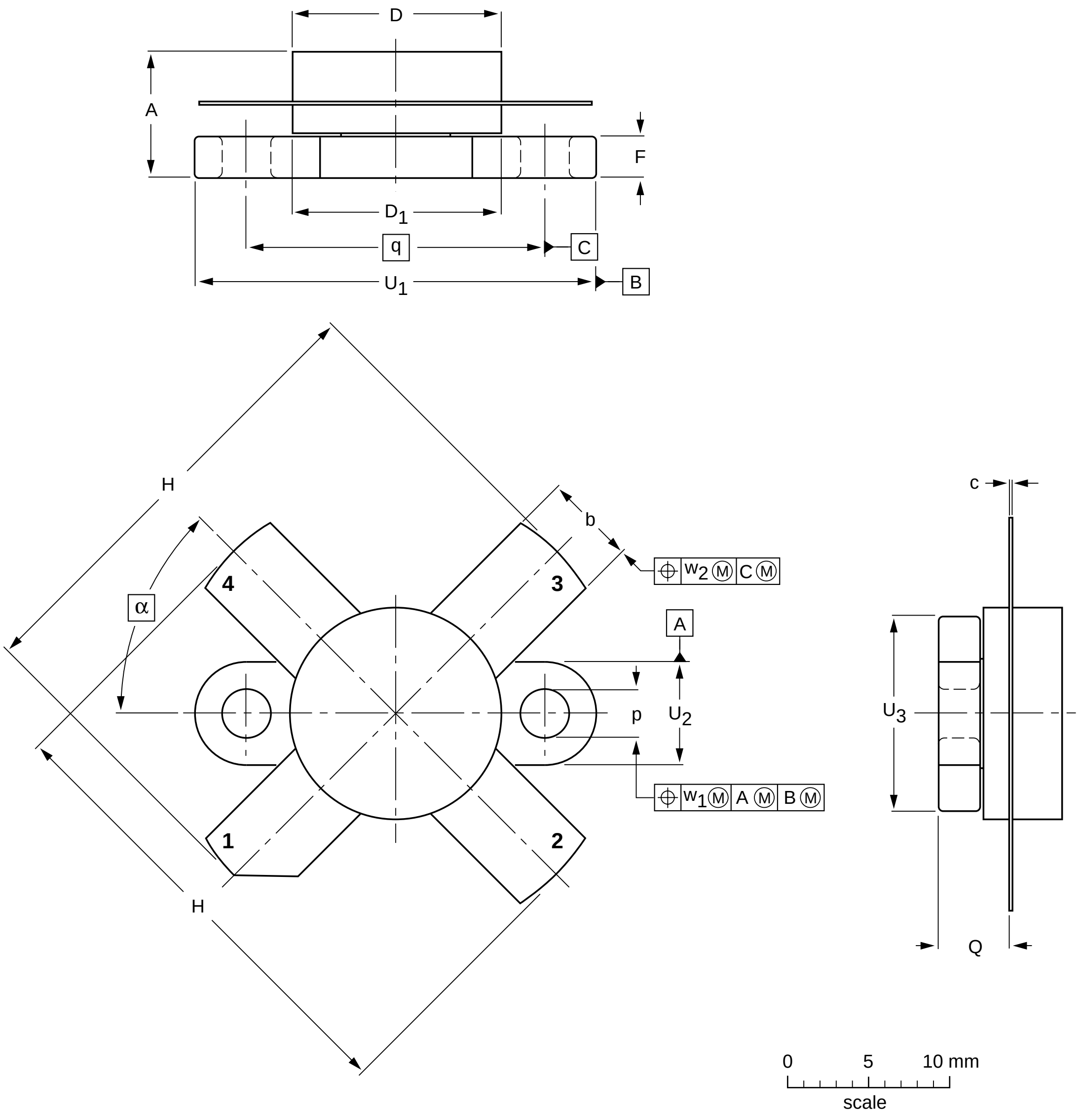


Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.18 Power gain as a function of frequency, typical values.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads **SOT121B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.25	0.51	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.01	0.02	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT121B						99-03-29

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