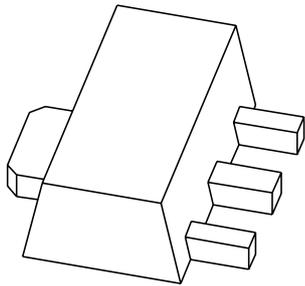


# DATA SHEET



## **BSS192**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
Supersedes data of 1997 Jun 20

2002 May 22

## P-channel enhancement mode vertical D-MOS transistor

# BSS192

### FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

### APPLICATIONS

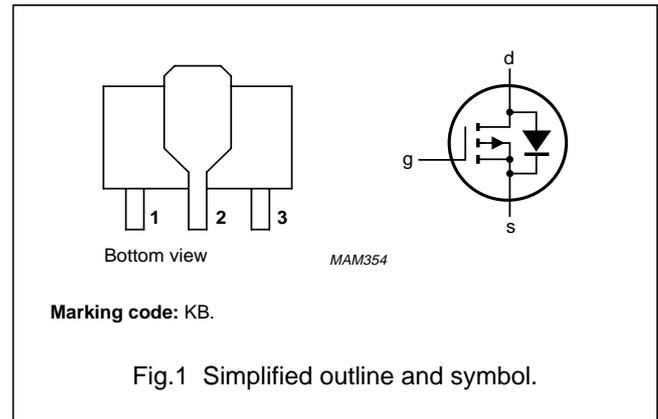
- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers.

### DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

### PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		-240	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -1 \text{ mA}$ ; $V_{GS} = V_{DS}$	-2.8	V
$I_D$	drain current (DC)		-200	mA
$R_{DSon}$	drain-source on-state resistance	$I_D = -200 \text{ mA}$ ; $V_{GS} = -10 \text{ V}$	12	$\Omega$

## P-channel enhancement mode vertical D-MOS transistor

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	–240	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$I_D$	drain current (DC)		–	–200	mA
$I_{DM}$	peak drain current		–	–600	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C

### Note

1. Device mounted on a ceramic substrate; area 2.5 cm<sup>2</sup>; thickness 0.7 mm.

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	125	K/W

### Note

1. Device mounted on a ceramic substrate; area 2.5 cm<sup>2</sup>; thickness 0.7 mm.

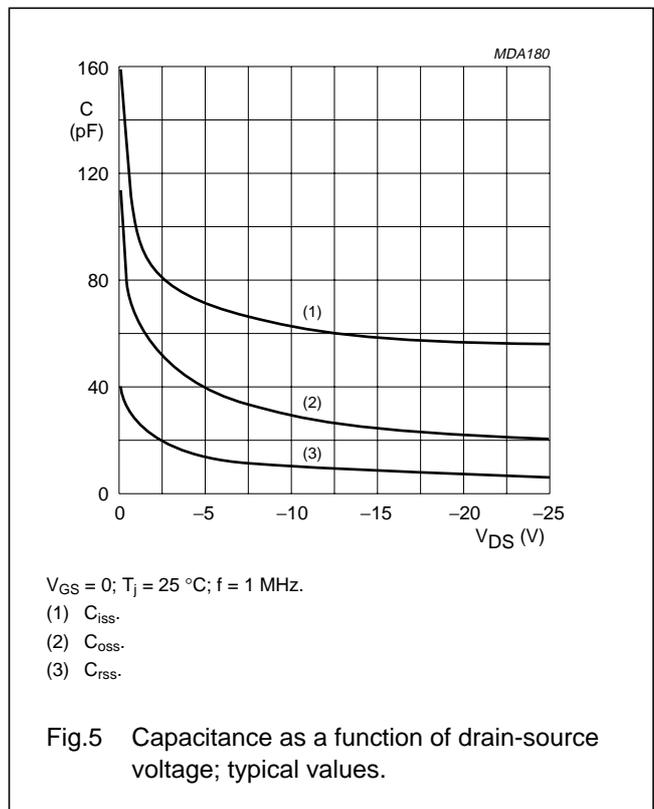
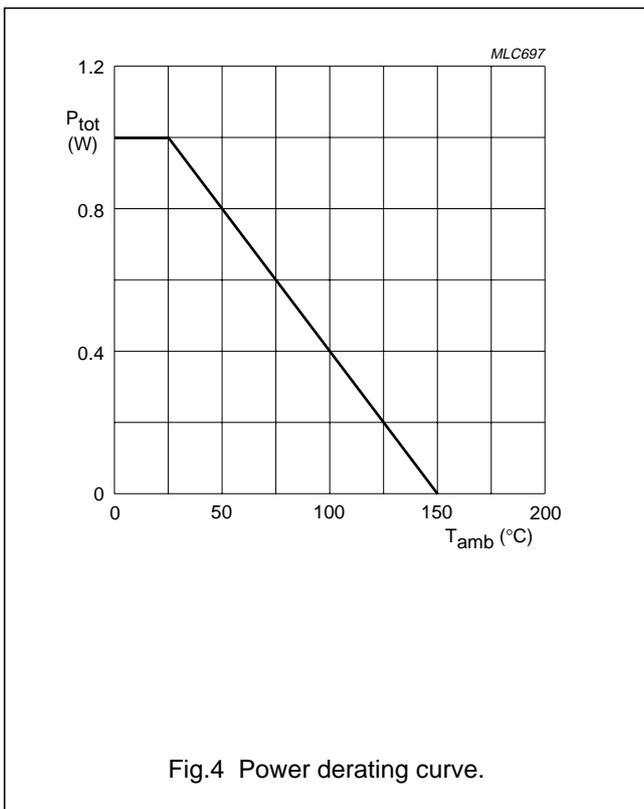
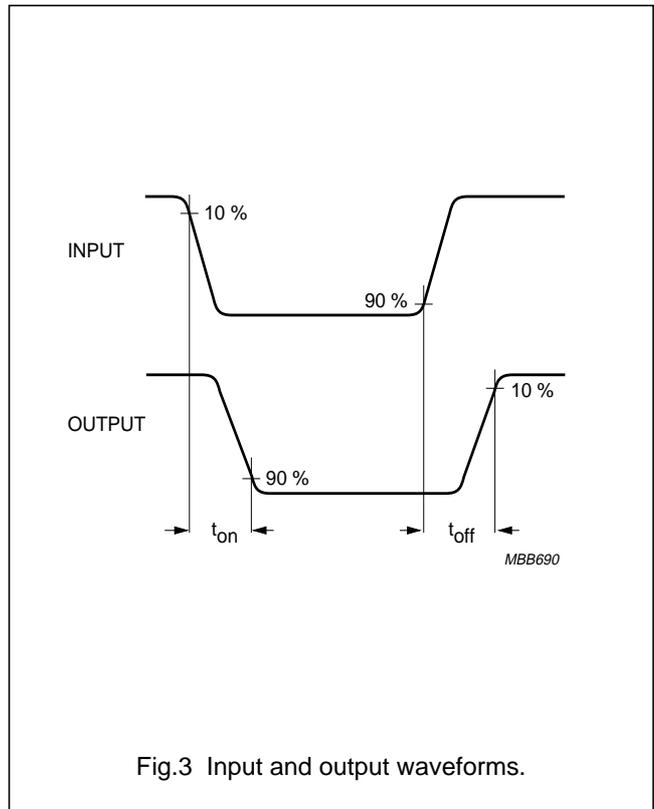
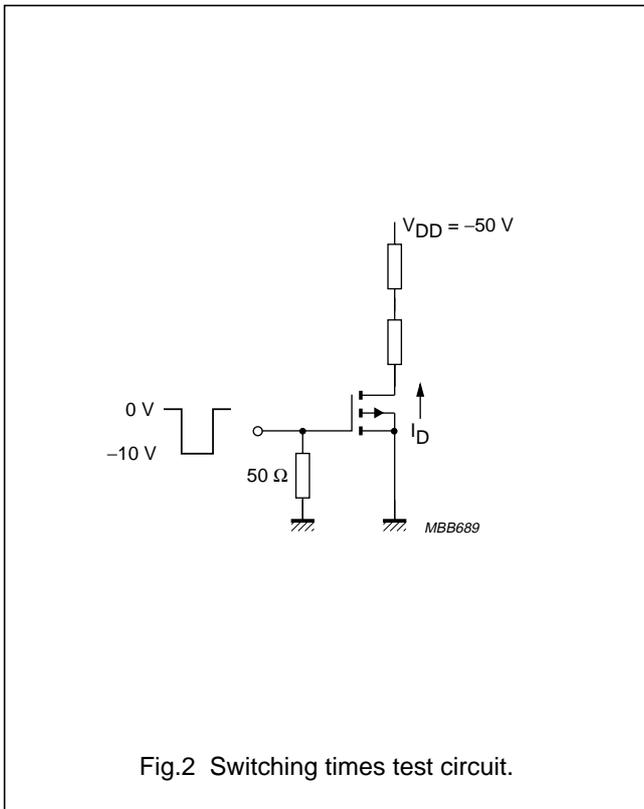
### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$ ; $I_D = -10\ \mu\text{A}$	–240	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{GS} = V_{DS}$ ; $I_D = -1\ \text{mA}$	–0.8	–	–2.8	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0$ ; $V_{DS} = -60\ \text{V}$	–	–	–200	nA
		$V_{GS} = -0.2\ \text{V}$ ; $V_{DS} = -200\ \text{V}$	–	–0.1	–60	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0$ ; $V_{GS} = \pm 20\ \text{V}$	–	–	$\pm 100$	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\ \text{V}$ ; $I_D = -200\ \text{mA}$	–	10	12	$\Omega$
$ y_{fs} $	forward transfer admittance	$V_{DS} = -25\ \text{V}$ ; $I_D = -200\ \text{mA}$	60	200	–	mS
$C_{iss}$	input capacitance	$V_{GS} = 0$ ; $V_{DS} = -25\ \text{V}$ ; $f = 1\ \text{MHz}$	–	55	90	pF
$C_{oss}$	output capacitance	$V_{GS} = 0$ ; $V_{DS} = -25\ \text{V}$ ; $f = 1\ \text{MHz}$	–	20	30	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0$ ; $V_{DS} = -25\ \text{V}$ ; $f = 1\ \text{MHz}$	–	5	15	pF
<b>Switching times</b> (see Figs 2 and 3)						
$t_{on}$	turn-on time	$V_{GS} = 0$ to $-10\ \text{V}$ ; $V_{DD} = -50\ \text{V}$ ; $I_D = -250\ \text{mA}$	–	5	10	ns
$t_{off}$	turn-off time	$V_{GS} = -10$ to $0\ \text{V}$ ; $V_{DD} = -50\ \text{V}$ ; $I_D = -250\ \text{mA}$	–	20	30	ns

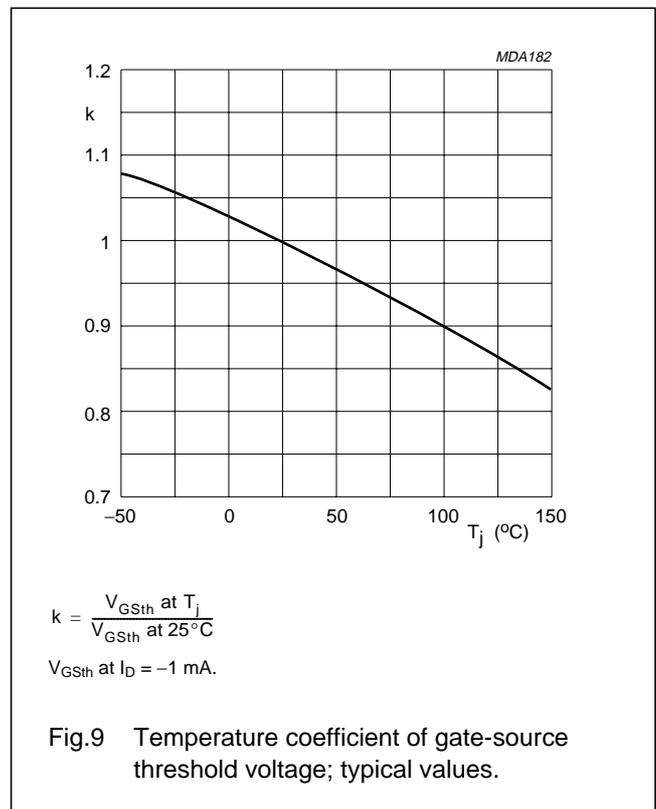
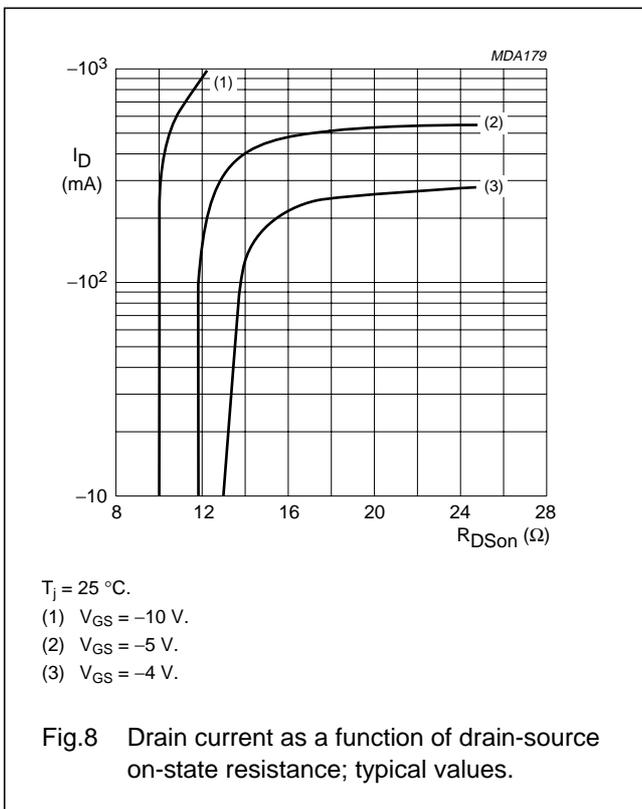
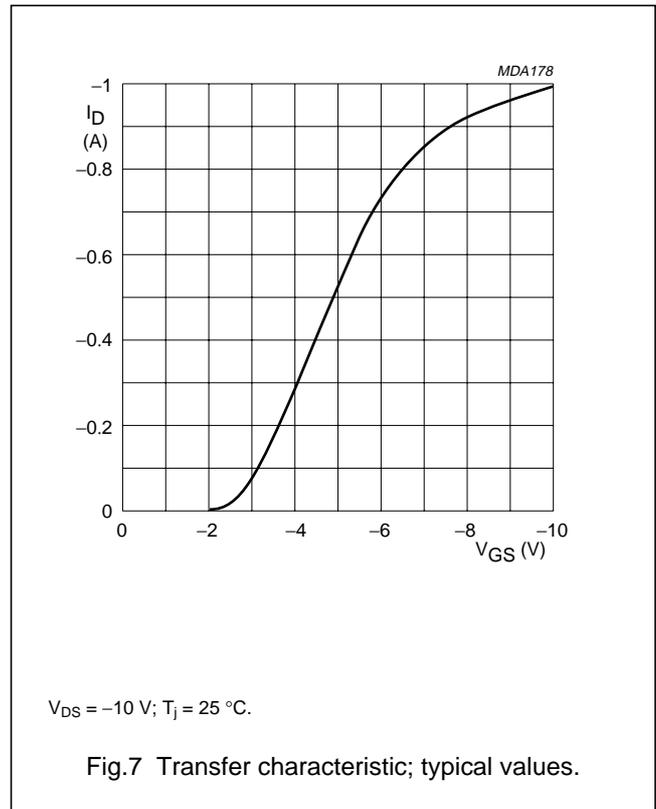
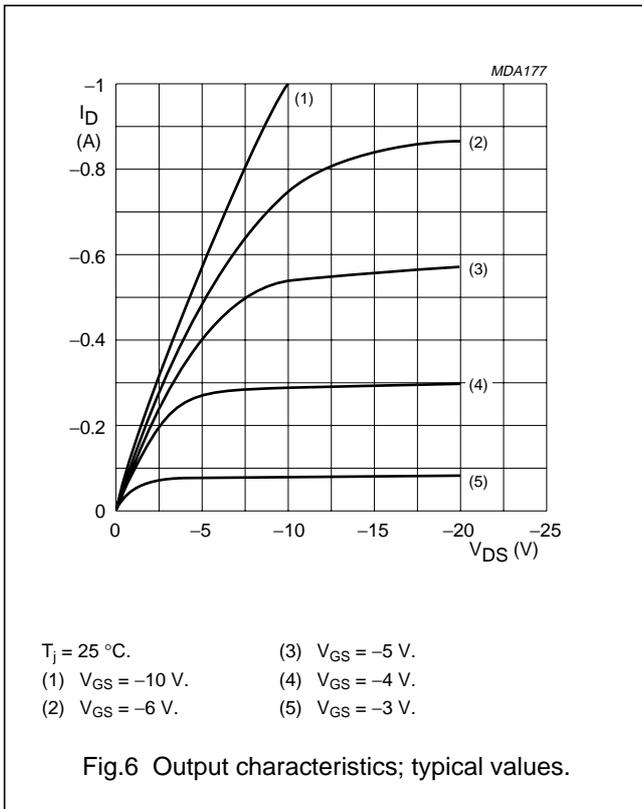
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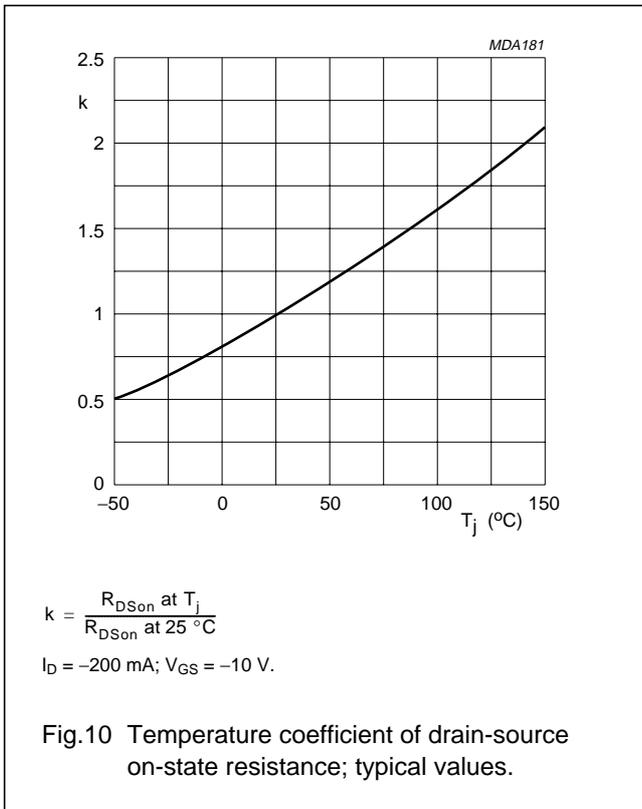
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P-channel enhancement mode  
vertical D-MOS transistor

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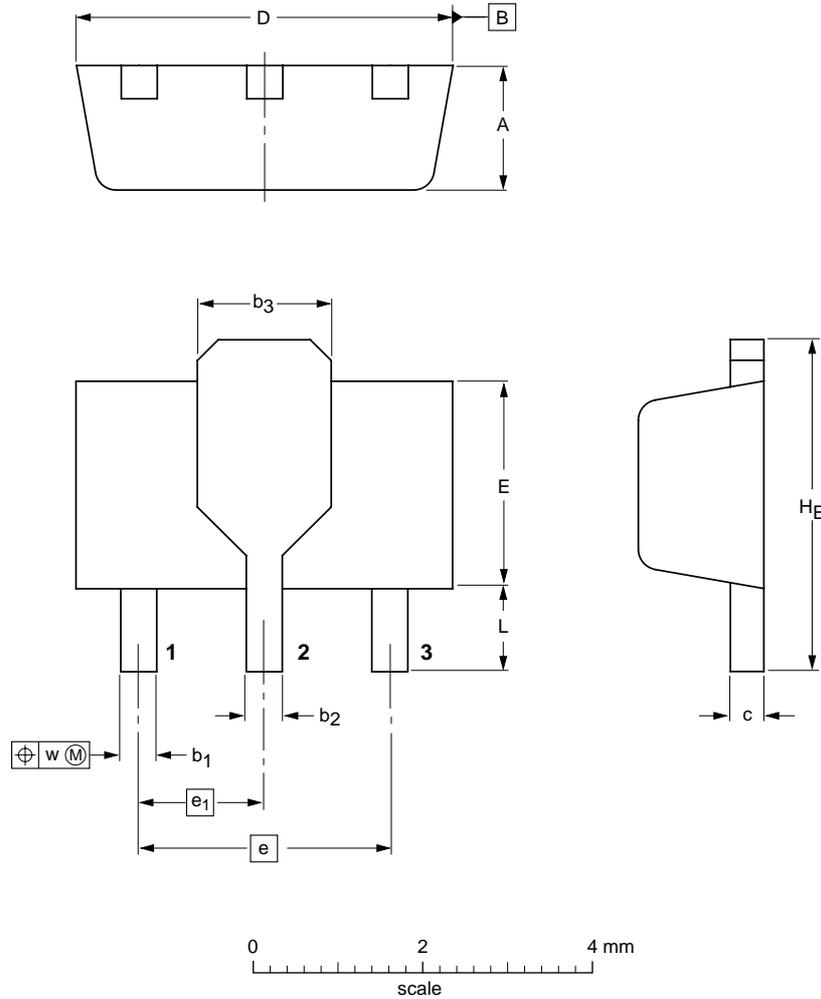
P-channel enhancement mode  
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT89		TO-243	SC-62		97-02-28 99-09-13

# P-channel enhancement mode vertical D-MOS transistor

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**NOTES**

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**NOTES**

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