

# 74ACQ241

# Octal Buffer/Line Driver with 3-STATE Outputs

#### **General Description**

The ACQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ utilizes Fairchild FACT Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- I<sub>CC</sub> and I<sub>OZ</sub> reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance

January 1990

Revised August 2001

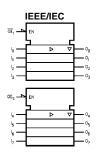
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC

## **Ordering Code:**

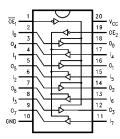
Order Number	Package Number	Package Description
74ACQ241SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACQ241PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

# **Logic Symbol**



### **Connection Diagram**



### **Pin Descriptions**

Pin Names	Description
OE₁, OE₂	3-STATE Output Enable Inputs
I <sub>0</sub> –I <sub>7</sub>	Inputs
O <sub>0</sub> -O <sub>7</sub>	Outputs

#### **Truth Tables**

Inp	uts	Outputs					
OE <sub>1</sub> I <sub>n</sub>		(Pins 12, 14, 16, 18)					
L	L	L					
L	Н	Н					
Н	Х	Z					

Inp	uts	Outputs
OE <sub>2</sub>	I <sub>n</sub>	(Pins 3, 5, 7, 9)
Н	L	L
Н	Н	Н
Н	X	Z

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

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## **Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0V

DC Input Diode Current (I<sub>IK</sub>)

 $\begin{array}{ll} V_{I} = -0.5 V & -20 \text{ mA} \\ V_{I} = V_{CC} + 0.5 V & +20 \text{ mA} \end{array} \label{eq:vi}$ 

DC Input Voltage (V<sub>I</sub>)  $-0.5V \text{ to V}_{CC} + 0.5V$ 

DC Output Diode Current (I<sub>OK</sub>)

DC Output Voltage (V<sub>O</sub>)  $-0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V}$ 

DC Output Source

or Sink Current ( $I_O$ )  $\pm$  50 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm$  50 mA

Storage Temperature (T  $_{STG}$ )  $-65^{\circ}$ C to  $+150^{\circ}$ C

DC Latch-Up Source or

Sink Current ±300 mA

Junction Temperature (T<sub>J</sub>)

DIP 140°C

# Recommended Operating Conditions

 $V_{IN}$  from 30% to 70% of  $V_{CC}$  $V_{CC}$  @ 3.0V, 4.5V, 5.5V

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT<sup>TM</sup> circuits outside databook specifications.

### **DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = +25°C T <sub>A</sub> =		T <sub>A</sub> = -40°C to +85°C Units		Conditions	
Symbol	Parameter	(V)	Тур	Guaranteed Limits		Units	Conditions	
V <sub>IH</sub>	Minimum High Level	3.0	1.5	2.1	2.1		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	3.15	3.15	V	or V <sub>CC</sub> - 0.1V	
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum Low Level	3.0	1.5	0.9	0.9		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	1.35	1.35	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum High Level	3.0	2.99	2.9	2.9			
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		2.56	2.46	V	$I_{OH} = -12 \text{ mA}$	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$	
V <sub>OL</sub>	Maximum Low Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		0.36	0.44	V	$I_{OL} = 12 \text{ mA}$	
		4.5		0.36	0.44	V	I <sub>OL</sub> = 24 mA	
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)	
I <sub>IN</sub>	Maximum Input			104	140		$V_I = V_{CC}$	
(Note 4)	Leakage Current	5.5		± 0.1	± 1.0	μΑ	GND	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 3)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub>	Maximum Quiescent	5.5		4.0	40.0		$V_{IN} = V_{CC}$	
(Note 4)	Supply Current	5.5		4.0	40.0	μΑ	or GND	
I <sub>OZ</sub>	Maximum 3-STATE						$V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$	
	Leakage Current	5.5		± 0.25	± 2.5	μΑ	$V_I = V_{CC}$ , GND	
							$V_O = V_{CC}$ , GND	
V <sub>OLP</sub>	Quiet Output	5.0	4.4	4.5		V	Figures 1, 2	
	Maximum Dynamic V <sub>OL</sub>		1.1	1.5		V	(Note 5)(Note 6)	

# DC Electrical Characteristics (Continued)

Symbol	Parameter	v <sub>cc</sub>			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
- Cymbol	r didilictor	(V)			Omico	Comunicino		
V <sub>OLV</sub>	Quiet Output	5.0 -0.6 -1.2			V	Figures 1, 2		
	Minimum Dynamic V <sub>OL</sub>	5.0	-0.0	-1.2			(Note 5)(Note 6)	
V <sub>IHD</sub>	Minimum High Level	5.0	3.1	3.5		V	(Note 5)(Note 7)	
	Dynamic Input Voltage	3.0					(14016-0)(14016-1)	
V <sub>ILD</sub>	Maximum Low Level	5.0	1.9	1.5		V	(Note 5)(Note 7)	
	Dynamic Input Voltage	5.0	1.5	1.5		•	(14016-3)(14016-1)	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4:  $I_{\rm IN}$  and  $I_{\rm CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\rm CC}$ .

Note 5: DIP package.

 $\textbf{Note 6:} \ \text{Max number of outputs defined as (n).} \ \text{Data Inputs are driven 0V to 5V.} \ \text{One output } @ \ \text{GND.}$ 

Note 7: Max number of Data Inputs (n) switching. n-1 Inputs switching 0V to 5V. Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>),

## **AC Electrical Characteristics**

		v <sub>cc</sub>		$T_A = +25^{\circ}C$		T <sub>A</sub> = -40°	C to +85°C	
Symbol	Symbol Parameter		C <sub>L</sub> = 50 pF			$C_L = 50 \text{ pF}$		Units
		(Note 8)	Min	Тур	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	3.3	2.0	6.5	9.0	2.0	9.5	ns
t <sub>PLH</sub>	Data to Output	5.0	1.5	4.5	6.0	1.5	6.5	115
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	8.0	13.0	2.5	13.5	no
t <sub>PZH</sub>		5.0	1.5	5.5	8.5	1.5	9.0	ns
t <sub>PHZ</sub>	Output Disable Time	3.3	1.0	8.5	14.5	1.0	15.0	ns
t <sub>PLZ</sub>		5.0	1.0	5.5	9.5	1.0	10.0	115
toshl	Output to Output	3.3		1.0	1.5		1.5	ns
t <sub>OSLH</sub>	Skew Data to Output (Note 9)	3.3		1.0	1.5		1.5	115

Note 8: Voltage Range 5.0 is 5.0V  $\pm$  0.5V. Voltage Range 3.3 is 3.3V  $\pm$  0.3V.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

### Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	70	pF	$V_{CC} = 5.0V$

#### **FACT Noise Characteristics**

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

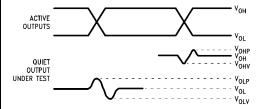
#### Equipment:

Hewlett Packard Model 8180A Word Generator PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

#### Procedure:

- 1. Verify Test Fixture Loading: Standard Load 50 pF,  $500\Omega$ .
- Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
- Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
- Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement
- Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope



#### FIGURE 1. Quiet Output Noise Voltage Waveforms

Note 10:  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference. Note 11: Input pulses have the following characteristics: f = 1 MHz,  $t_r = 3$  ns,  $t_r = 3$  ns, skew < 150 ps.

#### V<sub>OLP</sub>/V<sub>OLV</sub> and V<sub>OHP</sub>/V<sub>OHV</sub>:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a  $50\Omega$  coaxal cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V<sub>OLP</sub> and V<sub>OLV</sub> on the quiet output during the worst case transition for active and enable. Measure V<sub>OHP</sub> and V<sub>OHV</sub> on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

#### V<sub>ILD</sub> and V<sub>IHD</sub>:

- Monitor one of the switching outputs using a  $50\Omega$  coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V<sub>IL</sub>, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V<sub>IL</sub> limits, or on output HIGH levels that exceed V<sub>IH</sub> limits. The input LOW voltage level at which oscillation occurs is defined as V<sub>ILD</sub>.
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

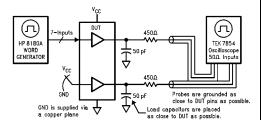
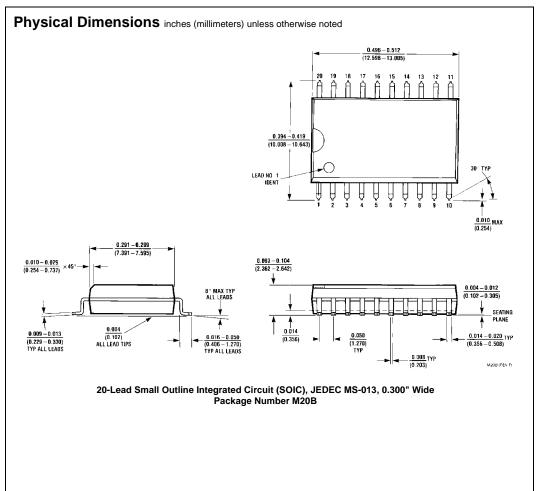
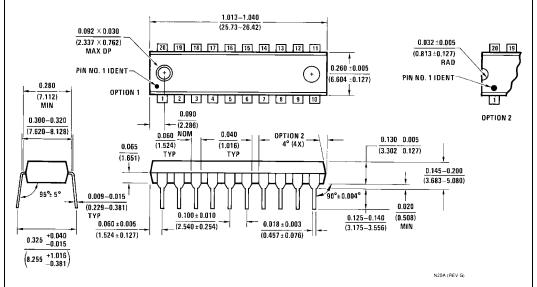


FIGURE 2. Simultaneous Switching Test Circuit



### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

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