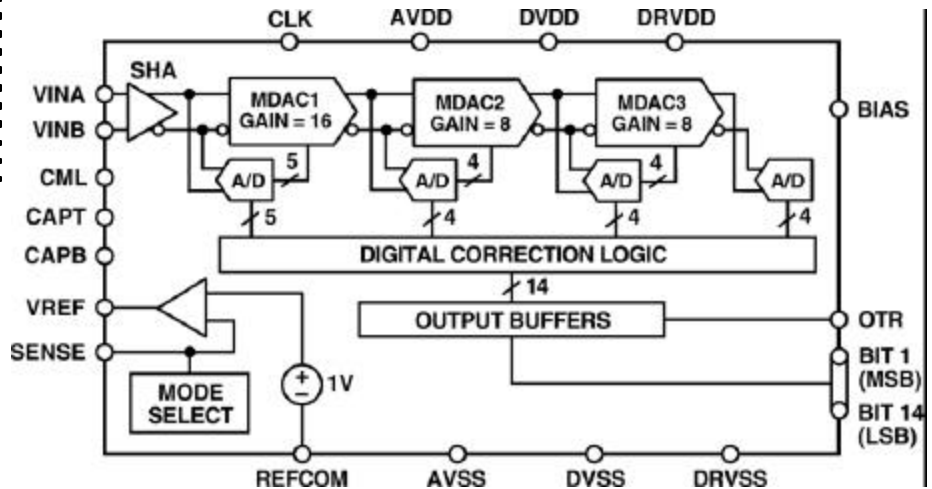
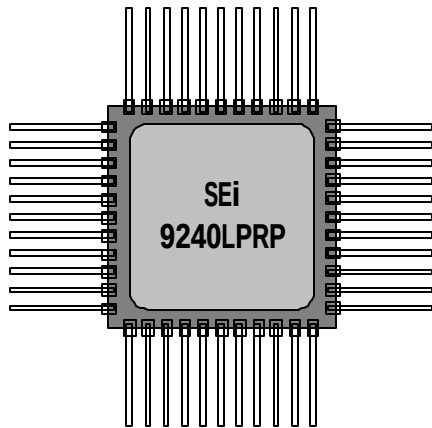




FEATURES:

- RAD-PAK® radiation-hardened against natural space radiation
- Low power dissipation: 285 mW
- Single 5V supply
- Integral nonlinearity error: 2.5 LSB
- Differential nonlinearity error: 0.6 LSB
- Input referred noise: 0.36 LSB
- Complete: On-chip sample-and-hold amplifier and voltage reference
- Signal-to-noise and distortion ratio: 77.5 dB
- Spurious-free dynamic range: 90 dB
- Out-of-range indicator
- Straight binary output data
- Total dose hardened to 100 Krads (Si); dependent on orbit and mission duration
- Single Event Latchup (SEL) protected

DESCRIPTION:

Space Electronics' 9240LPRP is a 14-bit, analog-to-digital converter that operates at a 10 MSPS rate. Manufactured with a high speed CMOS process, this monolithic ADC contains an on-chip, high performance, low noise, sample-and-hold amplifier and programmable voltage reference.

The 9240LPRP offers single supply operation and dissipates only 280 mW with a 5 volt supply. This device provides no missing codes and excellent temperature drift performance over the full operating temperature range.

Space Electronics has developed a complete Latchup Protection Technology (LPT) circuit in a single ASIC. All active LPT functions are integrated into the ASIC to protect up to three (analog and digital) supplies and up to 14 I/Os.

TABLE 1. 9240LPRP PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	DVSS	Digital Ground
2, 29	AVSS	Analog Ground
3	DVDD	5V Digital Supply
4, 28	AVDD	5V Analog Supply
5	DRVSS	Digital Output Driver Ground
6	DRVDD	Digital Output Driver Supply
7	CLK	Clock Input Pin
8-10	NC ¹	No Connect
11	BIT 14	Least Significant Data Bit (LSB)
12-23	BIT 13-BIT 2	Data Output Bits
24	BIT 1	Most Significant Data Bits (MSB)
25	OTR	Out of Range
26, 27, 30	NC ¹	No Connect
31	SENSE	Reference Select
32	VREF	Reference I/O
33	REFCOM	Reference Common
34, 38, 40, 43, 44	NC ¹	No Connect
35	BIAS ²	Power/Speed Programming
36	CAPB	Noise Reduction Pin
37	CAPT	Noise Reduction Pin
39	CML	Common-Mod Level (Midsupply)
41	VINA	Analog Input Pin (+)
42	VINB	Analog Input Pin (-)

1. Pins available as status bit.
2. See Speed/Power programmability section.

TABLE 2. 9240LPRP ABSOLUTE MAXIMUM RATINGS ¹

PARAMETER	SYMBOL	WITH RESPECT TO	MIN	MAX	UNIT
AVDD		AVSS	-0.3	6.5	V
DVDD		DVSS	-0.3	6.5	V
AVSS		DVSS	-0.3	0.3	V
AVDD		DVDD	-6.5	6.5	V
DRVDD		DRVSS	-0.3	6.5	V

TABLE 2. 9240LPRP ABSOLUTE MAXIMUM RATINGS ¹

PARAMETER	SYMBOL	WITH RESPECT TO	MIN	MAX	UNIT
DRVSS		AVSS	-0.3	0.3	V
REFCOM		AVSS	-0.3	0.3	V
CLK		AVSS	-0.3	AVDD + 0.3	V
Digital Outputs		DRVSS	-0.3	DRVDD + 0.3	V
VINA, VINB		AVSS	-0.3	AVDD + 0.3	V
VREF		AVSS	-0.3	AVDD + 0.3	V
SENSE		AVSS	-0.3	AVDD + 0.3	V
CAPB, CAPT		AVSS	-0.3	AVDD + 0.3	V
BIAS		AVSS	-0.3	AVDD + .3	V
Junction Temperature	T _J		--	150	°C
Storage Temperature	T _{STG}		-65	150	°C
Lead Temperature (10 sec)	T _L		--	300	°C

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

TABLE 3. 9240LPRP DC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, f_{SAMPLE} = 10 MSPS, R_{BIAS} = 2 kΩ, VREF = 2.5V, VINB = 2.5V, T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	AD9240	UNIT
RESOLUTION	14	Bits min
MAX CONVERSION RATE	10	MHz min
MAX REFERRED NOISE VREF = 1 V VREF = 2.5V	0.9 0.36	LSB rms typ LSB rms typ
ACCURACY Integral Nonlinearity (INL) Differential Nonlinearity (DNL) INL ¹ DNL ¹ No Missing Codes Zero Error (@ 25 °C) Gain Error (@ 25 °C) ² Gain Error (@ 25 °C) ³	 ±2.5 ±0.6 ±1.0 ±2.5 ±0.7 14 0.3 1.5 0.75	 LSB typ LSB typ LSB max LSB typ LSB typ Bits Guaranteed % FSR max % FSR max % FSR max
TEMPERATURE DRIFT Zero Error ⁴ Gain Error ^{2,4} Gain Error ^{3,4}	 3.0 20.0 5.0	 ppm/°C typ ppm/°C typ ppm/°C typ
POWER SUPPLY REJECTION	0.1	% FSR max

TABLE 3. 9240LPRP DC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, $f_{\text{SAMPLE}} = 10 \text{ MSPS}$, $R_{\text{BIAS}} = 2 \text{ k}\Omega$, VREF = 2.5V, VINB = 2.5V, T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	AD9240	UNIT
ANALOG INPUT		
Input Span (with VREF = 1.0V)	2	V p-p min
(with VREF = 2.5V)	5	V p-p max
Input (VINA or VINB) Range	0	V min
	AVDD	V max
Input Capacitance ⁵	16	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1V mode)	1	Volts typ
Output Voltage Tolerance (1V Mode) ⁴	± 14	mV max
Output Voltage (2.5V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5V Mode) ⁴	± 35	mV max
Load Regulation ⁶	5.0	mV max
REFERENCE INPUT RESISTANCE	5	k Ω typ
POWER SUPPLIES		
Supply Voltages		
- AVDD	5	V ($\pm 5\%$ AVDD Operating)
- DVDD	5	V ($\pm 5\%$ DVDD Operating)
- DRVDD	5	V ($\pm 5\%$ DRVDD Operating)
Supply Current		
- IAVDD	50	mA max (46 mA typ)
- IDRVDD	1	mA max (0.1 mA typ)
- IDVDD	15	mA max (11 mA typ)
- LPT-ASIC	30	mA max (20 mA typ)
POWER CONSUMPTION	480	mW max (385 mW typ)

1. VREF = 1V.
2. Including internal reference.
3. Excluding internal reference.
4. Guaranteed by design.
5. Sample tested.
6. Load regulation with 1 mA load current.

TABLE 4. 9240LPRP AC SPECIFICATIONS ¹(AVDD = 5V, DVDD = 5V, DRVDD = 5V, $f_{\text{SAMPLE}} = 10 \text{ MSPS}$, $R_{\text{BIAS}} = 2 \text{ k}\Omega$, VREF = 2.5V, $A_{\text{IN}} = -0.5 \text{ dBFS}$, AC COUPLED/DIFFERENTIAL INPUT, T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	AD9240	UNIT
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)		
$f_{\text{INPUT}} = 500 \text{ kHz}$	75.0	dB typ
	77.5	dB typ
$f_{\text{INPUT}} = 1.0 \text{ MHz}$	77.5	dB typ
$f_{\text{INPUT}} = 5.0 \text{ MHz}$	75.0	dB typ

TABLE 4. 9240LPRP AC SPECIFICATIONS¹(AVDD = 5V, DVDD = 5V, DRVDD = 5V, $f_{\text{SAMPLE}} = 10 \text{ MSPS}$, $R_{\text{BIAS}} = 2 \text{ kW}$, $V_{\text{REF}} = 2.5\text{V}$, $A_{\text{IN}} = -0.5 \text{ dBFS}$, AC COUPLED/DIFFERENTIAL INPUT, T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	AD9240	Unit
EFFECTIVE NUMBER OF BITS (ENOB)		
$f_{\text{INPUT}} = 500 \text{ kHz}$	12.2	Bits typ
	12.6	Bits typ
$f_{\text{INPUT}} = 1.0 \text{ MHz}$	12.6	Bits typ
$f_{\text{INPUT}} = 5.0 \text{ MHz}$	12.2	Bits typ
SIGNAL-TO-NOISE RATION (SNR)		
$f_{\text{INPUT}} = 500 \text{ kHz}$	76.0	dB typ
	78.5	dB typ
$f_{\text{INPUT}} = 1.0 \text{ MHz}$	78.5	dB typ
$f_{\text{INPUT}} = 5.0 \text{ MHz}$	78.5	dB typ
TOTAL HARMONIC DISTORTION (THD)		
$f_{\text{INPUT}} = 500 \text{ kHz}$	-78.0	dB typ
	-85.0	dB typ
$f_{\text{INPUT}} = 1.0 \text{ MHz}$	-85.0	dB typ
$f_{\text{INPUT}} = 5.0 \text{ MHz}$	-77.0	dB typ
SPURIOUS FREE DYNAMIC RANGE		
$f_{\text{INPUT}} = 500 \text{ kHz}$	90.0	dB typ
$f_{\text{INPUT}} = 1.0 \text{ MHz}$	90.0	dB typ
$f_{\text{INPUT}} = 5.0 \text{ MHz}$	80.0	dB typ
DYNAMIC PERFORMANCE		
Full Power Bandwidth	70	MHz typ
Small Signal Bandwidth	70	MHz typ
Aperture Delay	1	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step (0.0025%)	45	ns typ
Overvoltage Recovery Time	167	ns typ

1. Guaranteed by design.

TABLE 5. 9240LPRP Digital Specifications

(AVDD = 5V, DVDD = 5V, T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	AD9240	Unit
CLOCK INPUT			
High Level Input Voltage	V_{IH}	3.5	V min
Low Level Input Voltage	V_{IL}	1.0	V max
High Level Input Current ($V_{\text{IN}} = \text{DVDD}$)	I_{IH}	± 10	$\mu\text{A max}$
Low Level Input Current ($V_{\text{IN}} = 0\text{V}$)	I_{IL}	± 10	$\mu\text{A max}$
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS (with DRVDD = 5V)			
High Level Output Voltage ($I_{\text{OH}} = 50 \mu\text{A}$)	V_{OH}	4.5	V min
High Level Output Voltage ($I_{\text{OH}} = 0.5 \text{ mA}$)	V_{OH}	2.4	V min
Low Level Output Voltage ($I_{\text{OL}} = 1.6 \text{ mA}$)	V_{OL}	0.4	V max
Low Level Output Voltage ($I_{\text{OL}} = 50 \mu\text{A}$)	V_{OL}	0.1	V max
Output Capacitance	C_{OUT}	5	pF typ

TABLE 5. 9240LPRP DIGITAL SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, T_{MIN} TO T_{MAX} UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	AD9240	UNIT
LOGIC OUTPUTS (with DRVDD = 3V)			
High Level Output Voltage (I _{OH} = 50 μ A)	V _{OH}	2.4	V min
Low Level Output Voltage (I _{OL} = 50 μ A)	V _{OL}	0.7	V max

TABLE 6. 9240LPRP SWITCHING CHARACTERISTICS ¹(T_{MIN} TO T_{MAX} WITH AVDD = 5V, DVDD = 5V, DRVDD = 5V, R_{BIAS} = 2 k Ω , C_L = 20 pF)

PARAMETER	SYMBOL	AD9240	UNITS
Clock Period	t _C	100	ns min
CLOCK Pulsewidth High	t _{CH}	45	ns min
CLOCK Pulsewidth Low	t _{CL}	45	ns min
Output Delay	t _{OD}	8	ns min
		13	ns typ
		19	ns max
Pipeline Delay (Latency)		3	Clock Cycles

1. Sample tested.

TYPICAL DIFFERENTIAL CHARACTERIZATION CURVES/PLOTS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, f_{SAMPLE} = 10 MSPS, R_{BIAS} = 2 k Ω , T_A = 25 °C, DIFFERENTIAL INPUT)

FIGURE 1. TIMING DIAGRAM

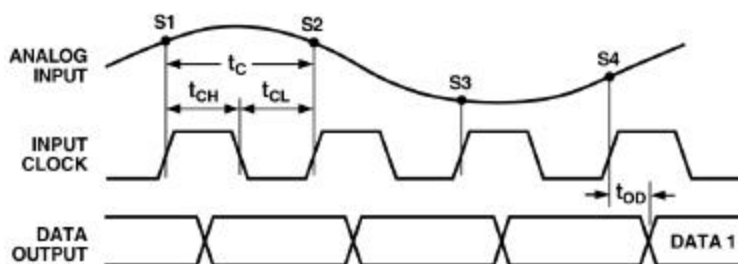


FIGURE 2. SINAD vs. INPUT FREQUENCY (INPUT SPACE = 2V, VCM = 2.5V)

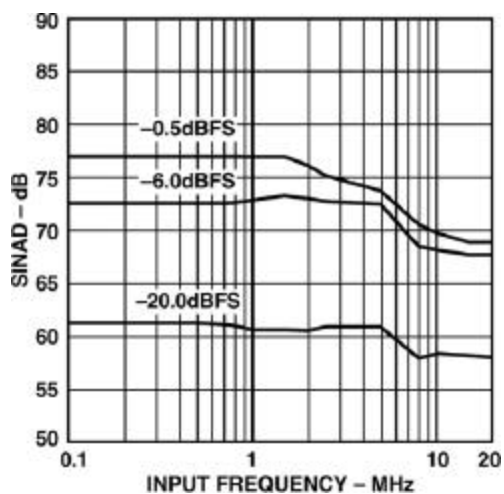


FIGURE 3. THD vs. INPUT FREQUENCY (INPUT SPAN = 5V, VCM = 2.5V)

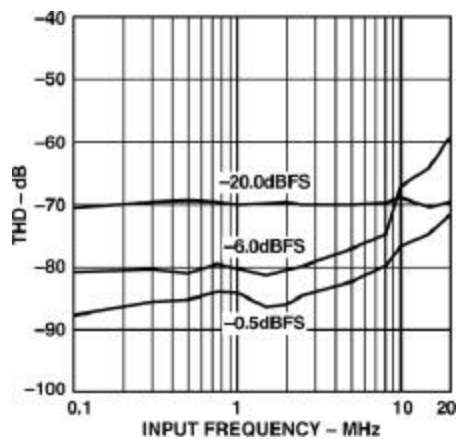


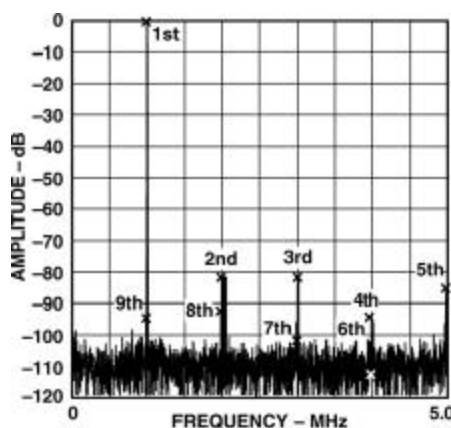
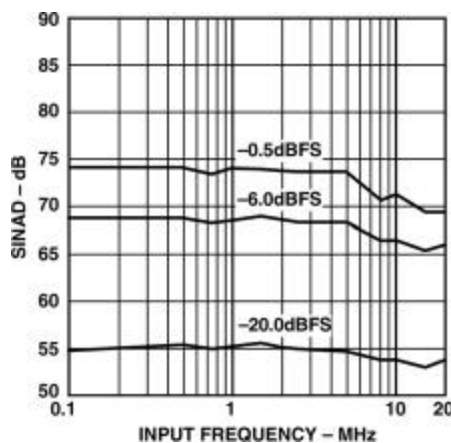
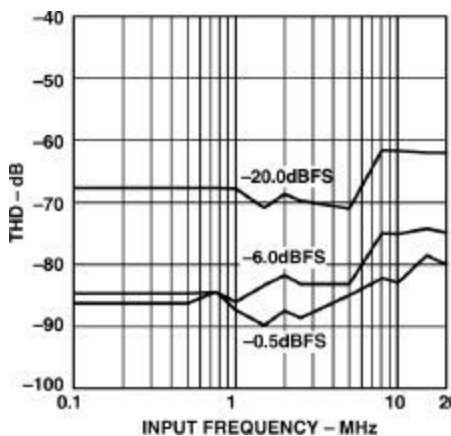
FIGURE 4. TYPICAL FFT, $f_{IN} = 1.0 \text{ MHz}$ (INPUT SPAN = 5V, $V_{CM} = 2.5V$)FIGURE 5. SINAD vs. INPUT FREQUENCY (INPUT SPAN = 2V, $V_{CM} = 2.5V$)FIGURE 6. THD vs. INPUT FREQUENCY (INPUT SPAN = 2V, $V_{CM} = 2.5V$)

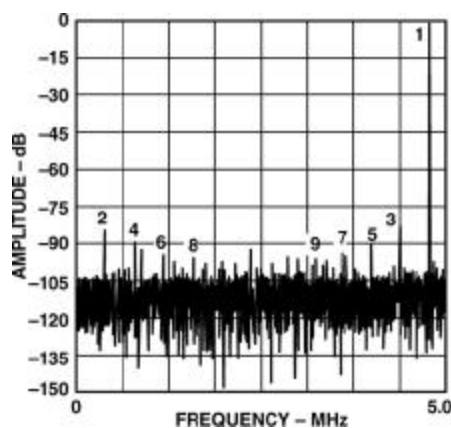
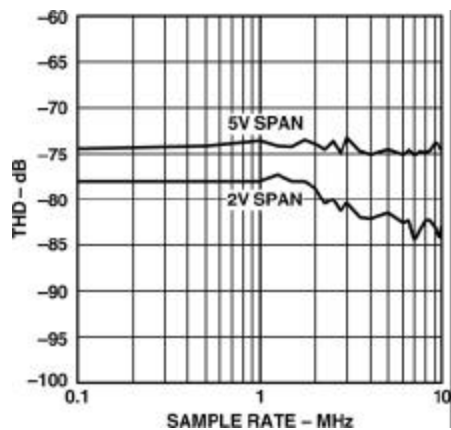
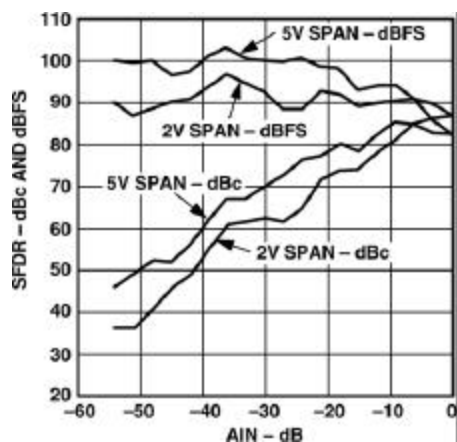
FIGURE 7. TYPICAL FFT, $f_{IN} = 5.0$ MHz (INPUT SPAN = 2V, $V_{CM} = 2.5$ V)FIGURE 8. THD VS. SAMPLE RATE ($f_{IN} = 5.0$ MHz, $A_{IN} = -0.5$ dBFS, $V_{CM} = 2.5$ V)FIGURE 9. SINGLE TONE SFDR ($f_{IN} = 5.0$ MHz, $V_{CM} = 2.5$ V)

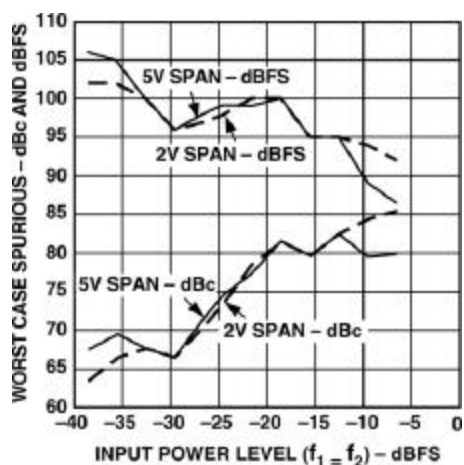
FIGURE 10. DUAL TONE SFDR ($f_1 = 0.95 \text{ MHz}$, $f_2 = 1.04 \text{ MHz}$, $V_{CM} = 2.5\text{V}$)

FIGURE 11. TYPICAL INL (INPUT SPAN = 5V)

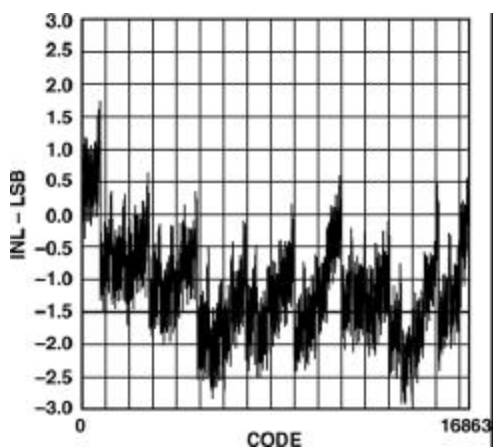


FIGURE 12. TYPICAL DNL (INPUT SPAN = 5V)

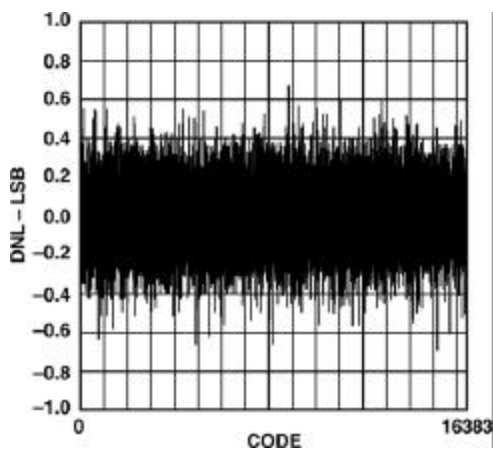


FIGURE 13. "GROUNDED-INPUT" HISTOGRAM (INPUT SPAN = 5V)

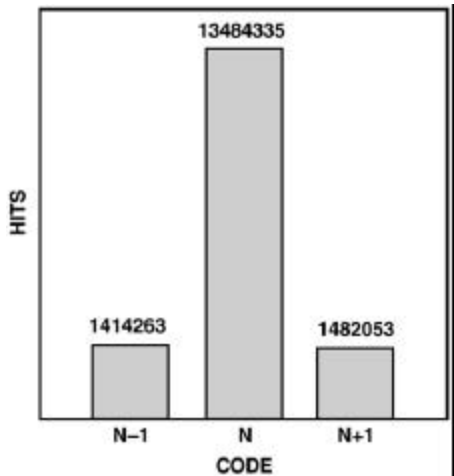


FIGURE 14. SINAD vs. INPUT FREQUENCY (INPUT SPAN = 2V, $V_{CM} = 2.5V$)

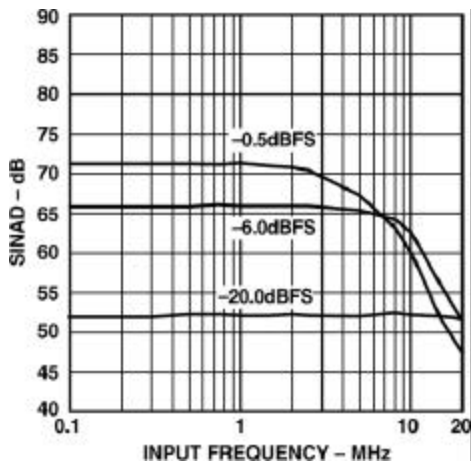


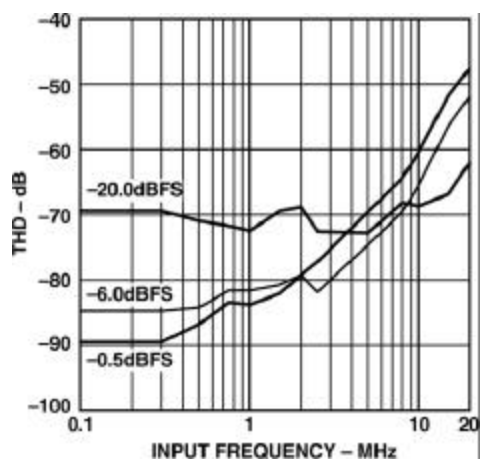
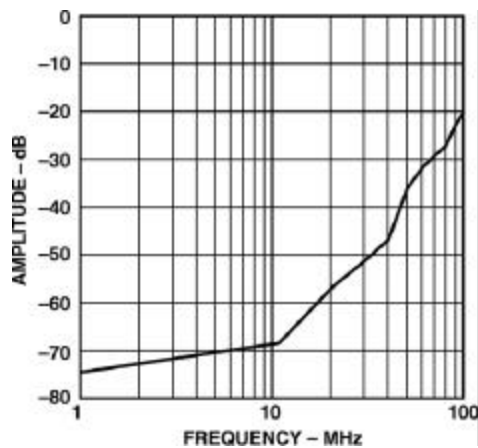
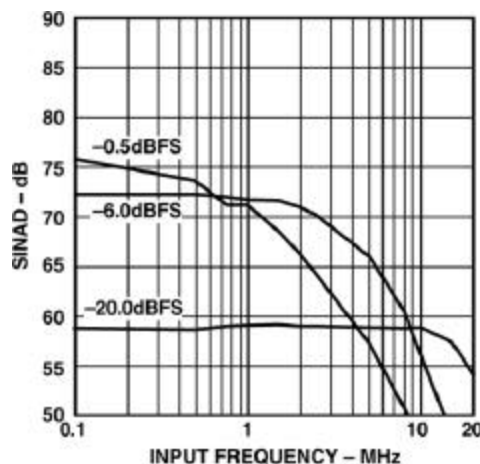
FIGURE 15. THD vs. INPUT FREQUENCY (INPUT SPAN = 5V, $V_{CM} = 2.5V$)FIGURE 16. CMR vs. INPUT FREQUENCY (INPUT SPAN = 2V, $V_{CM} = 2.5V$)FIGURE 17. SINAD vs. INPUT FREQUENCY (INPUT SPAN = 5V, $V_{CM} = 2.5V$)

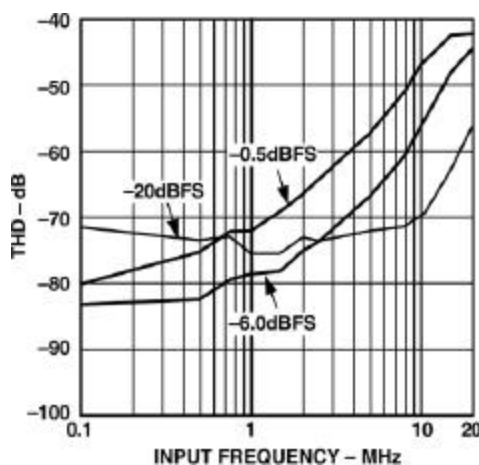
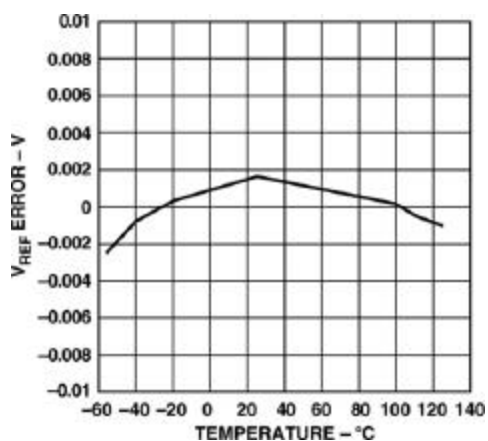
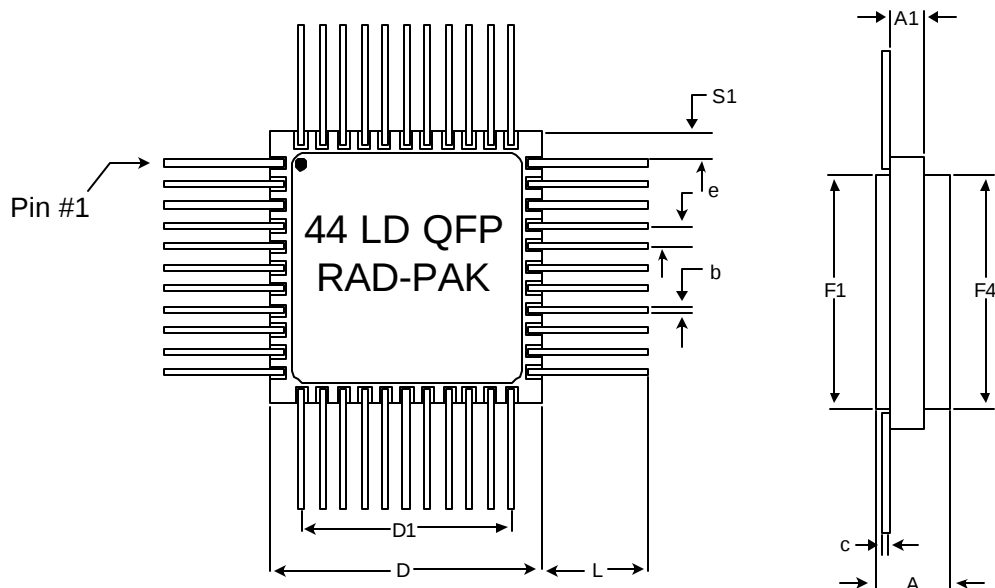
FIGURE 18. THD VS. INPUT FREQUENCY (INPUT SPAN = 5V, $V_{CM} = 2.5V$)

FIGURE 19. TYPICAL VOLTAGE REFERENCE ERROR VS. TEMPERATURE





44 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.127	0.140	0.153
b	0.015	0.017	0.019
c	0.007	0.010	0.010
D	0.642	0.650	0.658
D1	0.500 BSC		
e	0.050 BSC		
S1	0.013	0.067	--
F1	0.515	0.520	0.525
F2	0.469	0.475	0.481
L	0.265	0.275	0.285
A1	0.085	0.095	0.105
N	44		

Q44-02

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Space Electronics verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Space Electronics assumes no responsibility for the use of this information.

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