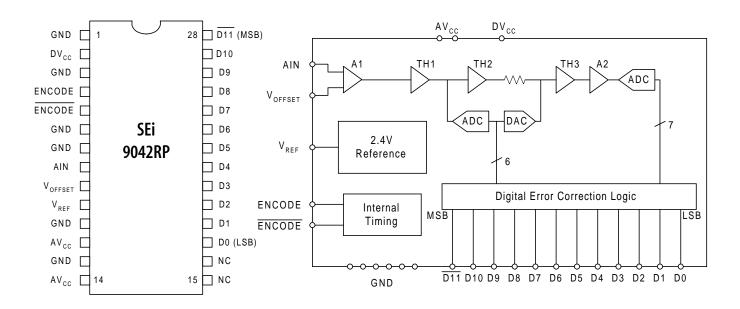


9042RP

12-Bit A/D Converter, 41 MSPS



FEATURES:

- Total dose hardness: typical 100 krad (Si); dependent upon orbit
- · 41 MSPS minimum sampling rate
- 80 dB Spurious-Free Dynamic Range (SFDR)
- · Package:
- 28 pin Rad-Pak® flat pack
- · 595 mW power dissipation
- Single 5 volt power supply
- · On-chip T/H and reference
- Two's complement output format
- · CMOS compatible output levels

DESCRIPTION:

Space Electronics'9042RP (RP for RAD-PAK®) 12-Bit monolithic analog-to-digital converter microcircuit features a typical 100 kilorad (Si) total dose tolerance; dependent upon orbit. Using SEi's radiation-hardened RAD-PAK® packaging technology, the 9042RP realizes a higher performance, and low power consumption. All necessary functions, including track-and-hold (T/H) and reference are included on chip to provide a complete convesion solution. The 9042RP runs off of a single +5V supply and provides CMOS-compatible digital outputs at 41 MSPS. Designed specifically to address the needs of wideband, multichannel receivers, the 9042RP maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 20 MHz. Noise performance is also exceptional; typical signal to noise ratio is 68 dB. Capable of surviving space environments, the 9042RP is ideal for satellite, spacecraft, and space probe missions. RAD-PAK® incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. This product is available with packaging and screening up to Class S.



RADIATION HARDENED 9042RP 12-BIT A/D CONVERTER, 41 MSPS

9042RP PIN DESCRIPTIONS

PIN NUMBER	NAME	FUNCTION FUNCTIONS	
1	GND	Ground.	
2	DV _{cc}	5 V Power Supply (Digital).	
3	GND	Ground.	
4	ENCODE	Encode input. Data conversion initiated on rising edge.	
5	ENCODE\	Complement of ENCODE. Drive differentially with ENCODE or bypass to Ground for single-ended clock mode.	
6, 7	GND	Ground.	
8	AIN	Analog Input.	
9	V _{OFFSET}	Voltage Offset Input. Sets mid-point of analog input range. Normally tied to V_{REF} through 50 Ω resistor.	
10	V _{REF}	Internal Voltage Reference. Nominally 2.4 V; normally tied to V_{OFFSET} through 50 Ω resistor. Bypass to Ground with 0.1 ${}_{\mu}\text{F}$ cap.	
11	GND	Ground.	
12	AVcc	5 V Power Supply (Analog).	
13	GND	Ground.	
14	AV _{cc}	5 V Power Supply (Analog).	
15, 16	NC	No Connects.	
17	D0 (LSB)	Digital Output Bit (Least Significant Bit).	
18-27	D1-D10	Digital Output Bits.	
28	D11\ (MSB)	Digital Output Bit (Most Significant Bit).	

9042RP ARSOLUTE MAXIMUM RATINGS1

PARAMETER	MIN	MAX	UNIT		
ELECTRICAL					
AV _{CC} Voltage	0	7	V		
DV _{CC} Voltage	0	7	V		
Analog Input Voltage	0.5	4.5	V		
Analog Input Current		20	MA		
Digital Input Voltage (ENCODE)	0	AV _{CC}	V		
ENCODE, ENCODE\ Differential Voltage		4	V		
Digital Output Current	-40	40	MA		
ENVIRONMENTAL					
Operating Temperature Range (Ambient)	-55	125	°C		
Storage Temperature Range (Ambient)	-65	150	°C		

Note:

1 Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.



9042RP

12-Bit A/D Converter, 41 MSPS

9042RP SWITCHING SPECIFICATIONS

 $(AV_{CC} = DV_{CC} = +5V \pm 10\%; ENCODE \& ENCODE) = 41 MSPS; V_{REF} tied to V_{OFFSET} through 50 \, \Omega; \, T_{MIN} = -55^{\circ}C, \, T_{MAX} = +125^{\circ}C)^1$

Parameter (Conditions)	Temp	Min	Тур	Max	Unit
Maximum Conversion Rate	Full	41			MSPS
Minimum Conversion Rate	Full			5	MSPS
Aperture Delay (t _A)	+25°C		-250		ps
Aperture Uncertainty (Jitter)	+25°C		0.7		ps rms
ENCODE Pulse Width High	+25°C	10			ns
ENCODE Pulse Width Low	+25°C	10			ns
Output Delay (t _{OD})	Full	5	9	14	ns

Note:

9042RP DC SPECIFICATIONS

 $(AV_{CC} = DV_{CC} = +5V + 10\%; V_{REF} \text{ tied to } V_{OFESET} \text{ through } 50\Omega; T_{MIN} = -55^{\circ}C, T_{MAX} = +125^{\circ}C)$

Parameter	10%; V _{REF} tied to V _{OFF}	Min	Тур	Max	Unit
RESOLUTION			12		Bits
DC ACCURACY	,		•		•
No Missing Codes	Full		Guaranteed		
Offset Error	Full	-10	±3	+10	mV
Offset Tempco	Full		25		ppm/°C
Gain Error	Full	-6.5	0	+6.5	% FS
Gain Tempco	Full		-50		ppm/°C
REFERENCE OUT (V _{REF}) ²	+25°C		2.4		V
ANALOG INPUT (AIN)					
Input Voltage Range			V _{REF} ±0.500		V
Input Resistance	Full	200	250	300	Ω
Input Capacitance⁵	+25°C		7		pF
ENCODE INPUT 3					•
Logic Compatibility ⁴			TTL/CMOS		
Logic "1" Voltage	Full	2.0		5.0	V
Logic "0" Voltage	Full	0		0.9	V
Logic "1" Current (V _{INH} = 5 V)	Full	450	625	800	μA
Logic "0" Current (V _{INL} = 0 V)	Full	-400	-300	-200	μA
Input Capacitance⁵	+25°C		2.5		pF
DIGITAL OUTPUTS					
Logic Compatibility			CMOS		
Logic "1" Voltage ($I_{OH} = 10 \mu A$)	+25°C	3.5	4.2		V
	Full	3.5			V
Logic "0" Voltage ($I_{OL} = 10 \mu A$)	+25°C		0.75	0.80	V
•	Full			0.90	V
Output Coding		Two's Complement			
POWER SUPPLY					
AV _{CC} Supply Voltage	Full		5.0		V
I (AV _{CC}) Current	Full			160	mA
DV _{CC} Supply Voltage	Full		5.0		V
I (DV _{CC}) Current	Full			20	mA
I _{CC} (Total) Supply Current	Full			180	mA
Power Dissipation	Full			990	mW
Power Supply Rejection	+25°C	-20	±1	+20	mV/V
(PSRR)	Full		±5		mV/V

Notes

- 1 C1 tied to GND through 0.01 mF capacitor.
- $2\ V_{REF}$ is normally tied to V_{OFFSET} through $50\ \Omega$. If V_{REF} is used to provide dc offset to other circuits, it should first be buffered.
- 3 ENCODE driven by single-ended source; ENCODE\ bypassed to ground through 0.01 μF capacitor.
- 4 ENCODE may also be driven differentially in conjunction with ENCODE.
- Specifications subject to change without notice.
- 5 Guaranteed by design.

¹ C1 tied to GND through 0.01 μ F capacitor.



9042RP

12-Bit A/D Converter, 41 MSPS

9042RP AC SPECIFICATIONS¹

 $(AV_{CC} = DV_{CC} = +5V_{+}10\%; ENCODE \& ENCODE = 41 MSPS; V_{RFF} tied to V_{OFFSFT} through 50 \, \Omega; T_{MIN} = -55^{\infty}C, T_{MAX} = +125^{\infty}C)^2$

Parameter	Temp	Min	Тур	Max	Unit
SNR ²					
Analog Input 1.2MHz	+25°C		68		dB
@ -1 dBFS	Full		67.5		dB
9.6 MHz	+25°C		67.5		dB
	Full		67		dB
19.5MHz	+25°C		67		dB
	Full		66.5		dB
SINAD ³					
Analog Input 1.2 MHz	+25°C		67.5		dB
@ -1 dBFS	Full		67		dB
9.6 MHz	+25°C		67.5		dB
	Full		67		dB
19.5MHz	+25°C		67		dB
	Full		66.5		dB
Worst Spur⁴					
Analog Input 1.2MHz	+25°C		80		dBc
@ -1 dBFS	Full		78		dBc
9.6 MHz	+25°C		80		dBc
	Full		78		dBc
19.5 MHz	+25°C		80		dBc
	Full		78		dBc
Small Signal SFDR (w/Dither)⁵					
Analog Input @ 1.2 MHz	Full		90		dBFS
9.6 MHz	Full		90		dBFS
19.5 MHz	Full		90		dBFS
Two-Tone IMD Rejection ⁶	F				JD -
F1, F2 @ -7 dBFS	Full		80		dBc
Two Tone SFDR (w/Dither) ⁷	Full		90		dBFS
Thermal Noise	+25°C	4.0	0.33	4.0	LSB rms
Differential Nonlinearity	+25°C	-1.0	±0.3	+1.0	LSB
(ENCODE = 20 MSPS)	Full	-1.0		+1.25	LSB
Integral Nonlinearity	F		0.75		LCD
(ENCODE = 20 MSPS)	Full		±0.75		LSB
Analog Input Bandwidth ⁸	+25°C		100		MHz
Transient Response8	+25∘C		10		ns
Overvoltage Recovery Time ⁸	+25°C		25		ns

Notes

- 1 All ac specifications tested by driving ENCODE and ENCODE\ differentially.
- 2 Analog input signal power at -1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed).
- 3 Analog input signal power at -1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics.
- 4 Analog input signal power at -1 dBFS; worst spur is the ratio of the signal level to worst spur, usually limited by harmonics.
- 5 Analog input signal power swept from -20 dBFS to -95 dBFS; dither power = -32.5 dBm; dither circuit used on input signal SFDR is ratio of converter full scale to worst spur.
- 6 Tones at -7 dBFS (F1 = 15.3 MHz, F2 = 19.5 MHz); two tone intermodulation distortion (IMD) rejection is ratio of either tone to worst third order intermod product.
- 7 Both input tones swept from -20 to -95 dBFS; Dither power = -32.5 dBm; dither circuit used on input signal (see "Overcoming Static Nonlinearities with Dither);

two tone spurious-free dynamic range (SFDR) is the ratio of converter full scale to worst spur.

8 Guaranteed by design.



9042RP

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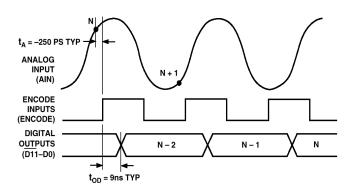


Figure 1. Timing Diagram

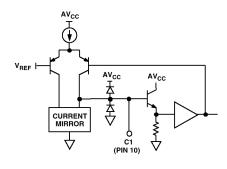


Figure 4. Compensation Pin, C1

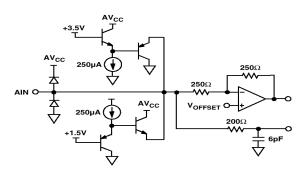


Figure 2. Analog Input Stage

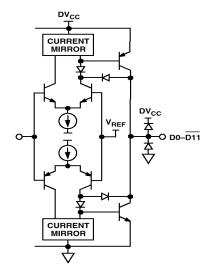


Figure 5. Digital Output Stage

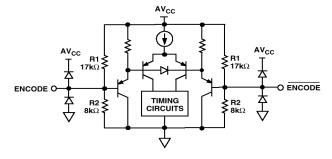


Figure 3. Encode Inputs

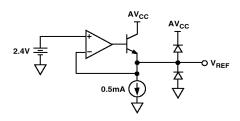


Figure 6. 2.4 V Reference



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9042RP TYPICAL PERFORMANCE CHARACTERISTICS

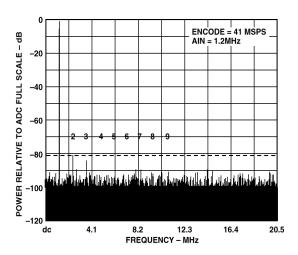


Figure 7. Single tone at 1.2MHz

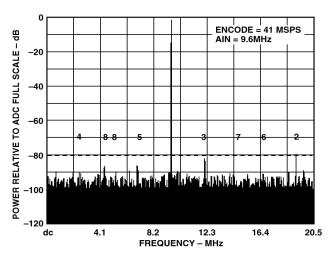


Figure 8. Single Tone at 9.5MHz

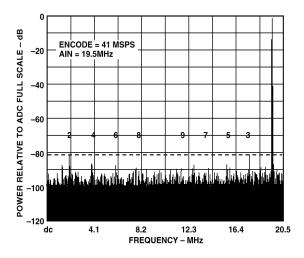


Figure 9. Single tone at 19.5MHz

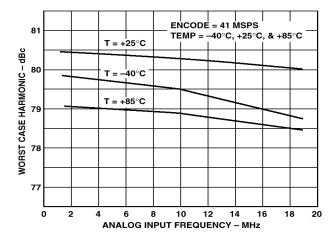


Figure 10. Harmonics vs. AIN



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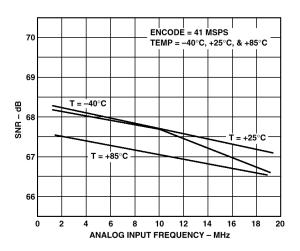


Figure 11. Noise vs. AIN

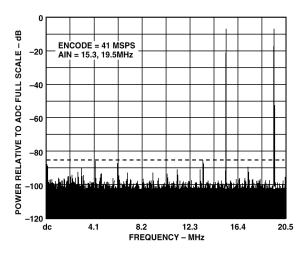


Figure 13. Two Tones at 15.9MHz and 19.6MHz

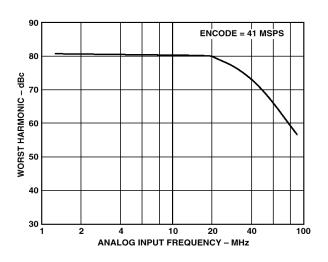


Figure 12. Harmonics vs. AIN

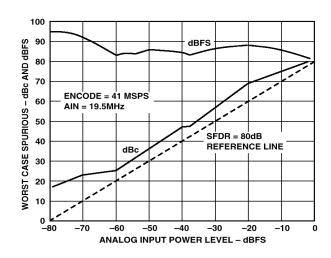


Figure 14. Single Tone SFDR



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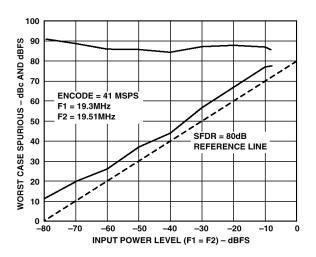


Figure 15. Two Tones SFDR

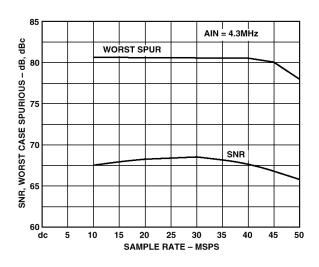


Figure 16. SNR Worst Harmonic vs. Encode

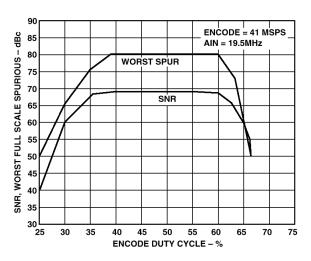


Figure 17. SNR Worst Case Spurious vs. Duty Cycle

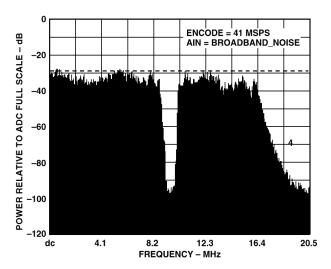
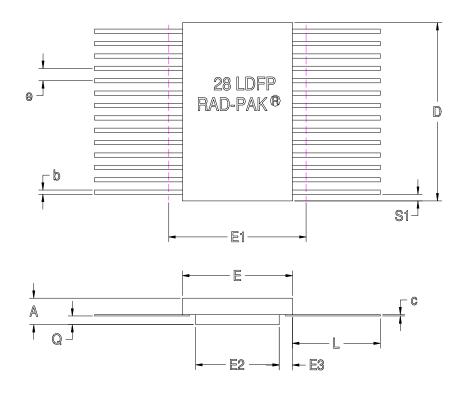


Figure 18. NPR Output Spectrum



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28 Pin RAD-PAK® Flat Package

SYMBOL	DIMENSION			
	MIN	NOM	MAX	
Α	0.129	0.142	0.155	
b	0.015	0.017	0.022	
С	0.004	0.005	0.009	
D		0.820	0.828	
E	0.474	0.480	0.486	
E1			0.506	
E2	0.255	0.260		
E3	0.000	0.110		
е	0.050 BSC			
L	0.375	0.385	0.395	
Q	0.021	0.025	0.029	
S1	0.000	0.077		
N	28			

F28-12



<u>9042RP</u>

12-Bit A/D Converter, 41 MSPS

Important Notice:

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