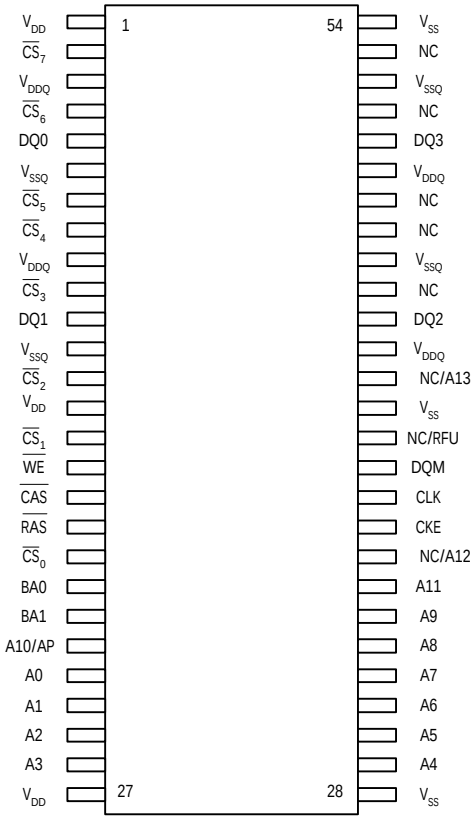
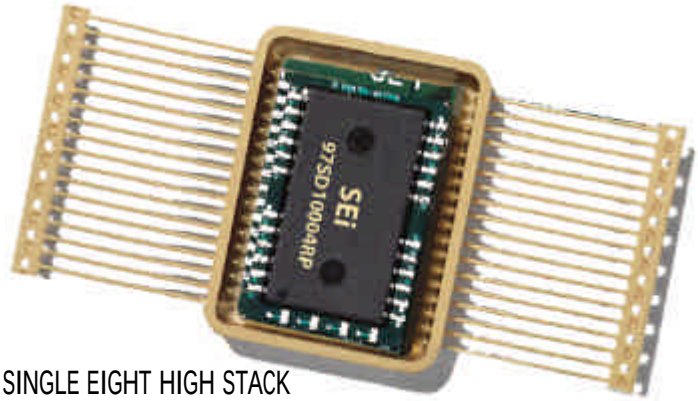
PRELIMINARY

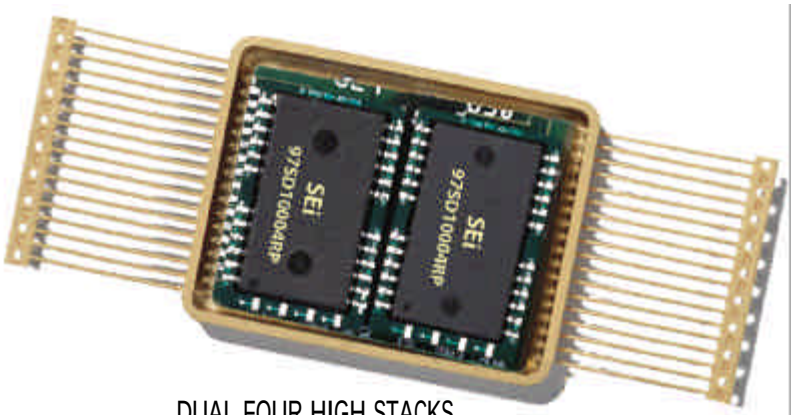
SPACE ELECTRONICS INC.
SPACE PRODUCTS

1 GIGABIT SYNCHRONOUS DRAM
97SD10004RP





SINGLE EIGHT HIGH STACK



DUAL FOUR HIGH STACKS

FEATURES:

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
- CAS latency (2 & 3)
- Burst length (1, 2, 4, 8 Page)
- Burst type (Sequential & Interleave)
- Il inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)
- TID
  - Total dose tolerance is 100 krads (Si); dependent upon orbit
- SEL:
  - No Single Event Latch-up observed
  - $SEL_{TH} > 82$ MeV/mg/cm^2
- SEU:
  - $LET_{TH} = 15$ MeV/mg/cm^2
  - cross section = 3E-08 cm^2/bit

DESCRIPTION:

Space Electronics' is offering a One Gigabit synchronous high data rate Dynamic RAM in a very compact hermetic package using stacked TSOPs. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications for space. The patented radiation-hardened Rad-Pak® technology incorporates radiation shielding in a microcircuit package. It eliminates box shielding while providing required lifetime in orbit. This product is available with packaging and screening up to Class S. This product is upgradable to 2 or 4 Gb with identical footprints.

(858) 452-4167 - Fax: (858) 452-5499 - www.spaceelectronics.com

BLOCK DIAGRAM

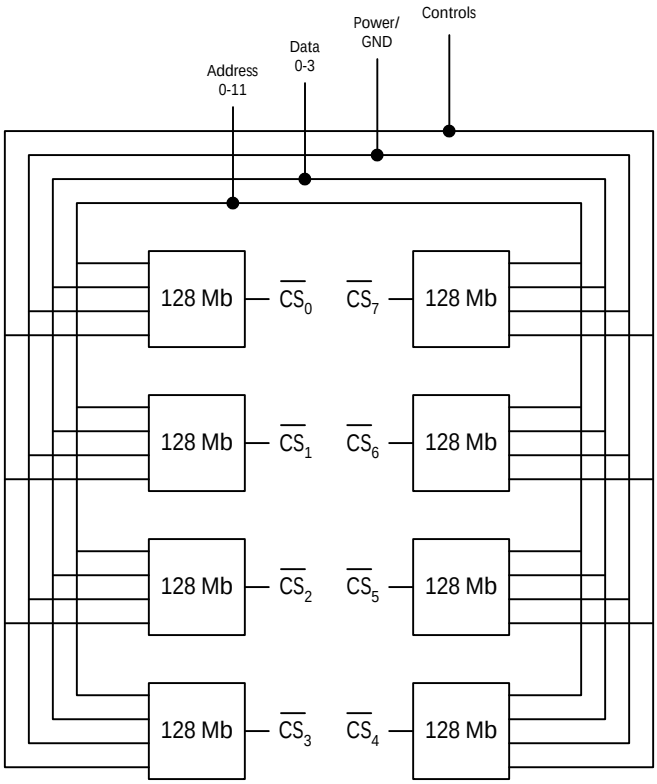


TABLE 1. ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0	4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0	4.6	V
Storage temperature	T_{STG}	-55	150	°C
Power dissipation	P_D		1	W
Short circuit current	I_{OS}		50	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

TABLE 2. DC OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS (VOLTAGE REFERENCED TO V_{SS} = 0V, T_A = -40 TO 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V
Input logic high voltage [1]	V_{IH}	2.0	3.0	V_{DD}+0.3	V
Input logic low voltage [2]	V_{IL}	-0.3	0	0.8	V
Output logic high voltage (I_{OH} = -2mA)	V_{OH}	2.4	-	-	V

TABLE 2. DC OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS (VOLTAGE REFERENCED TO V_{SS} = 0V, T_A = -40 TO 85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Output logic low voltage (I_{OL} = 2mA)	V_{OL}	-	-	0.4	V
Input leakage current [3,4]	I_{LI}	-10	-	10	uA

1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}. Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

TABLE 3. CAPACITANCE

(V_{DD} = 3.3V, T_A = 23 ºC f = 1 MHz, V_{REF} = 1.4V ± 200 mV)

PIN	SYMBOL	MIN	MAX	UNIT
Clock [1]	C_{CLK}	2.5	32	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM [2]	C_{IN}	2.5	40	pF
Address [2]	C_{ADD}	2.5	40	pF
DQ_0 ~ DQ_3 [3]	C_{OUT}	4.0	52	pF

1. -A only specify a maximum value of 3.5 pF.
2. -A only specify a maximum value of 3.8 pF.
3. -A only specify a maximum value of 6.0 pF.

TABLE 4. DC CHARACTERISTICS

(T_A = -40 TO 85°C UNLESS OTHERWISE SPECIFIED.)

PARAMETER	SYMBOL	TEST CONDITION	MAX	UNIT
Operating current (One bank active) [1]	I_{CC1}	Burst length = 1 t_{RC} ³ t_{RC}(min) I_O = 0 mA	160	mA
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10 ns	8	mA
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	8	mA
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10 ns Input signals are changed one time during 20ns	160	mA
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	56	mA
Active standby current in power-down mode [1]	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10 ns	40	mA
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	40	mA
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10 ns Input signals are changed one time during 20 ns	240	mA

TABLE 4. DC CHARACTERISTICS

(T_A = -40 TO 85°C UNLESS OTHERWISE SPECIFIED.)

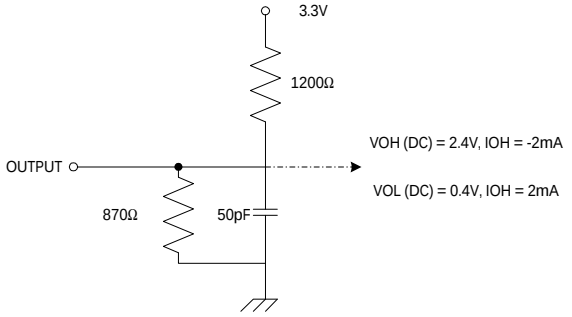
PARAMETER	SYMBOL	TEST CONDITION	MAX	UNIT
Active standby current in non power-down mode (One bank active)	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	160	mA
Operating current (Burst mode)	I_{CC4}	IO = 0 mA Page burst t_{CCD} = 2 CLKs	180	mA
			260	mA
Refresh current [2]	I_{CC5}	t_{RC} ≥ t_{RC}(min)	12	mA
Self refresh current	I_{CC6}	CKE ≤ 0.2V	6.4	mA

1. Measured with outputs open.
2. Refresh period is 64ms.

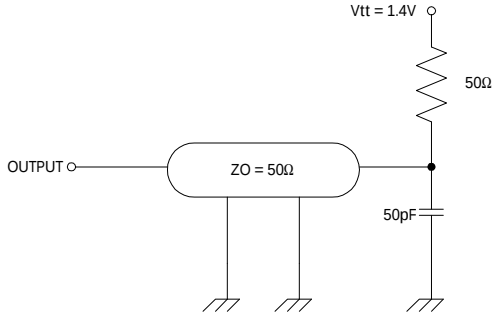
TABLE 5. AC OPERATING TEST CONDITIONS

(V_{DD} = 3.3V ± 0.3V, T_A = 0 TO 70°C)

PARAMETER	VALUE	UNIT
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See AC Output Load Circuit	



DC Output Load Circuit



AC Output Load Circuit

TABLE 6. OPERATING AC PARAMETER

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Row active to row active delay [1]	t_{RRD}	20	--	--	ns
RAS to CAS delay [1]	t_{RCD}	20	--	--	ns
Row precharge time [1]	t_{RP}	20	--	--	ns

TABLE 6. OPERATING AC PARAMETER

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Row active time [1]	t_{RAS}	50	--	--	ns
		--	--	100	µ
Row cycle time [1]	t_{RC}	70	--	--	ns
Last data in to row precharge [2]	$t_{RDL\ (min)}$	--	2	--	CLK
Last data in to Active delay	$t_{DAL\ (min)}$	--	2 CLK + 20 ns	--	CLK
Last data in new col. address delay [2]	$t_{CDL\ (min)}$	--	1	--	CLK
Last data in to burst stop[2]	$t_{BDL\ (min)}$	--	1	--	CLK
Col. address to col. address stop [3]	$t_{CCD\ (min)}$	--	1	--	CLK
Number of valid output data [4]	CAS latency = 3	--	2	--	ea
	CAS latency = 2	--	--	1	ea

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

TABLE 7. AC CHARACTERISTICS

PARAMETER		SYMBOL	MIN	MAX	UNIT
CLK cycle time [1]	CAS latency = 3	t_{CC}	10	1000	ns
	CAS latency = 2		12	1000	
CLK to valid output delay [1,2]	CAS latency = 3	t_{SAC}	--	6	ns
	CAS latency = 2		--	7	
Output data hold time [2]	CAS latency = 3	t_{OH}	3	--	ns
	CAS latency = 2		3	--	
CLK high pulse width [3]		t_{CH}	3	--	ns
CLK low pulse width [3]		t_{CL}	3	--	ns
Input setup time [3]		t_{SS}	2	--	ns
Input hold time [3]		t_{SH}	1	--	ns
CLK to output in Low-Z [2,4]		t_{SLZ}	1	--	ns
CLK to output in High-Z [4]	CAS latency = 3	t_{SHZ}	--	6	ns
	CAS latency = 2		--	7	

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)= 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.
4. Not tested.

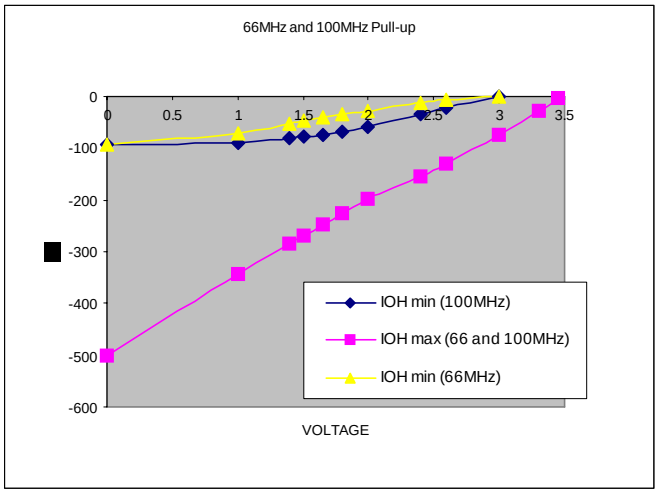
TABLE 8. DQ BUFFER OUTPUT DRIVE CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output rise time [2,3]	trh	Measure in linear region: 1.2V ~1.8V	1.37	--	4.37	V/ns
Output fall time [2,3]	tfh	Measure in linear region: 1.2V ~ 1.8V	1.30	--	3.8	V/ns
Output rise time [3,4,5]	trh	Measure in linear region: 1.2V ~ 1.8V	2.80	3.90	5.60	V/ns
Output fall time [3]	tfh	Measure in linear region: 1.2V ~ 1.8V	2.0	2.9	5.0	V/ns

1. All measurements done with respect to V_{SS}.
2. Measured into 50 pF only, use these values to characterize to.
3. Not tested.
4. Rise time specification based on 0 pF + 50 Ω to V_{SS}, use these values to design to.
5. Fall time specification based on 0 pF + 50 Ω to V_{DD}, use these values to design to.

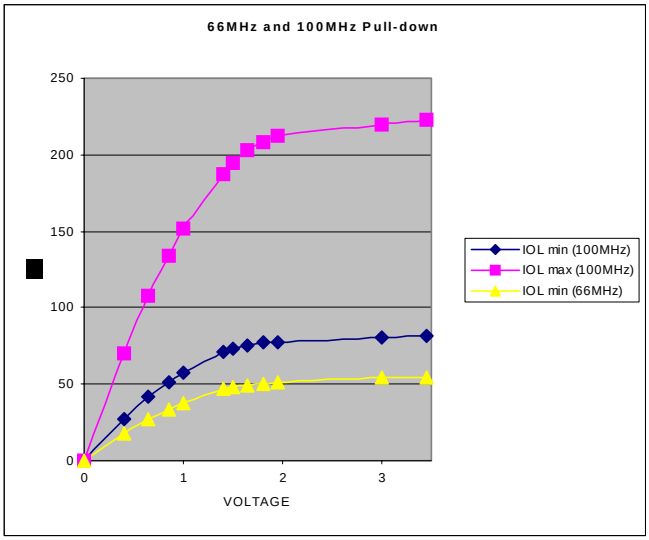
I_{OH} CHARACTERISTICS (PULL-UP)

VOLTAGE	100MHZ MIN	100MHZ MAX	66MHZ MIN
(V)	I (mA)	I (mA)	I (mA)
3.45	--	-2.4	--
3.3	--	-27.3	--
3.0	0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0



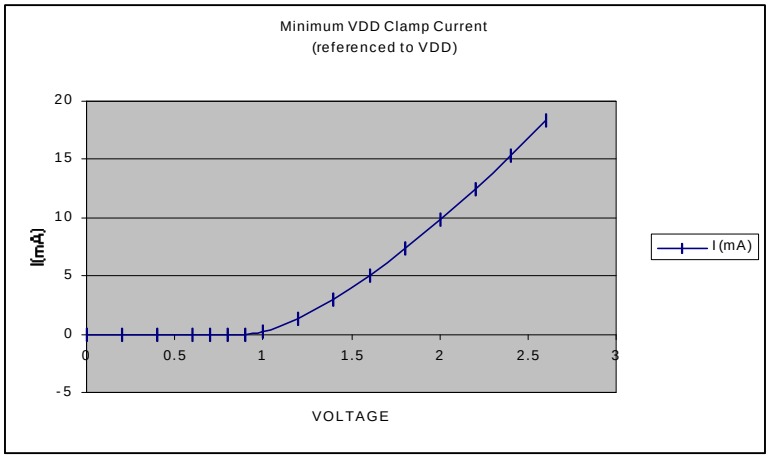
I_{OL} CHARACTERISTICS (PULL-DOWN)

VOLTAGE	100MHZ MIN	100MHZ MAX	66MHZ MIN
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9



V_{DD} CLAMP @CLK,CKE,$\overline{CS}$,DQM & DQ

V_{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



V_{SS} CLAMP @CLK,CKE,$\overline{CS}$,DQM & DQ

V_{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

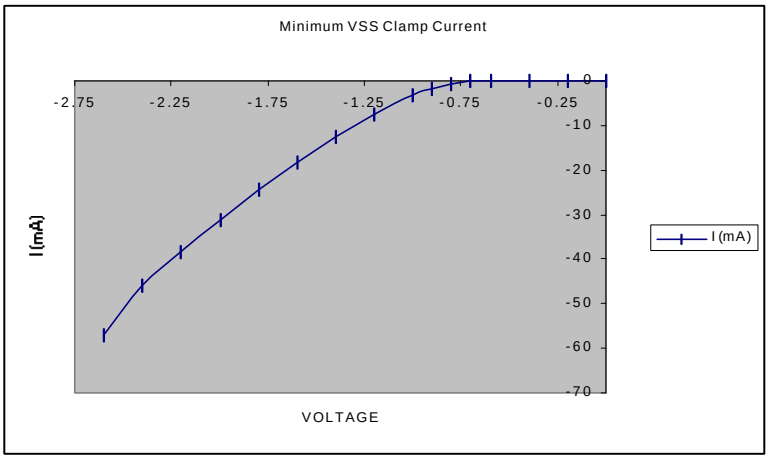


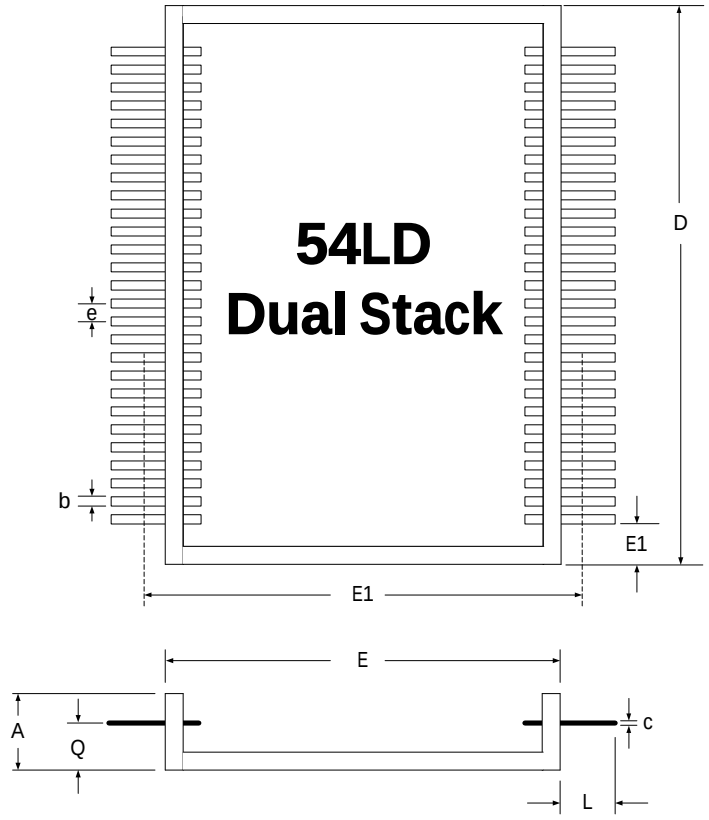
TABLE 9. SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don¢t Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11, A9 ~ A0
Register	Mode Register Set [1]		H	X	L	L	L	L	X	OP CODE [2]		
Refresh [3]	Auto Refresh		H	H	L	L	L	H	X	X		
	Self Refresh	Entry		L								
		Exit	L	H	L	H	H	H	X	X		
				H	H	X	X	X				
Bank Active & Row Address			H	X	L	L	H	H	X	V	Row Address	
Read & Column Address	Auto Precharge Disable [4]		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9, A11)
	Auto Precharge Enable [4, 5]										H	
Write & Column Address	Auto Precharge Disable [4]		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9, A11)
	Auto Precharge Enable [4, 5]										H	
Burst Stop [6]			H	X	L	H	H	L	X	X		
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X
	All banks									X	H	
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X		
					L	V	V	V				
		Exit	L	H	X	X	X	X	X			
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X		
					L	H	H	H				
		Exit	L	H	H	X	X	X	X			
					L	V	V	V				
DQM [7]			H	X					V	X		
No Operation Command			H	X	H	X	X	X	X	X		
					L	H	H	H				

1. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
2. OP Code : Operand Code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@MRS)
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.

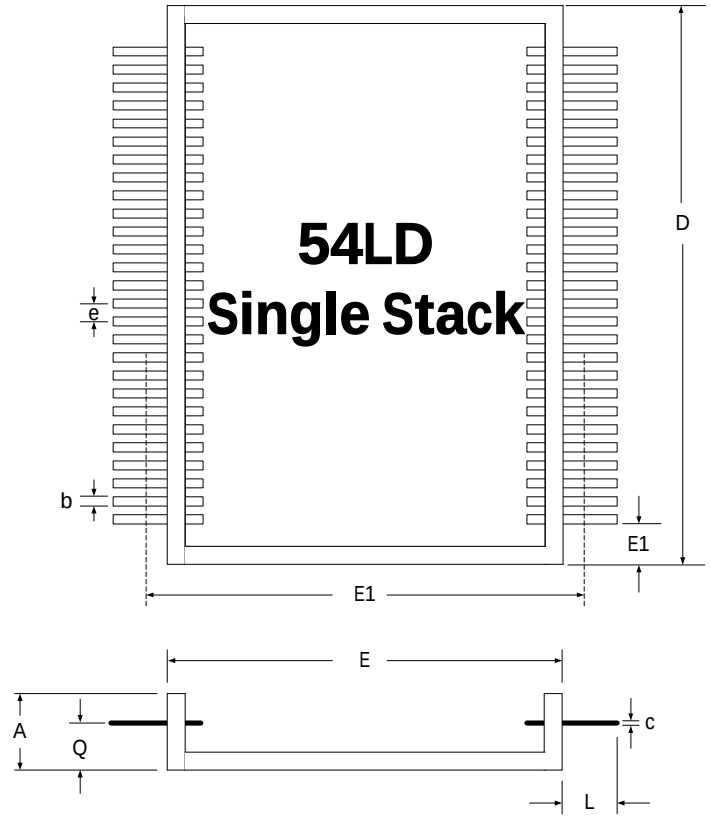
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the assoiated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2).



54-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.363	0.370	0.377
b	0.010	0.015	0.020
c	0.005	0.010	0.015
D	--	1.750	2.405
E	1.660	1.750	1.670
E1	--	--	1.865
e	0.050 BSC		
L	0.500	--	--
Q	0.182	0.195	0.208
S1	0.363	0.368	0.373
N	54		

F54-01
Note: All dimensions in inches.



54-PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.363	0.370	0.377
b	0.010	0.015	0.020
c	0.005	0.010	0.015
D	--	1.750	2.405
E	0.900	1.100	1.300
E1	--	--	1.865
e	0.050 BSC		
L	0.500	--	--
Q	0.182	0.195	0.208
S1	0.363	0.368	0.373
N	54		

F54-02
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Space Electronics verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Space Electronics assumes no responsibility for the use of this information.

Space Electronics' products are not authorized for use as critical components in life support devices or systems without express written approval from Space Electronics.

Any claim against Space Electronics Inc. must be made within 90 days from the date of shipment from Space Electronics. Space Electronics' liability shall be limited to replacement of defective parts.