## 900/H2 Series Product Line of 32-Bit Microcontrollers with Internal ROM

Seamless core 900 Family

Toshiba is now offering the **TMP94CS40AF** product line — internal ROM versions of the 32-bit **900/H2** Series from the **900**-Family. Thanks to its seamless core line, Toshiba provides strong support for customers developing more advanced systems.

Features

- Original high-speed 32-bit CPU core
- Full instruction code compatibility with 16-bit **900**-Series microcontrollers
- High-speed instruction execution (basic instructions: one clock cycle)
- Internal data bus: 32 bits, external data bus: 8/16/32 bits
- Operating frequency: 20 MHz (basic instructions: 50 ns)
  Operating frequency: 24 MHz (under development)
- High-speed data transfer function (micro DMA: 5 clock cycles (min)/8 channels)
- 64-KB internal ROM (**TMP94CS40AF**)
- Connectable directly to memory (DRAM controller/2 channels)
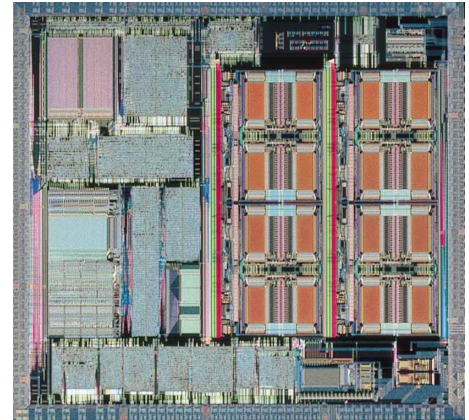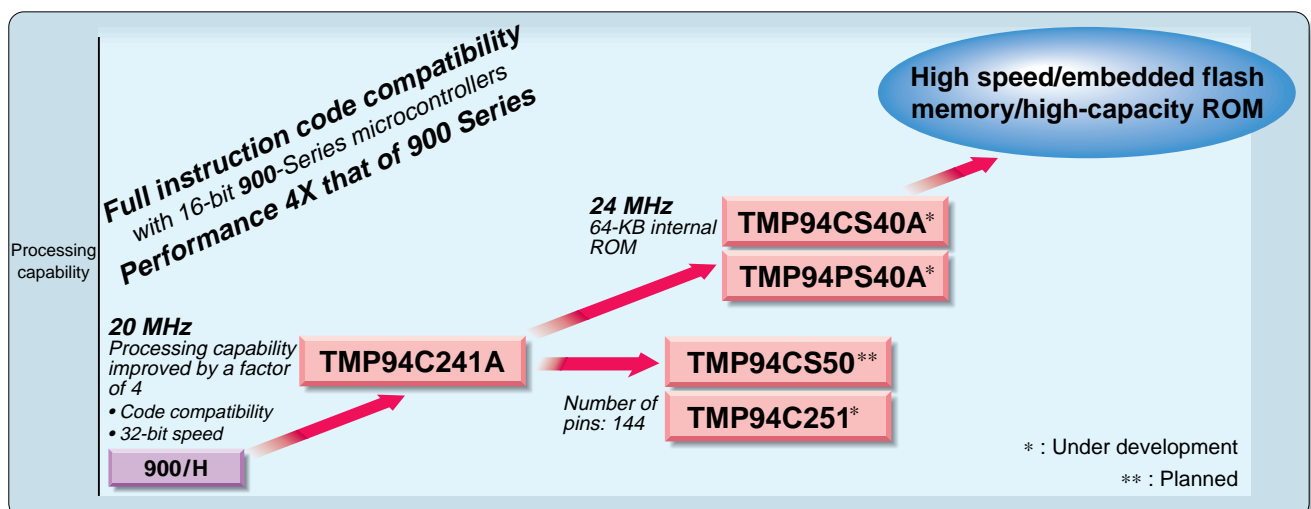
Product List

Product name	Function	Embedded ROM (bytes)	Embedded RAM (bytes)	I/O Port	Minimum Instruction Execution Time	Operating Temperature (°C)	Package	Features
★ **TMP94C241AF**	Timer counters: 16 bits X 4	—	2K	64	50 ns	−20 to 70	QFP160	DA converter: 8 bits X 2 channels
* **TMP94CS40AF**	Timers: 8 bits X 4 Serial interface: 2 channels	64 K			50 ns (20 MHz) 41.6 ns (24 MHz)			24 MHz operation
* **TMP94PS40AF**	DRAM controller: 2 channels	64 K (OTP)						
* **TMP94C251F**	AD converter: 10 bits X 8 channels Watchdog timer	—			50 ns		QFP144	DA converter: 8 bits X 2 channels
** **TMP94CS50F**	CS/WAIT controller	64 K						

★ : Sample under shipment   ∗ : Under development   ∗∗ : Planned
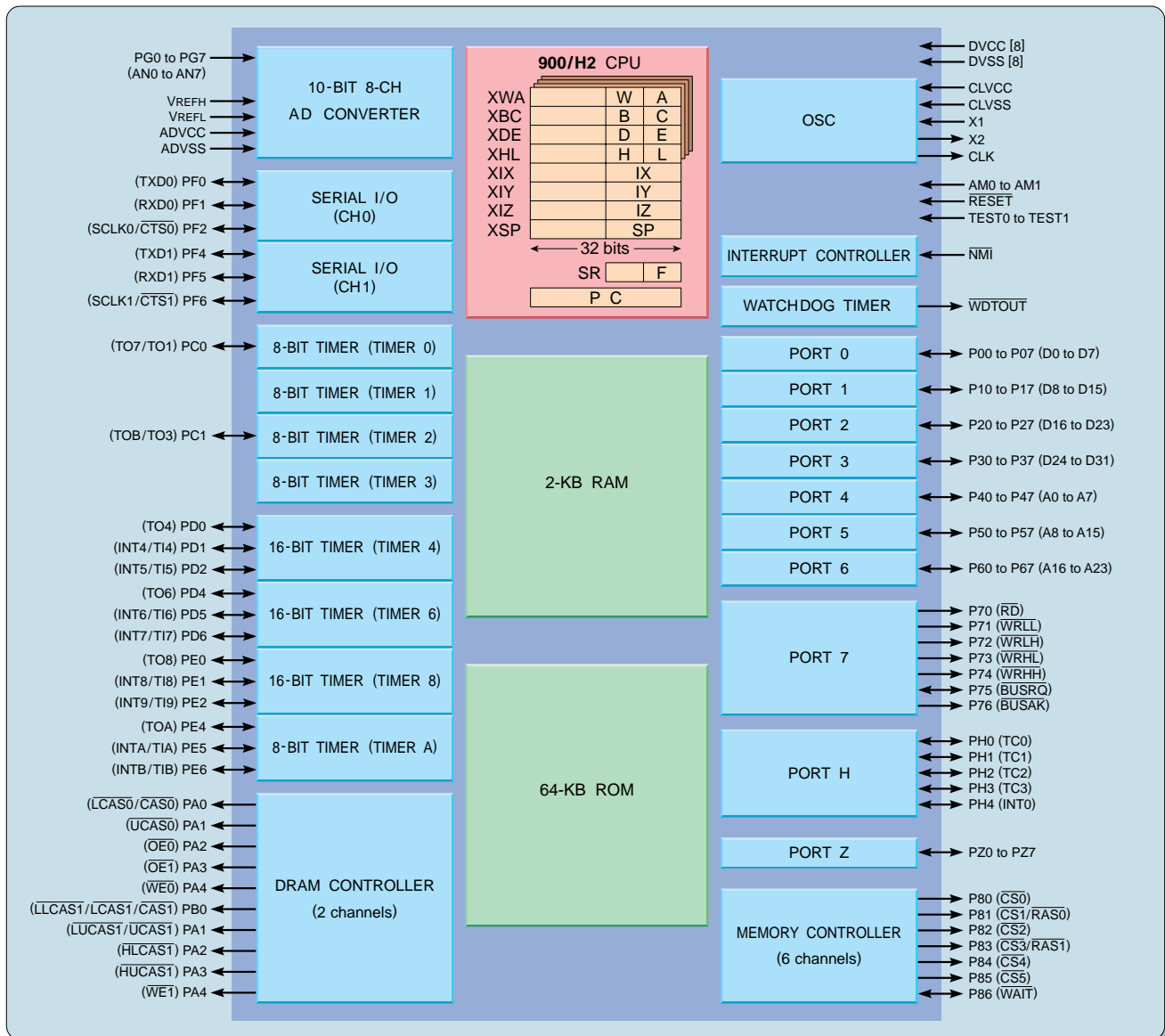
900 Series: Seamless High-Performance Upgrade

Package and ROM product lines provide a timely response to customer needs

900/H2 Product Road Map

TMP94CS40AF Block Diagram

Block Diagram labels:

- PG0 to PG7 (AN0 to AN7) → 10-BIT 8-CH AD CONVERTER
- VREFH, VREFL, ADVCC, ADVSS → AD CONVERTER
- (TXD0) PF0, (RXD0) PF1, (SCLK0/CTS0) PF2 → SERIAL I/O (CH0)
- (TXD1) PF4, (RXD1) PF5, (SCLK1/CTS1) PF6 → SERIAL I/O (CH1)
- (TO7/TO1) PC0 → 8-BIT TIMER (TIMER 0), 8-BIT TIMER (TIMER 1)
- (TOB/TO3) PC1 → 8-BIT TIMER (TIMER 2), 8-BIT TIMER (TIMER 3)
- (TO4) PD0, (INT4/TI4) PD1, (INT5/TI5) PD2 → 16-BIT TIMER (TIMER 4)
- (TO6) PD4, (INT6/TI6) PD5, (INT7/TI7) PD6 → 16-BIT TIMER (TIMER 6)
- (TO8) PE0, (INT8/TI8) PE1, (INT9/TI9) PE2 → 16-BIT TIMER (TIMER 8)
- (TOA) PE4, (INTA/TIA) PE5, (INTB/TIB) PE6 → 8-BIT TIMER (TIMER A)
- (LCAS0/CAS0) PA0, (UCAS0) PA1, (OE0) PA2, (OE1) PA3, (WE0) PA4, (LLCAS1/LCAS1/CAS1) PB0, (LUCAS1/UCAS1) PA1, (HLCAS1) PA2, (HUCAS1) PA3, (WE1) PA4 → DRAM CONTROLLER (2 channels)

CPU block: 900/H2 CPU
- XWA: W | A
- XBC: B | C
- XDE: D | E
- XHL: H | L
- XIX: IX
- XIY: IY
- XIZ: IZ
- XSP: SP
- ← 32 bits →
- SR | F
- P C

Center blocks: 2-KB RAM, 64-KB ROM

Right side:
- DVCC [8], DVSS [8], CLVCC, CLVSS, X1, X2, CLK → OSC
- AM0 to AM1, RESET, TEST0 to TEST1
- NMI → INTERRUPT CONTROLLER
- SR | F
- WATCHDOG TIMER → WDTOUT
- PORT 0 → P00 to P07 (D0 to D7)
- PORT 1 → P10 to P17 (D8 to D15)
- PORT 2 → P20 to P27 (D16 to D23)
- PORT 3 → P30 to P37 (D24 to D31)
- PORT 4 → P40 to P47 (A0 to A7)
- PORT 5 → P50 to P57 (A8 to A15)
- PORT 6 → P60 to P67 (A16 to A23)
- PORT 7 → P70 (RD), P71 (WRLL), P72 (WRLH), P73 (WRHL), P74 (WRHH), P75 (BUSRQ), P76 (BUSAK)
- PORT H → PH0 (TC0), PH1 (TC1), PH2 (TC2), PH3 (TC3), PH4 (INT0)
- PORT Z → PZ0 to PZ7
- MEMORY CONTROLLER (6 channels) → P80 (CS0), P81 (CS1/RAS0), P82 (CS2), P83 (CS3/RAS1), P84 (CS4), P85 (CS5), P86 (WAIT)
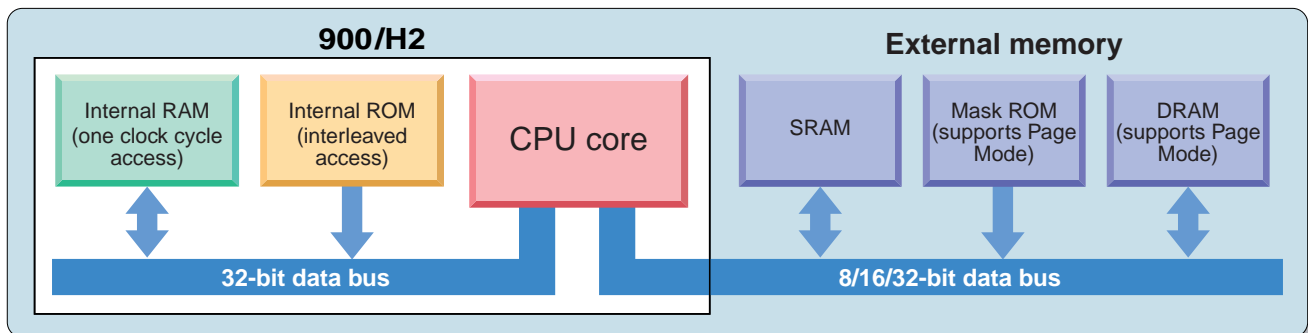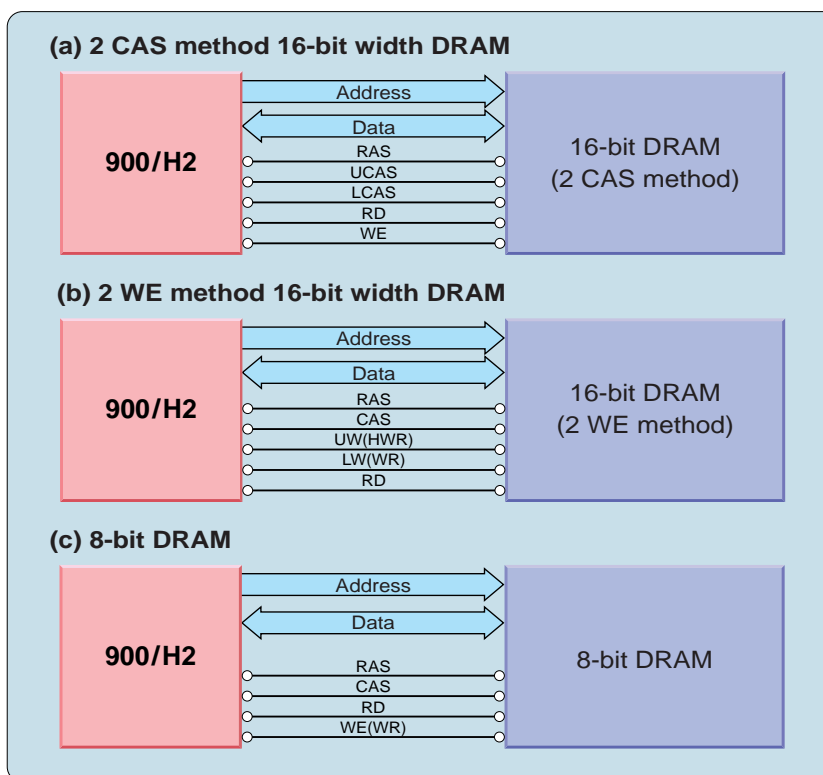
TMP94CS40AF Specifications

- ● Original high-speed 32-bit CPU core (**900/H2** CPU)
  - ■ Full instruction code compatibility with **TLCS-900**, **TLCS-900/L** and **TLCS-900/H** Series
  - ■ 16-MB linear address space
  - ■ General-purpose registers and register banks
  - ■ Internal data bus width: 32 bits
  - ■ Micro DMA: 8 channels
- ● Minimum instruction execution time: 50 ns (20 MHz)
- ● Internal ROM: 64 KB <**TMP94CS40A**>
  (Internal PROM: 64 KB <**TMP94PS40A**>)
  Internal RAM: 2 KB (32 bits, one clock cycle access)
- ● External memory expansion
  - ■ Expandable to 16 MB (shared program/data)
  - ■ External 8/16/32-bit data bus connectable simultaneously to 8-, 16- and 32-bit devices
  - ■ External start-up data bus width select pin (8/16/32-bit bus selectable)

- ● Memory controller
  - ■ Chip Select/WAIT/bus width control: 6 blocks
- ● DRAM controller: 2 channels
  - ■ Direct interface: 8/16/32-bit data bus
  - ■ High-speed page mode supported
- ● 8-bit timer: 4 channels
- ● 16-bit timer: 4 channels
- ● Serial interface: 2 channels
- ● 10-bit AD converter: 8 channels
- ● Watchdog timer
- ● Interrupt function
  Internal I/O: 18
  External pins: 10
- ● 5 V/20 MHz (10 MHz input externally)
- ● 160-pin mini-flat package

3

Maximizes Performance of a Wide Range of Memory Devices

The **900/H2** Series can be directly connected to a wide range of external memory devices without the need for external circuits. The internal memory is connected via a 32-bit data bus. Internal RAM can be accessed in one clock cycle.

900/H2

| Internal RAM (one clock cycle access) | Internal ROM (interleaved access) | CPU core |

32-bit data bus

External memory

| SRAM | Mask ROM (supports Page Mode) | DRAM (supports Page Mode) |

8/16/32-bit data bus

Improved DRAM Control Function

(a) 2 CAS method 16-bit width DRAM

900/H2 — Address, Data, RAS, UCAS, LCAS, RD, WE — 16-bit DRAM (2 CAS method)

(b) 2 WE method 16-bit width DRAM

900/H2 — Address, Data, RAS, CAS, UW(HWR), LW(WR), RD — 16-bit DRAM (2 WE method)

(c) 8-bit DRAM

900/H2 — Address, Data, RAS, CAS, RD, WE(WR) — 8-bit DRAM

- Direct connection to a wide range of DRAM devices is possible.

- Because the CPU and the memory refresh are asynchronous, access to non-DRAM memory devices does not degrade performance.

Enhanced High-Speed Data Transfer Function (micro DMA)

The **900/H2** Series incorporates high-speed data transfer — as performed by a DMAC (direct memory access controller) — as a standard function.
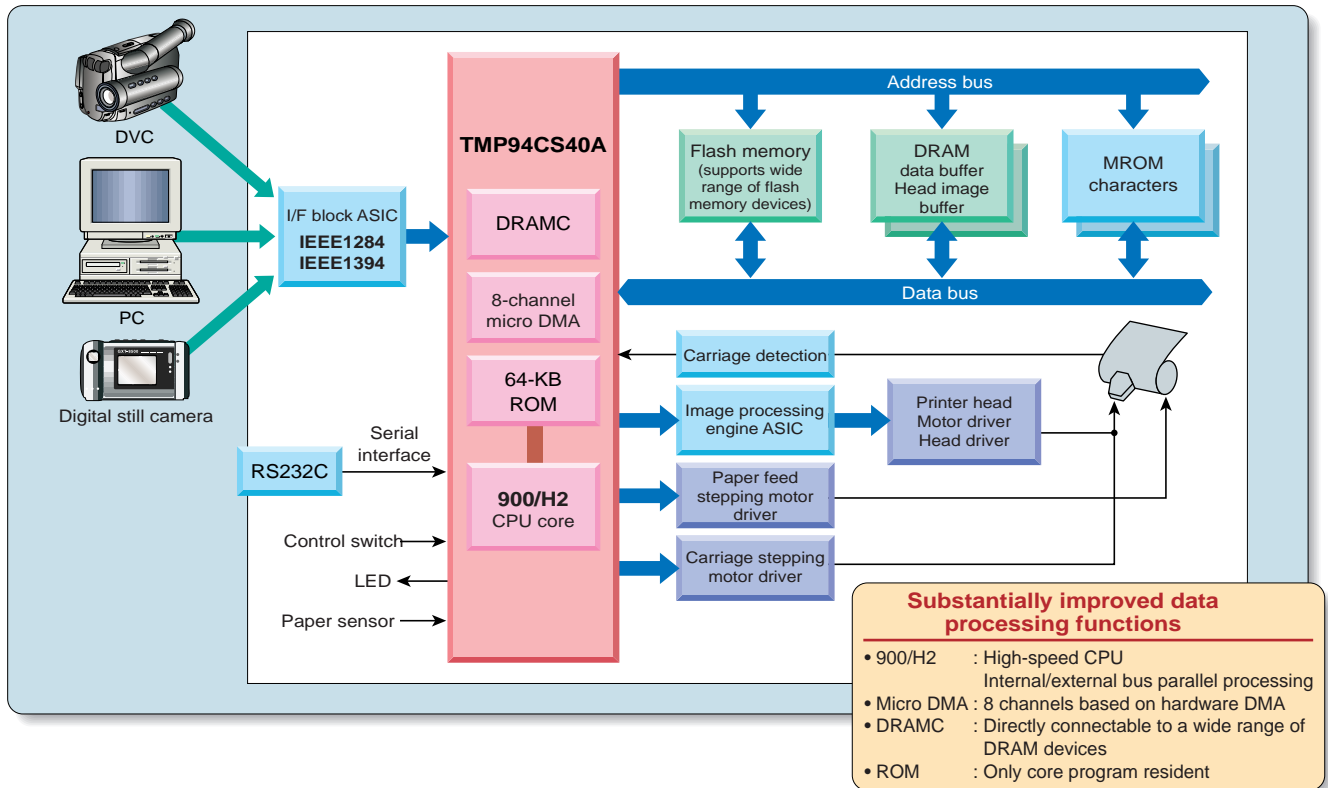
Function and Performance Comparison

Parameter	900, 900/L Series	900/H, 900/L1 Series	900/H2 Series
Number of channels	4 channels	4 channels	8 channels
Minimum transfer time	1600 ns/2 bytes	640 ns/2 bytes	250 ns/4 bytes
Start-up sources	Interrupt	Interrupt and software trigger	Interrupt and software trigger
Burst Mode	No	No	Yes
Transfer modes	I/O → memory, Memory → I/O	I/O → memory, Memory → I/O	I/O → memory, Memory → I/O, Memory → memory

4

Application example for printer

The following depicts a system for the efficient processing of data received via a high-speed communications interface; in this case, a system to print the output from multimedia equipment directly.
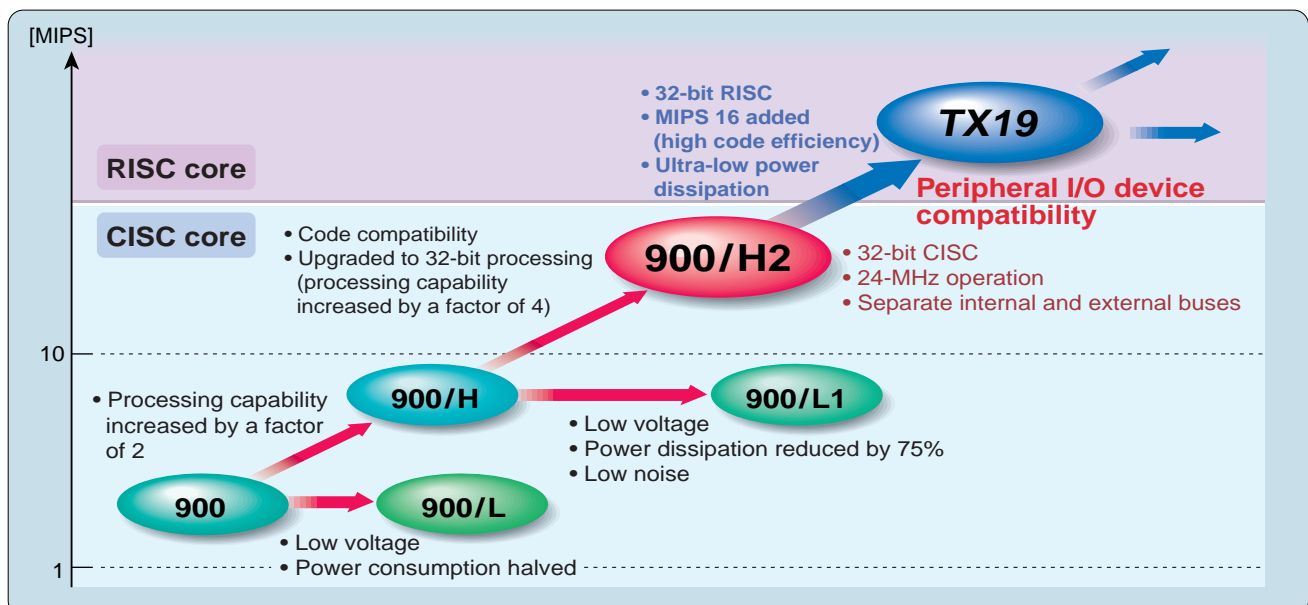
DVC

PC

Digital still camera

RS232C

Serial interface

Control switch

LED

Paper sensor

I/F block ASIC
IEEE1284
IEEE1394

TMP94CS40A
- DRAMC
- 8-channel micro DMA
- 64-KB ROM
- **900/H2** CPU core

Address bus

| Flash memory (supports wide range of flash memory devices) | DRAM data buffer Head image buffer | MROM characters |

Data bus

Carriage detection

Image processing engine ASIC

Printer head Motor driver Head driver

Paper feed stepping motor driver

Carriage stepping motor driver

Substantially improved data processing functions
- 900/H2 : High-speed CPU Internal/external bus parallel processing
- Micro DMA : 8 channels based on hardware DMA
- DRAMC : Directly connectable to a wide range of DRAM devices
- ROM : Only core program resident

Designed to Allow Smooth Migration to the TX Series

TX System RISC

The numerous peripheral I/O devices that have been proven to work with the **900** Family are also compatible with the **TX System RISC** family. Toshiba's solutions for more advanced system performance make effective use of existing resources.

Toshiba Microcontroller Road Map

[MIPS]

RISC core

CISC core

- 32-bit RISC
- MIPS 16 added (high code efficiency)
- Ultra-low power dissipation

TX19

Peripheral I/O device compatibility

- Code compatibility
- Upgraded to 32-bit processing (processing capability increased by a factor of 4)

900/H2

- 32-bit CISC
- 24-MHz operation
- Separate internal and external buses

10

- Processing capability increased by a factor of 2

900/H

900/L1

- Low voltage
- Power dissipation reduced by 75%
- Low noise

900

900/L

- Low voltage
- Power consumption halved

1

900-Series CPU Core Enhances Performance of Advanced Embedded Systems

Conditions required for embedded application IP

1. Compact core

● **Custom instructions written specially for embedded applications, optimized circuit structure**
● **Totally original architecture designed for efficient use of C language code**
  ➡ Substantial improvement in C language code generation efficiency (code size can be as small as 1.2× equivalent assembly code)
  ➡ Significant improvement in program efficiency (especially for programs larger than 64 KB)

2. Real-time response

● **Multi-bank system**
  ➡ Substantial improvement in interrupt response speed allows system to operate at maximum efficiency.
  ➡ Amount of program code can also be reduced.
● **High-speed data transfer function (micro DMA)**
  ➡ Supports high-speed data transfer (equivalent to hardware DMA) as a standard function.
  ➡ **900/H2** core has eight channels.

3. Line of products supporting advanced user systems

● **Seamless core product line**
  ➡ 16-bit core family and 32-bit core **900/H2** offer full instruction code compatibility.
  ➡ Common development environment for 16/32-bit systems enables development system to respond swiftly to market changes.
● **Fully developed memory support**
  ➡ DRAMC can respond flexibly to system demands and memory market trends.

CPU Core Performance

<Instruction Execution Time Comparison> Unit: ns

Instruction	Operand Size		
	8 bits	16 bits	32 bits
• Data transfer 1 LD reg, reg	160 ←Current products 50 ←900/H2 series	160 ←Current products 50 ←900/H2 series	160 ←Current products 50 ←900/H2 series
• Data transfer 2 LD reg, mem	320 100	320 100	480 100
• Arithmetic operation ADD reg, imm	240 50	320 50	480 50
• Bit processing SET imm, reg	240 50	240 50	
• Jump JR disp8	400 100		

Multifunction Multi-Window Debugger Revolutionizes Development Environments

● Operates with Windows®95 and Windows NT®4.0. Debugging environment is completely new.
● Advanced operation offers real-time response, avoiding interruptions in program development.
● Profile function simplifies complex environment settings.
● Fully developed on-line help function allows effective use of the wide range of functions.

∗ Windows® and Windows NT® are registered trademarks of Microsoft Corporation.
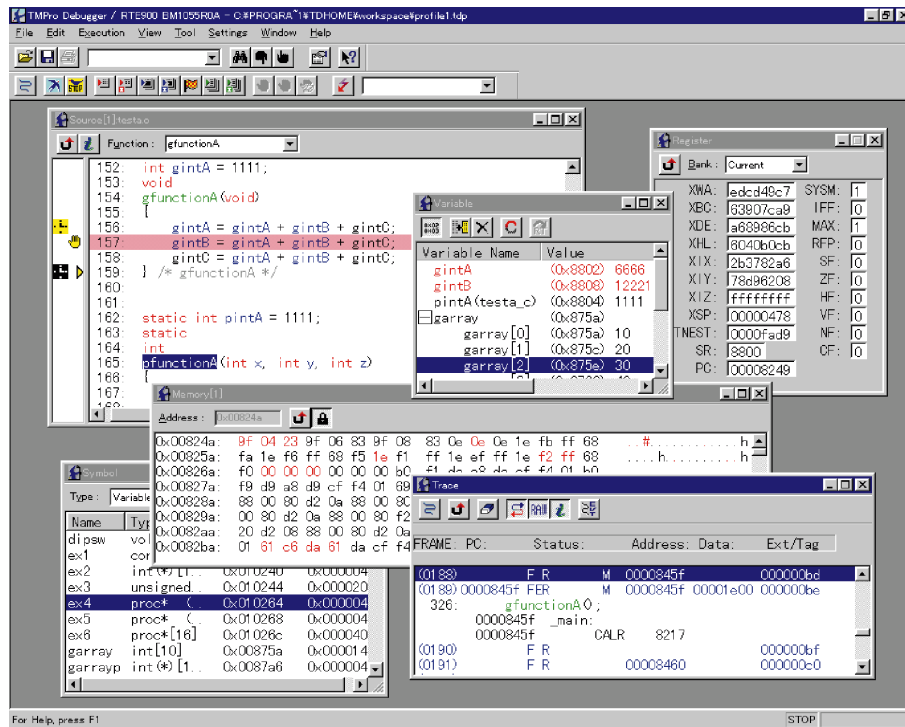
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