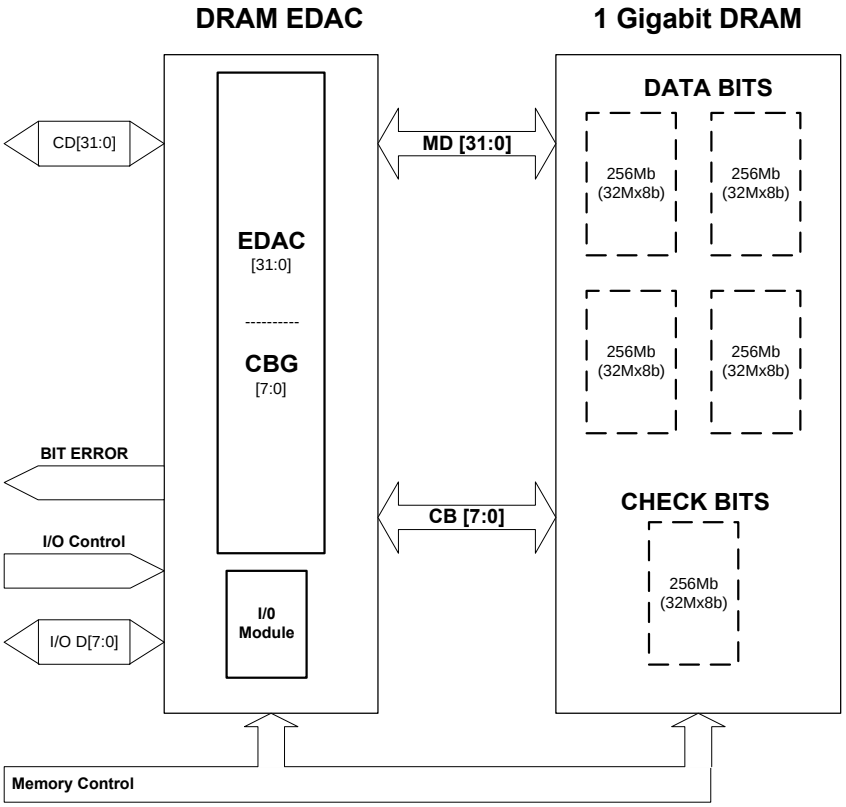
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

1 GIGABIT ERROR CORRECTED DRAM

98C100032DRP



FEATURES:

- 1 Gigabit available DRAM (five 256 Mb DRAM stacks, four data, one checkbit)
- 32 bits wide, built in EDAC
- RAD-PAK® radiation-hardened against natural space radiation
- Total dose hardness: 100 krad (Si) typical; dependent upon orbit
- Single event effect
  - SEL_{TH}: No latchup > 117 MeV/mg/cm^2
  - SEU: IE $^{-10}$ errors/device - day with memory scrubbing
  - Single bit error detection/correction
  - Double bit error detection
- Package:
  - 196 Pin RAD-PAK® quad flat package
- Access time: 90, 120 ns
- Common Data Inputs and Outputs
- EDO or Fast Page Mode capability
- 4096 Cycles / 64ms Refresh

DESCRIPTION:

Space Electronics' 98C100032DRP (RP for RAD-PAK®) high-performance 1 Gigabit Multi-Chip Module (MCM) Dynamic Random Access Memory features a typical 100 kilorad (Si) total dose tolerance; dependent upon orbit. The device has a no single event latchup and single event upset error rate of IE-10 errors/device - day. The 98C100032DRP combines plastic TSOP 256 Mb DRAM stacks and SEi's 48D32DRP 32-bit EDAC into a hermetically sealed package. The design is architected using a 32/7 hamming code EDAC, providing 32 data bits and 7 check bits; DRAM stacks are manufactured using 64 Mb DRAM devices, stacked four high to create each 8-bit wide 256 Mb stack. Five 256 Mb stacks are combined into the 98C100032DRP to create a 32-bit wide, 1 Gb usable memory area. The 98C100032DRP is available with packaging and screening up to Class S.

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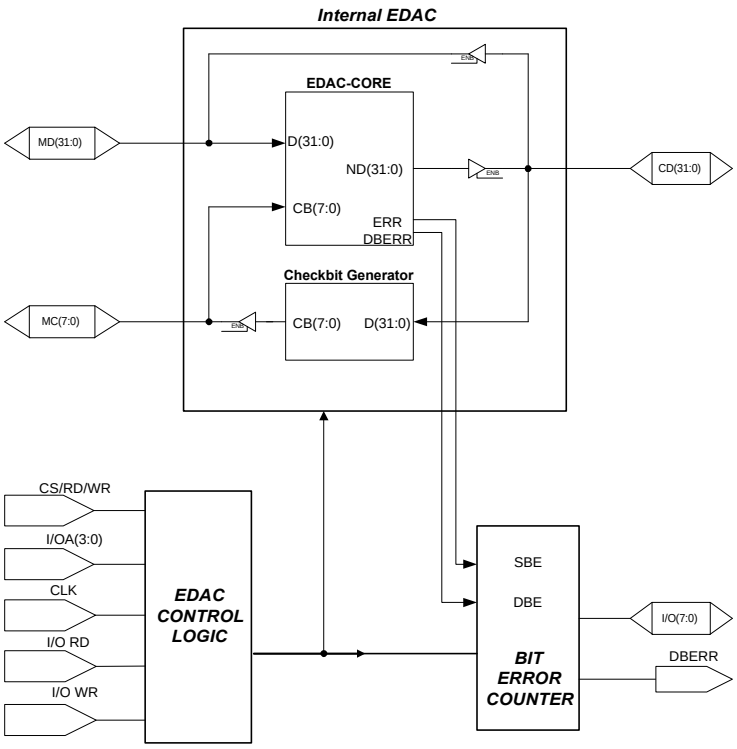
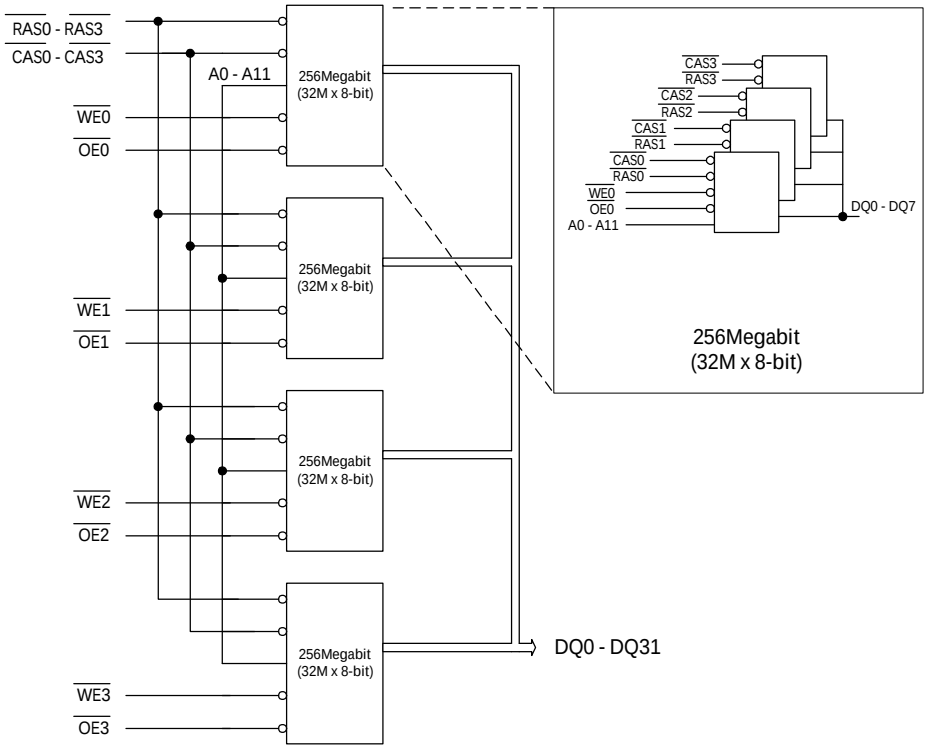


INTERNAL EDAC DESCRIPTION:

The EDAC broken down into two main blocks -- the check bit generator (CBG) and the read/correct data (CORR). The unique flow-thru architecture achieves 90 ns from data in (MD) to corrected data out (CD). Two readable error counters allow single-bit error (ERR) and doubel-bit error (DBERR) tracking. Error signals can be internally marked via two mask bits.

INTERNAL DRAM DESCRIPTION:

The data DRAM uses four 256 Megabit stacks. It has a 32-bit wide data bus that is byte addressable. The component is designed specifically for high-speed, low-power and high-reliability application. The device has $\overline{CAS}$-before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities.



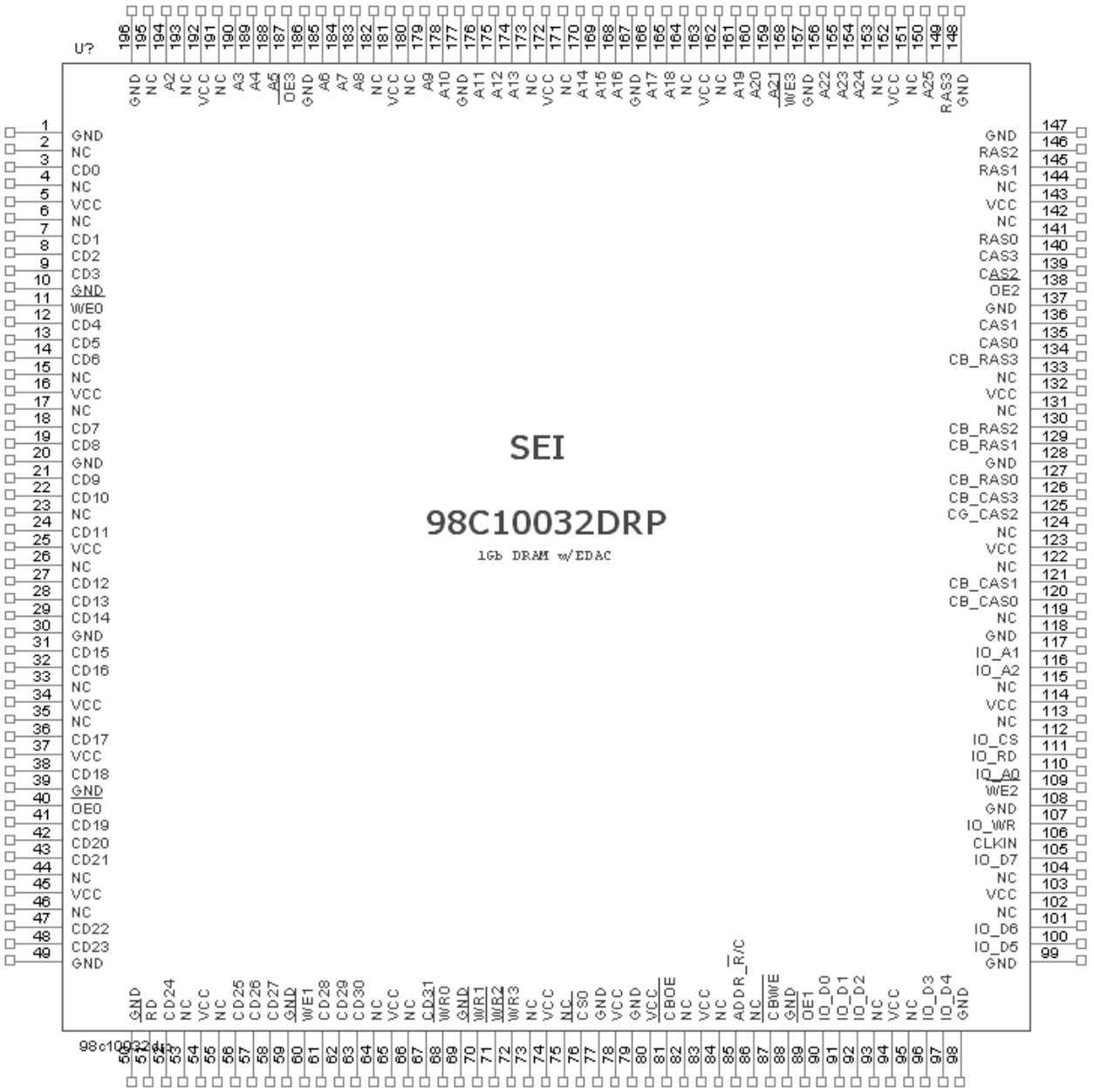


TABLE 1. 98C100032DRP PIN DESCRIPTION

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	GND	50	GND	99	GND	148	GND
2	NC	51	$\overline{RD}$	100	IO_D5	149	RAS3
3	CD0	52	CD24	101	IO_D6	150	A25
4	NC	53	NC	102	NC	151	NC
5	V_{CC}	54	V_{CC}	103	V_{CC}	152	V_{CC}
6	NC	55	NC	104	NC	153	NC
7	CD1	56	CD25	105	IO_D7	154	A24
8	CD2	57	CD26	106	CLKIN	155	A23
9	CD3	58	CD27	107	IO_WR	156	A22
10	GND	59	GND	108	GND	157	GND
11	NC	60	NC	109	NC	158	NC
12	CD4	61	CD28	110	IO_A0	159	A21
13	CD5	62	CD29	111	IO_RD	160	A20
14	CD6	63	CD30	112	IO_CS	161	A19
15	NC	64	NC	113	NC	162	NC
16	V_{CC}	65	V_{CC}	114	V_{CC}	163	V_{CC}
17	NC	66	NC	115	NC	164	NC
18	CD7	67	CD31	116	IO_A2	165	A18
19	CD8	68	$\overline{WR0}$	117	IO_A1	166	A17
20	GND	69	GND	118	GND	167	GND
21	CD9	70	$\overline{WR1}$	119	NC	168	A16
22	CD10	71	$\overline{WR2}$	120	CB_CAS0	169	A15
23	CD11	72	$\overline{WR3}$	121	CB_CAS1	170	A14
24	NC	73	NC	122	NC	171	NC
25	V_{CC}	74	V_{CC}	123	V_{CC}	172	V_{CC}
26	NC	75	NC	125	NC	173	NC
27	CD12	76	$\overline{CS0}$	125	CB_CAS2	174	A13
28	CD13	77	GND	126	CB_CAS3	175	A12
29	CD14	78	V_{CC}	127	CB_RAS0	176	A11
30	GND	79	GND	128	GND	177	GND
31	CD15	80	V_{CC}	129	CB_RAS1	178	A10
32	CD16	81	$\overline{CBOE}$	130	CB_RAS2	179	A9
33	NC	82	NC	131	NC	180	NC
34	V_{CC}	83	V_{CC}	132	V_{CC}	181	V_{CC}
35	NC	84	NC	133	NC	182	NC

TABLE 1. 98C100032DRP PIN DESCRIPTION

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
36	CD17	85	ADDR_R/C	134	CB_RAS3	183	A8
37	V_{CC}	86	NC	135	CAS0	184	A7
38	CD18	87	CB_$\overline{WE}$	136	CAS1	185	A6
39	GND	88	GND	137	GND	186	GND
40	NC	89	NC	138	NC	187	NC
41	CD19	90	IO_D0	139	CAS2	188	A5
42	CD20	91	IO_D1	140	CAS3	189	A4
43	CD21	92	IO_D2	141	RAS0	190	A3
44	NC	93	NC	142	NC	191	NC
45	V_{CC}	94	V_{CC}	143	V_{CC}	192	V_{CC}
46	NC	95	NC	144	NC	193	NC
47	CD22	96	IO_D3	145	RAS1	194	A2
48	CD23	97	IO_D4	146	RAS2	195	NC
49	GND	98	GND	147	GND	196	GND

TABLE 2. 98C100032DRP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	7.0	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5	7.0	V
Operating Temperature	T_A	-40	85	ºC
Storage Temperature	T_{STG}	-55	150	ºC
Output Current (Source/Sink)	I_{OUT}	-20	20	mA

TABLE 3. 98C100032DRP RECOMMENDED OPERATING CONDITIONS

(VOLTAGE REFERENCED TO V_{SS}, T_A = -40 TO 85 ºC UNLESS OTHERWISE SPECIFEID)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	--	V_{DD} +1.0	V
Input Low Voltage	V_{IL}	-1.0	--	0.8	V

TABLE 4. 98C100032DRP CAPACITANCE

(T_A = 25 °C, V_{DO} = 5.0V, f = 1 MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Address Input	C_{ADR}	V_{IN} = 0V	150	pF
$\overline{CAS}$ Input	C_{CAS}		45	pF
$\overline{RAS}$ Input	C_{RAS}		45	pF
Write Enable	C_{WE}		--	pF
Output Enable	C_{OE}		--	pF
Data Input/Output	$C_{I/O}$		20	pF

TABLE 5. 98C100032DRP DC CHARACTERISTICS

(RECOMMENDED OPERATING CONDITIONS UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Leakage Current	I_{IN}	$\overline{WE}$, $\overline{OE}$ $\overline{CAS}$, $\overline{RAS}$	-20 -80	20 80	uA
Output Leakge Current	I_{OUT}	Data out is disabled, 0 V ≤ V_{OUT} < V_{DD}	-20	20	uA
Output High Voltage Level	V_{OH}	I_{OH} = -5mA	2.4	--	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.2mA	--	0.4	V
Operating Current 98C100032DRP-9 98C100032DRP-12	I_{CC1}	$\overline{RAS}$ and $\overline{CAS}$ cycling @ tRC = min	 -- --	 750 700	mA
Standby Current	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{IH}	--	43	mA
$\overline{RAS}$-only Refresh Current 98C100032DRP-9 98C100032DRP-12	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling @ t_{RC} = min	 -- --	 750 700	mA
FAST-PAGE-MODE Current 98C100032DRP-9 98C100032DRP-12	I_{CC4}	 $\overline{RAS}$ = V_{IL} $\overline{CAS}$ address cycling @ t_{RC} = min	 -- --	 400 380	mA
Standby Current	I_{CC5}	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{DD} - 0.2V	--	22	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current 98C100032DRP-9 98C100032DRP-12	I_{CC6}	$\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min	 -- --	 750 700	mA

TABLE 6. 98C100032DRP AC CHARACTERISTICS

(-40 °C ≤ T_A ≤ 80 °C, V_{DD} = 5.0V ± 10%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX
Random read or write cycle time	t_{RC}			ns
98C100032DRP-9		130	--	
98C100032DRP-12		150	--	
Read-modify-write cycle time	t_{RWC}			ns
98C100032DRP-9		175	--	
98C100032DRP-12		205	--	
Access time for $\overline{RAS}$ [1,2,3]	t_{RAC}			ns
98C100032DRP-9		--	90	
98C100032DRP-12		--	120	
Access time for CAS [1,2,4]	t_{CAC}			ns
98C100032DRP-9		--	15	
98C100032DRP-12		--	20	
Access time from column address [1,3]	t_{AA}			ns
98C100032DRP-9		--	30	
98C100032DRP-12		--	34	
$\overline{CAS}$ to output in LOW-Z [1]	t_{CLZ}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Output buffer turn-off delay [5]	t_{OFF}			ns
98C100032DRP-9		0	15	
98C100032DRP-12		0	20	
Transition time (rise and fall) [6,7]	t_T			ns
98C100032DRP-9		3	50	
98C100032DRP-12		3	50	
$\overline{RAS}$ precharge time	t_{RP}			ns
98C100032DRP-9		40	--	
98C100032DRP-12		50	--	
$\overline{RAS}$ pulse width	t_{RAS}			ns
98C100032DRP-9		60	10K	
98C100032DRP-12		70	10K	
$\overline{RAS}$ hold time	t_{RSH}			ns
98C100032DRP-9		15	--	
98C100032DRP-12		20	--	
$\overline{CAS}$ hold time	t_{CSH}			ns
98C100032DRP-9		60	--	
98C100032DRP-12		70	--	
$\overline{CAS}$ pulse width	t_{CAS}			ns
98C100032DRP-9		15	10K	
98C100032DRP-12		20	10K	
$\overline{RAS}$ to $\overline{CAS}$ delay time [2,7]	t_{RCD}			ns
98C100032DRP-9		20	45	
98C100032DRP-12		20	50	

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PARAMETER	SYMBOL	MIN	TYP	MAX
$\overline{RAS}$ to column address delay time [3]	t_{RAD}			ns
98C100032DRP-9		15	30	
98C100032DRP-12		15	35	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}			ns
98C100032DRP-9		5	--	
98C100032DRP-12		5	--	
Row address set-up time	t_{ASR}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Row address hold time	t_{RAH}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		10	--	
Column address set-up time	t_{ASC}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Column address hold time	t_{CAH}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		15	--	
Column address to $\overline{RAS}$ lead time	t_{RAL}			ns
98C100032DRP-9		30	--	
98C100032DRP-12		35	--	
Read command set-up time	t_{RCS}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Read command hold time referenced to $\overline{CAS}$ [8]	t_{RCH}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Read command hold time referenced to $\overline{RAS}$ [8]	t_{RRH}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Write command hold time	t_{WCH}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		15	--	
Write command pulse width	t_{WP}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		15	--	
Write command to $\overline{RAS}$ lead time	t_{RWL}			ns
98C100032DRP-9		15	--	
98C100032DRP-12		20	--	
Write command to $\overline{CAS}$ lead time	t_{CWL}			ns
98C100032DRP-9		15	--	
98C100032DRP-12		20	--	

TABLE 6. 98C100032DRP AC CHARACTERISTICS

(-40 °C ≤ T_A ≤ 80 °C, V_{DD} = 5.0V ± 10%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX
Data set-up time [9]	t_{DS}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
Data hold time [9]	t_{DH}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		15	--	
Refresh Period	t_{REF}			ms
98C100032DRP-9		--	64	
98C100032DRP-12		--	64	
Write command set-up time [10]	t_{WCS}			ns
98C100032DRP-9		0	--	
98C100032DRP-12		0	--	
$\overline{CAS}$ to $\overline{WE}$ delay time [10]	t_{CWD}			ns
98C100032DRP-9		40	--	
98C100032DRP-12		50	--	
$\overline{RAS}$ to $\overline{WE}$ delay time [10]	t_{RWD}			ns
98C100032DRP-9		85	--	
98C100032DRP-12		100	--	
Column address to $\overline{WE}$ delay time [10]	t_{AWD}			ns
98C100032DRP-9		55	--	
98C100032DRP-12		65	--	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPWD}			ns
98C100032DRP-9		60		
98C100032DRP-12		70		
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		10	--	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh) [11]	t_{CHR}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		15	--	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}			ns
98C100032DRP-9		5	--	
98C100032DRP-12		5	--	
Fast Page mode cycle time	t_{PC}			ns
98C100032DRP-9		40	--	
98C100032DRP-12		45	--	
Fast Page mode read-modify-write cycle time	t_{PRWC}			ns
98C100032DRP-9		85	--	
98C100032DRP-12		100	--	
$\overline{CAS}$ precharge time (Fast Page cycle)	t_{CP}			ns
98C100032DRP-9		10	--	
98C100032DRP-12		10	--	

TABLE 6. 98C100032DRP AC CHARACTERISTICS

(-40 °C ≤ T_A ≤ 80 °C, V_{DD} = 5.0V ± 10%, V_{IH}/V_{IL} = 2.0/0.8V, V_{OH}/V_{OL} = 2.0/0.8V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX
$\overline{RAS}$ pulse width (Fast Page cycle) 98C100032DRP-9 98C100032DRP-12	t_{RASP}	 60 70	 200K 200K	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge 98C100032DRP-9 98C100032DRP-12	t_{RHCP}	 35 40	 -- --	ns
$\overline{OE}$ access time 98C100032DRP-9 98C100032DRP-12	t_{OEA}	 -- --	 15 20	ns
$\overline{OE}$ to data delay 98C100032DRP-9 98C100032DRP-12	t_{OED}	 15 20	 -- --	ns
Output to buffer turn off delay time from $\overline{OE}$ [5] 98C100032DRP-9 98C100032DRP-12	t_{OEZ}	 0 0	 15 20	ns
$\overline{OE}$ command hold time 98C100032DRP-9 98C100032DRP-12	t_{OEH}	 15 20	 -- --	ns
$\overline{WE}$ to $\overline{RAS}$ precharge time (C-B-R refresh) 98C100032DRP-9 98C100032DRP-12	t_{WRP}	 10 10	 -- --	ns
$\overline{WE}$ to $\overline{RAS}$ hold time (C-B-R refresh) 98C100032DRP-9 98C100032DRP-12	t_{WRH}	 10 10	 -- --	ns

1. Measured with a load equivalent to 2 TTL load and 100 pF.
2. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
3. Operation within the t_{RAD} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5 ns for all inputs.
7. Guaranteed by design.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-modify-write cycles.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating partners. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycles in an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selection address. If neither of the above conditions is satisfied, the condition of the data out is indeterminable.
11. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if $t_{CHR} \geq t_{RAS}$ or $\overline{CAS}$ < 0.2 V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.

FIGURE 1. READ CYCLE

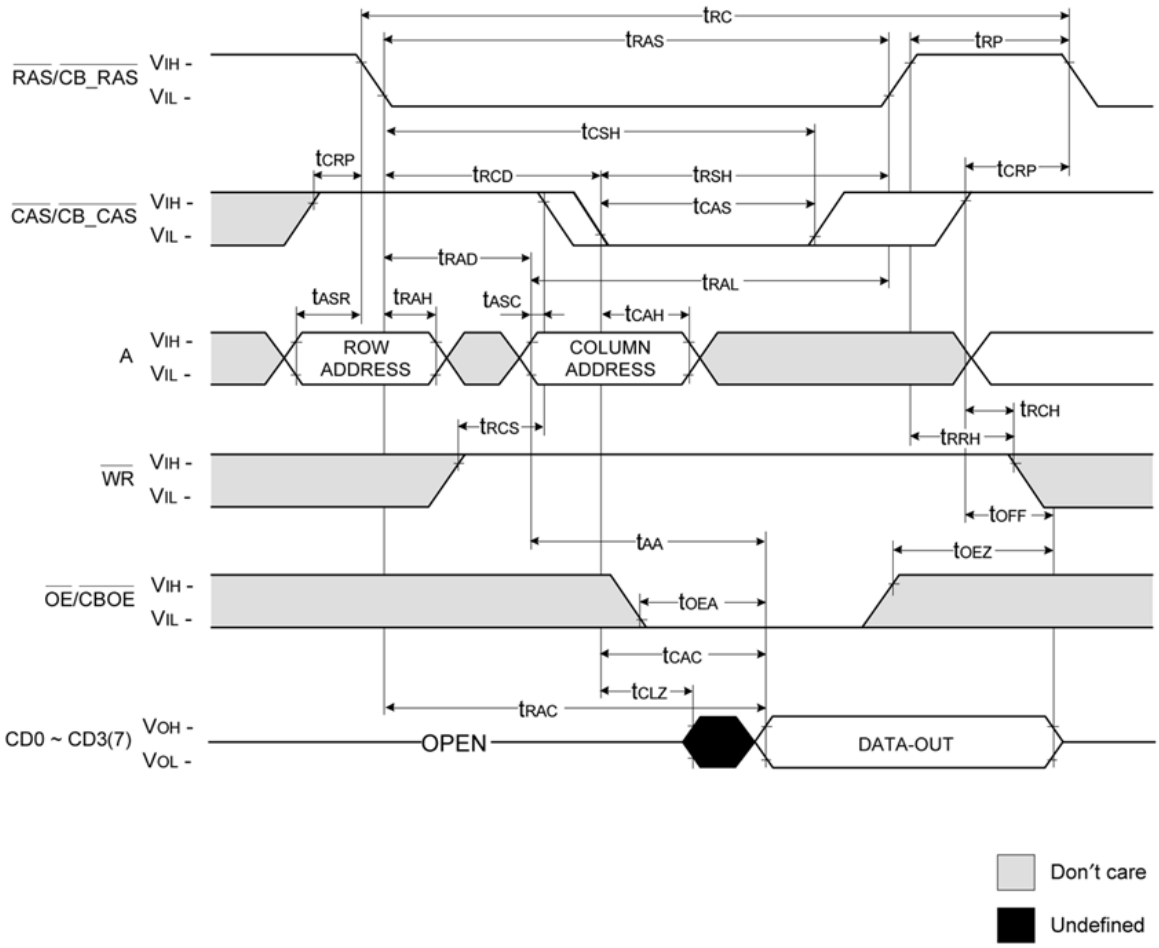


FIGURE 2. WRITE CYCLE (EARLY WRITE)

NOTE: D_{OUT} = OPEN

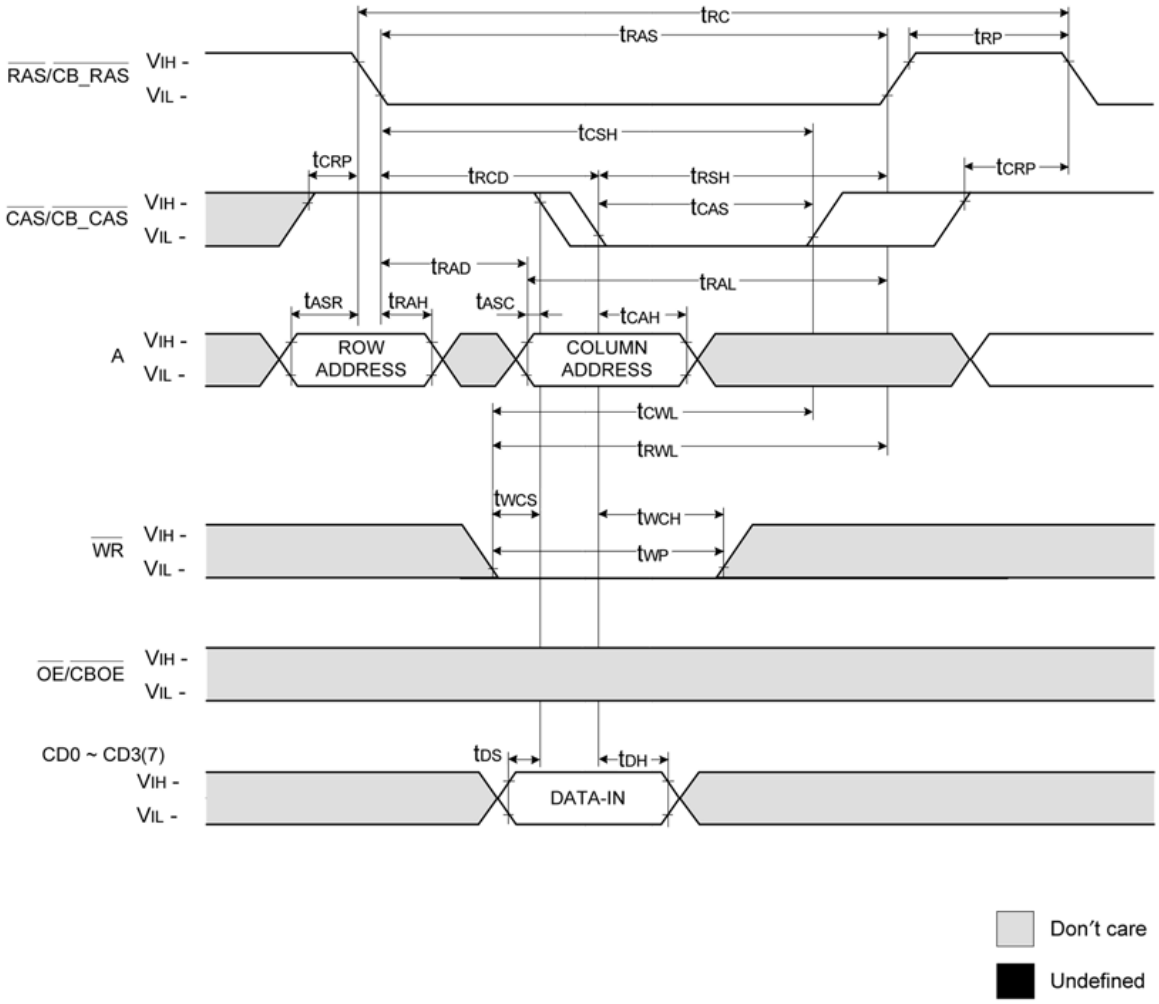


FIGURE 3. WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE: D_{OUT} = OPEN

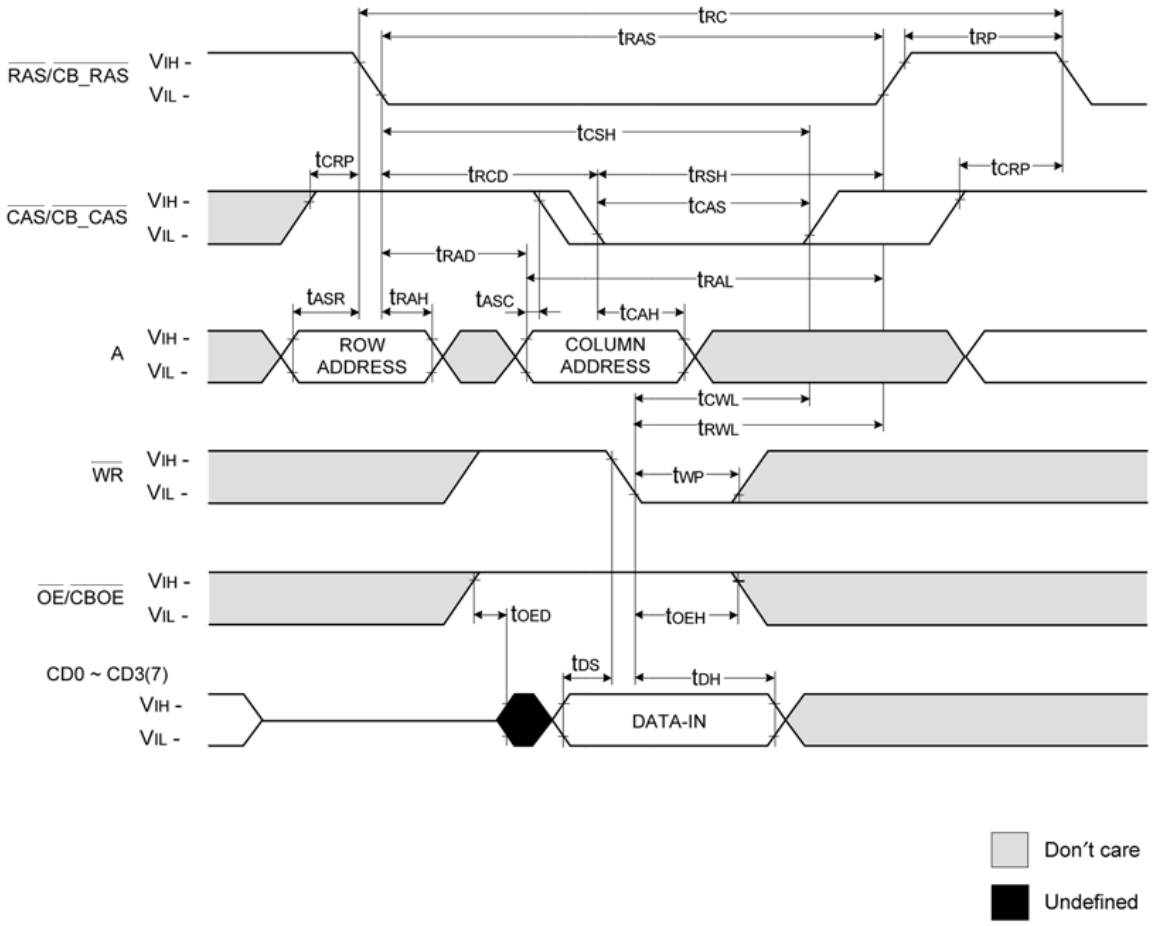


FIGURE 4. READ-MODIFY-WRITE CYCLE

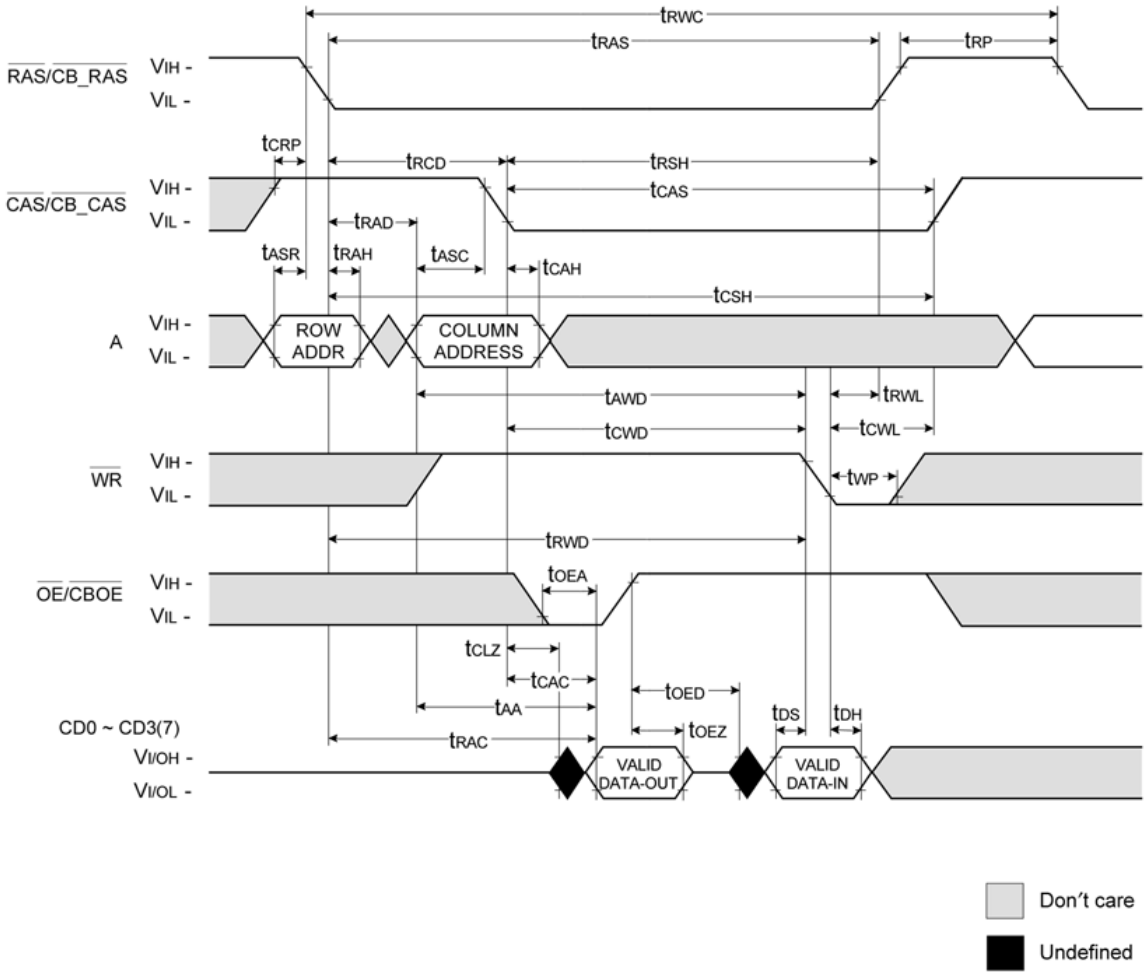


FIGURE 5. FAST PAGE READ CYCLE

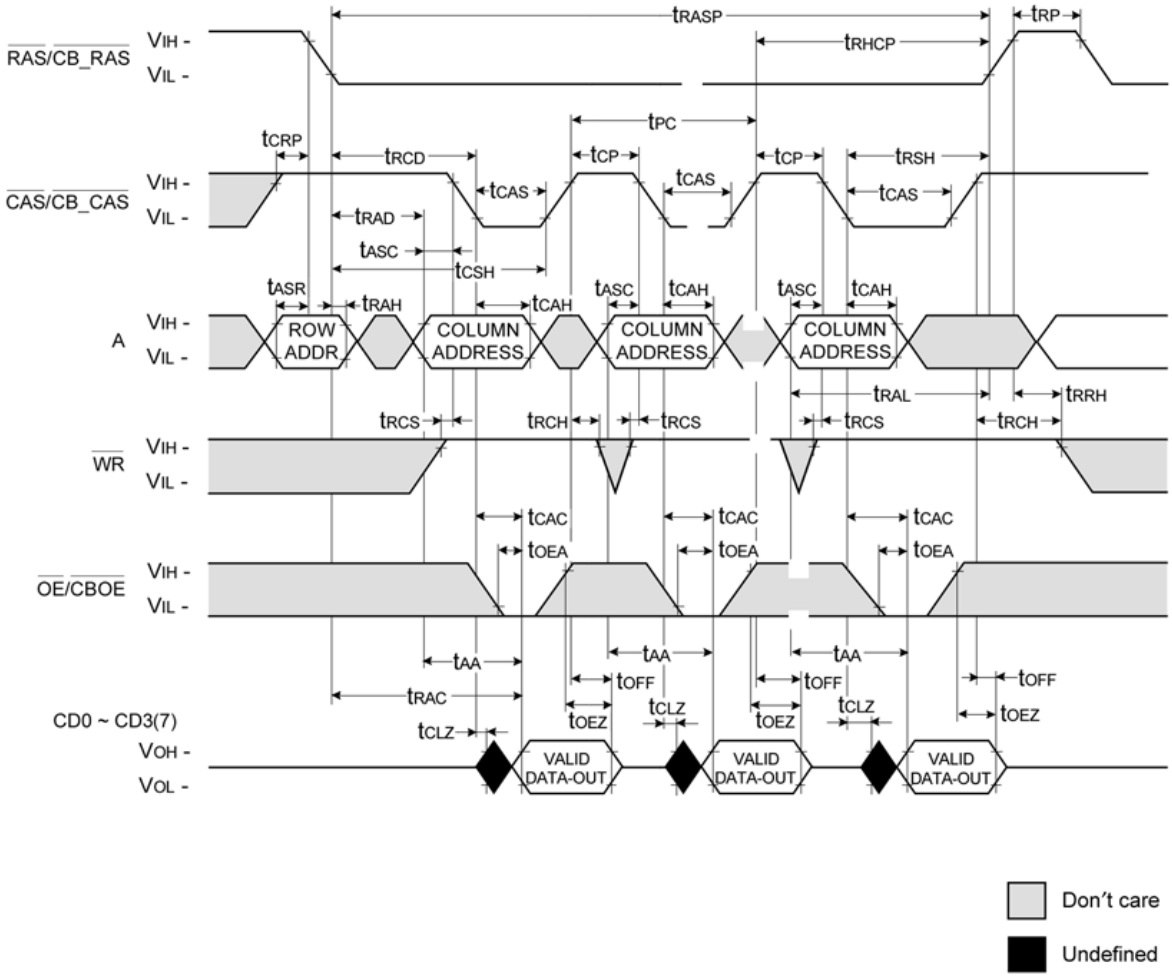


FIGURE 6. FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE: D_{OUT} = OPEN

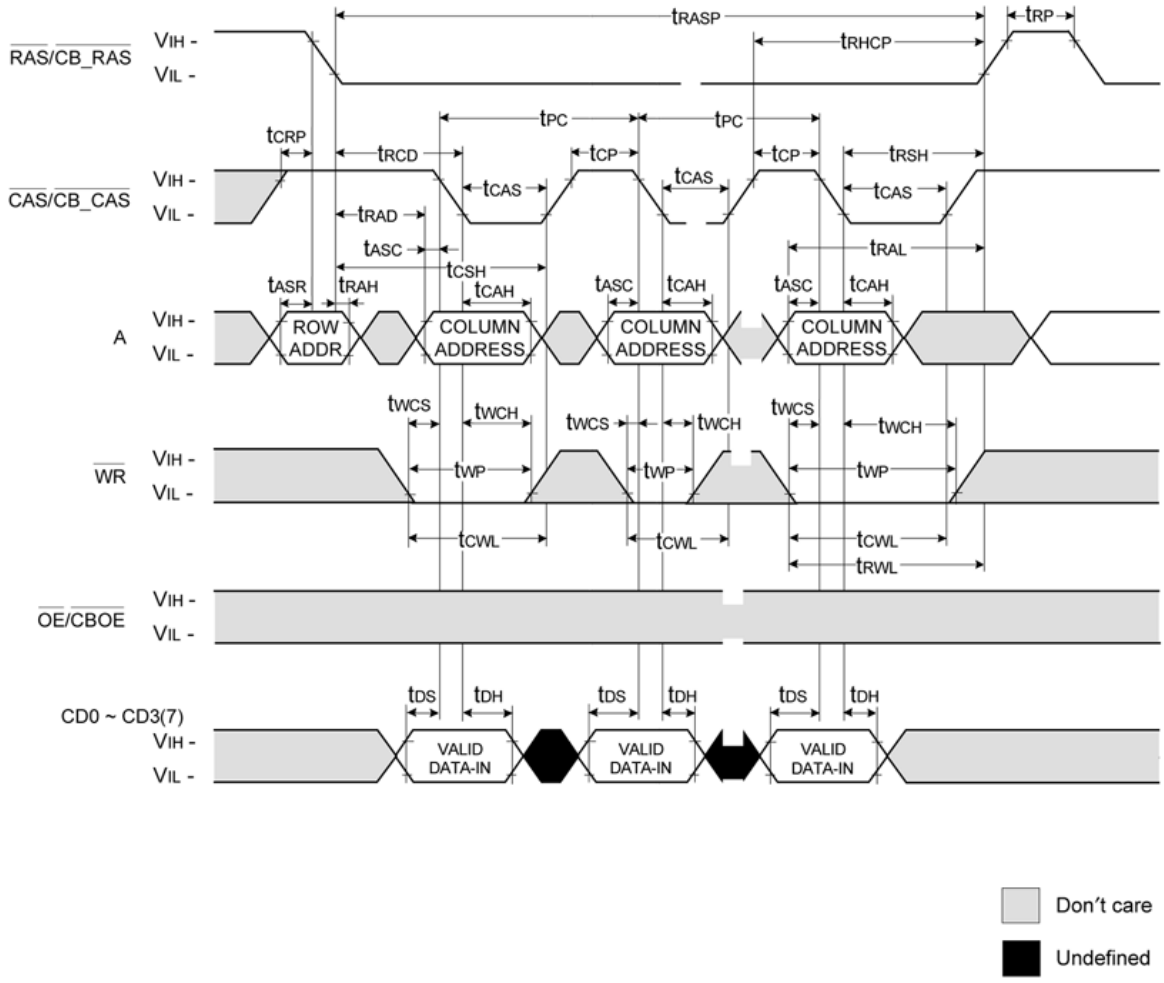


FIGURE 7. FAST PAGE READ-MODIFY-WRITE CYCLE

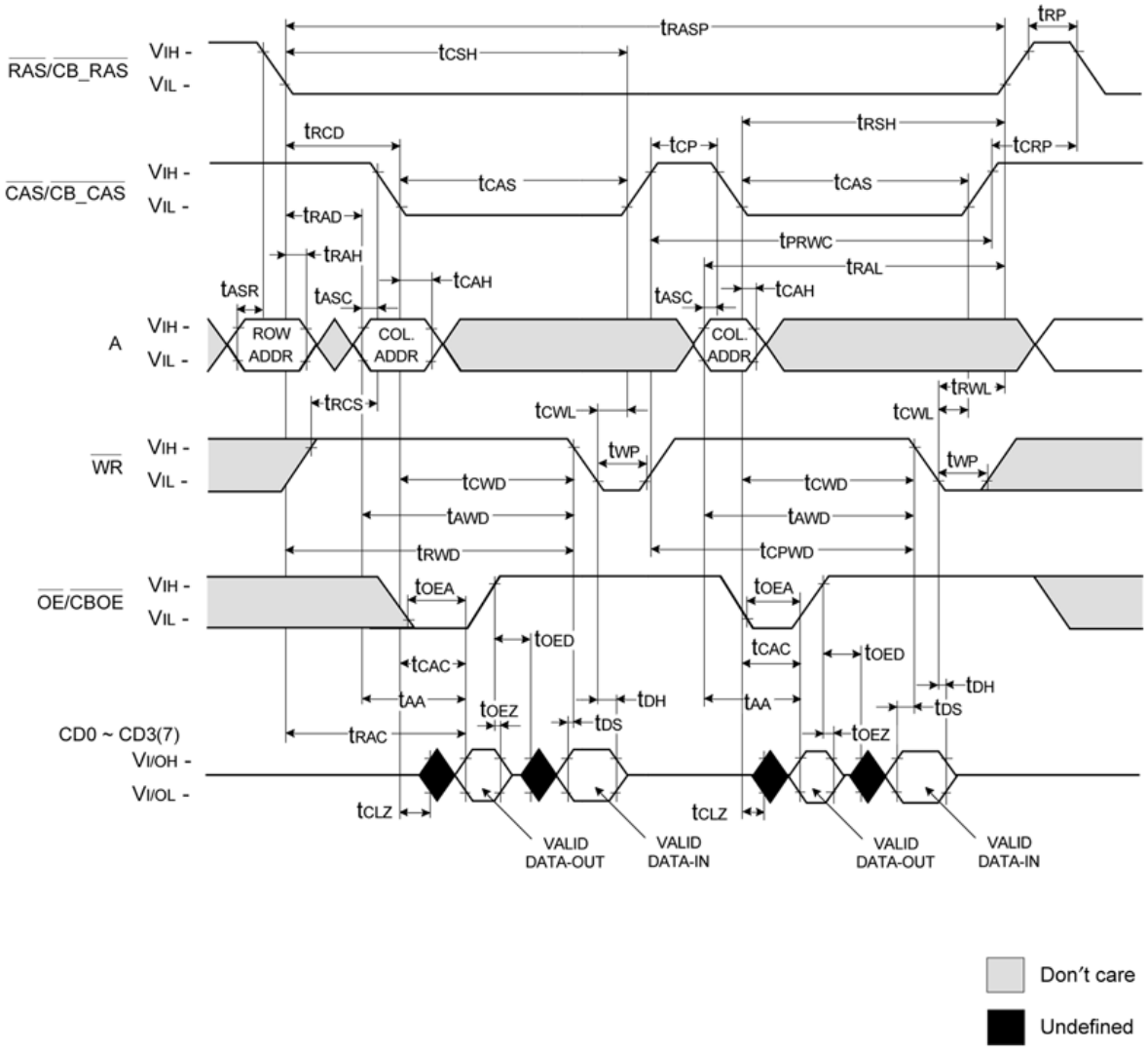


FIGURE 8. $\overline{\text{RAS}}$-ONLY REFRESH CYCLE

NOTE: $\overline{\text{WR}}$, $\overline{\text{OE}}$, D_{IN} = DON'T CARE; D_{OUT} = OPEN

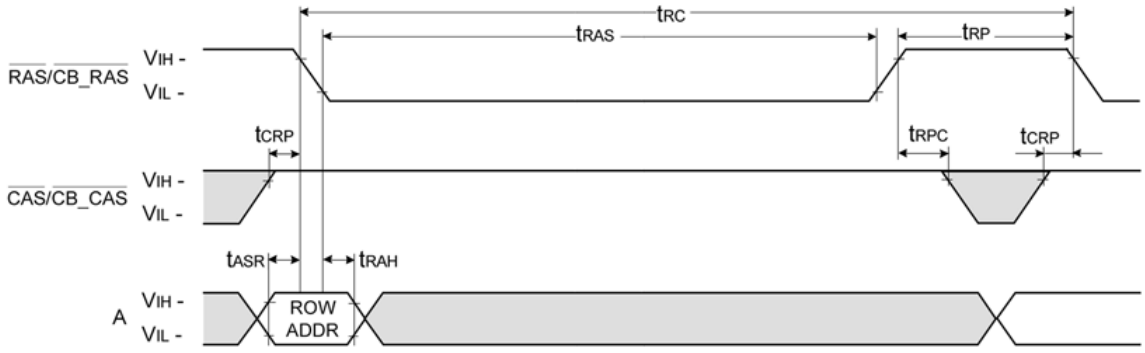


FIGURE 9. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

NOTE: $\overline{\text{OE}}$, A = DON'T CARE

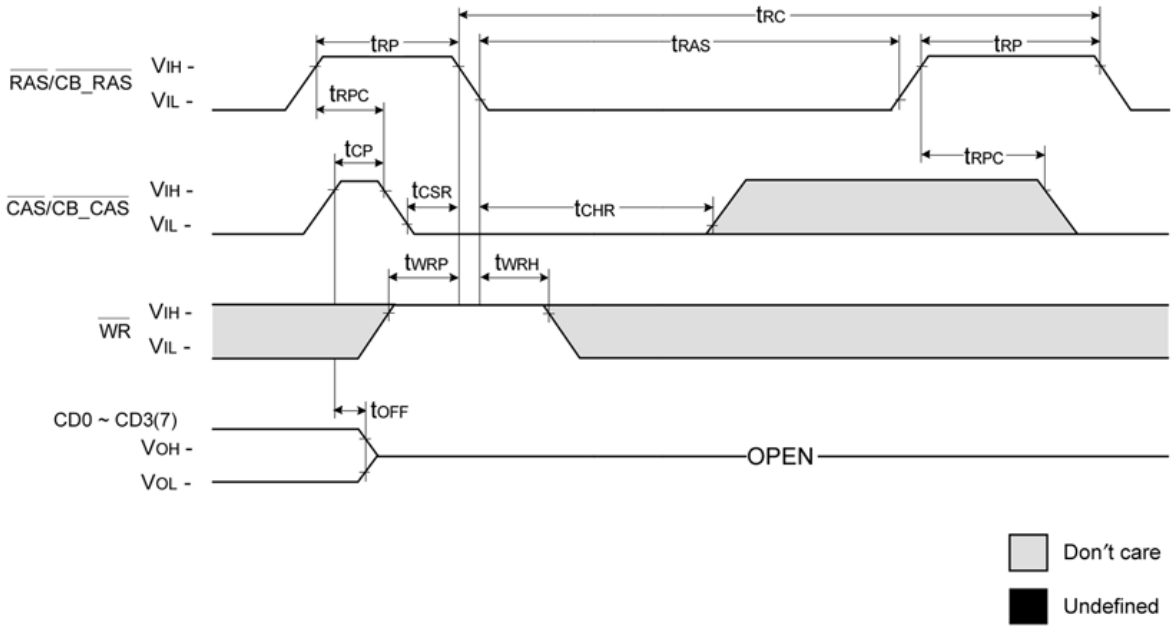


FIGURE 10. HIDDEN REFRESH CYCLE (READ)

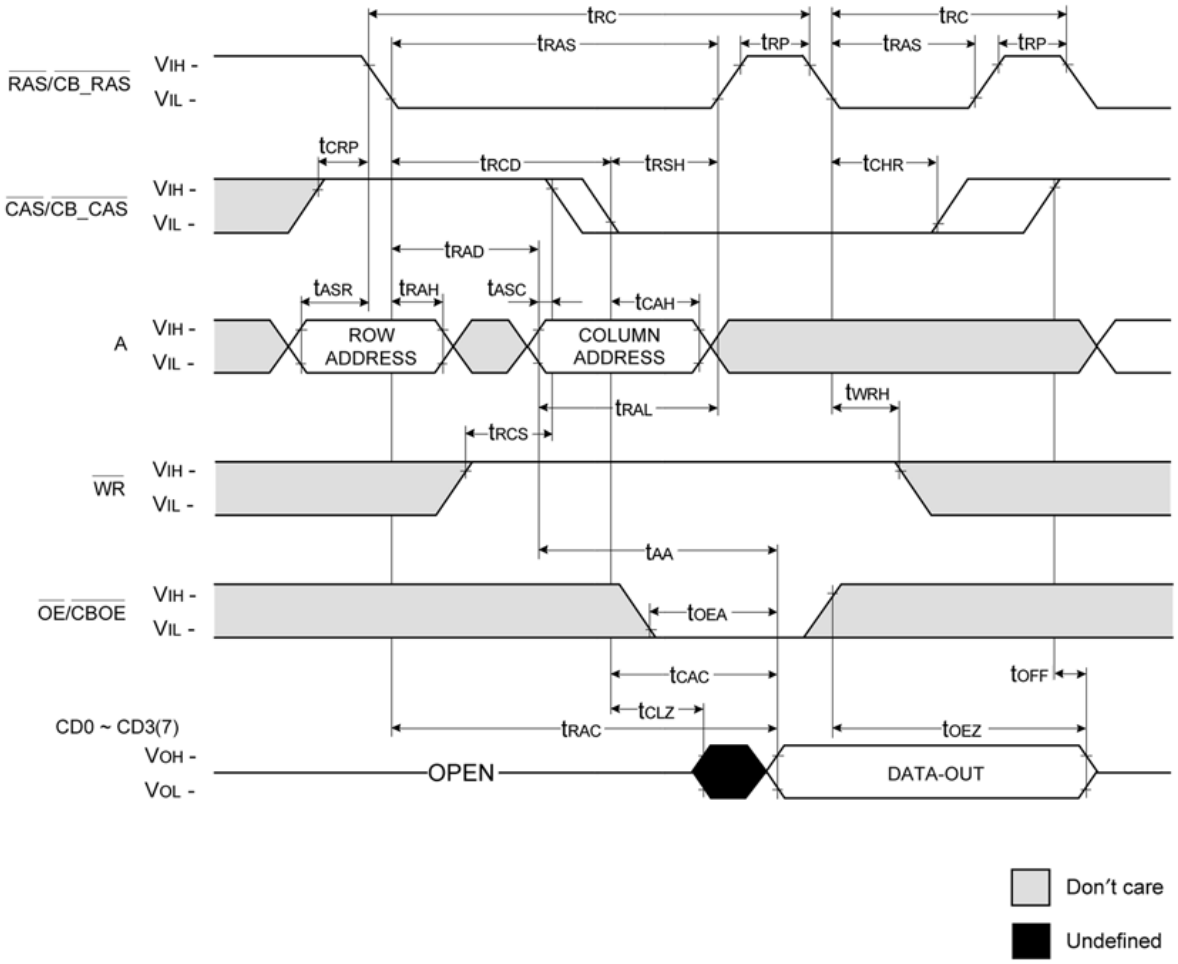


FIGURE 11. HIDDEN REFRESH CYCLE (WRITE)

NOTE: D_{OUT} = OPEN

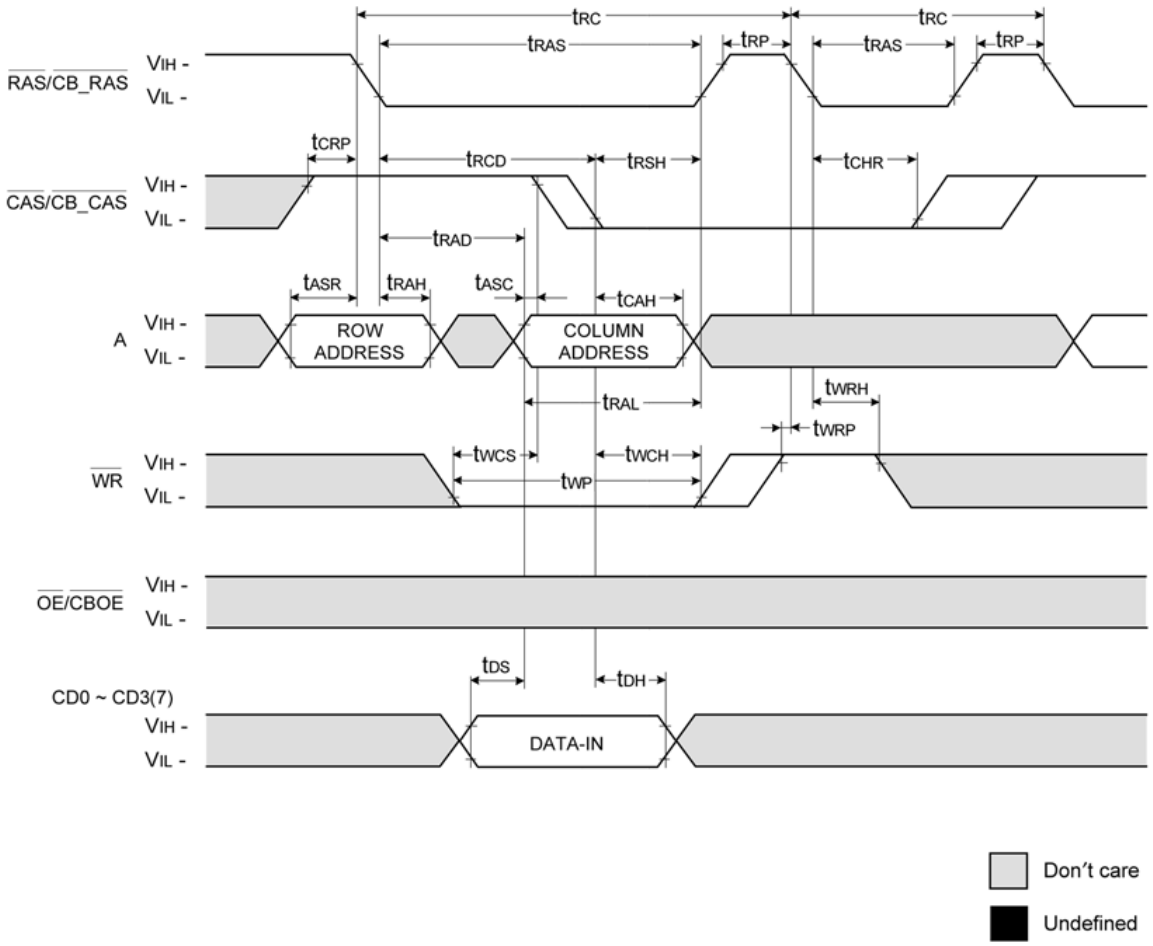
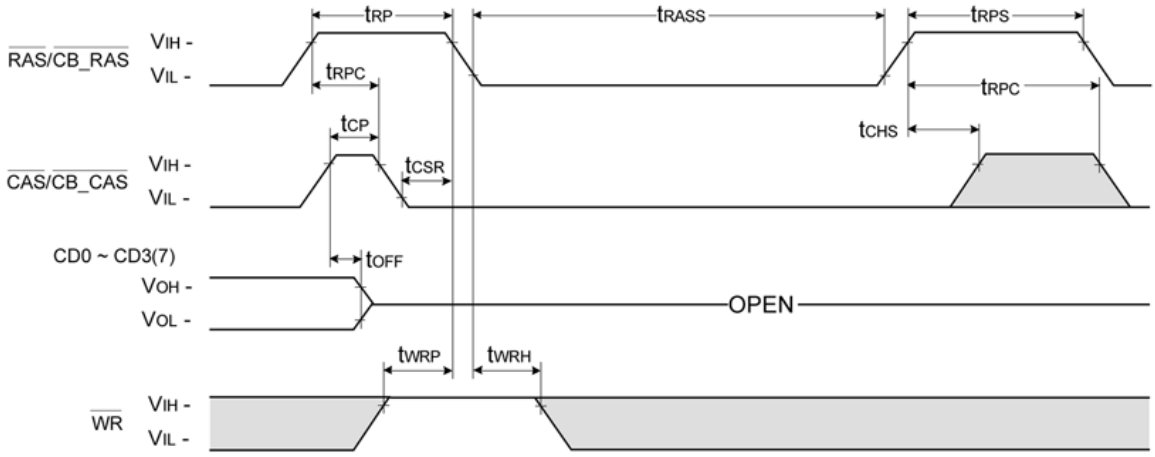
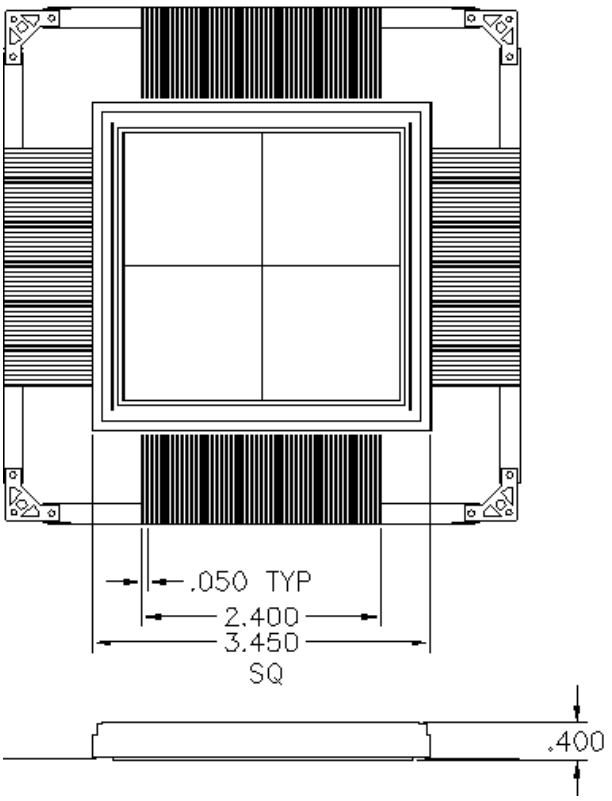


FIGURE 12. $\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE

NOTE: $\overline{OE}$, A = DON'T CARE





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SYMBOL	DIMENSION		
	MIN	NOM	MAX