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FT18

Application Note

Note:
The FTE18 demonstrator board facilitates the evaluation of the FT18 sensor. It uses the timing described in this application note.

PHILIPS

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A. Table of Contents

B. List of Figures

1. Introduction

This application note describes the operation and structure of the Philips FT18 frame transfer CCD image sensor. It is provided as a tool to aid in the design of camera modules using the FT18. Therefore the sensor is described in greater detail than the data sheet provides. Basic timing design is developed out of the sensor information. Block diagrams explain how to construct a Pulse Pattern Generator, including drivers, level shifting circuitry, sensor DC-voltages and the pre- (and post-) processing for the sensor. Some detailed schematics are also provided in the design example section which give some recommendations for operating the device. The mechanical dimensions of the FT18 will help to develop the proper opto-mechanical interface.

2. The FT18 Sensor

2.1 Features

- High resolution of 1024 x 1024 active pixels
- Can operate in a 1024 x 2048 (H x V) interlaced and a 1024 x 1024 true progressive scan mode
- Vertical binning is possible. (1024x512)
- Operates in frame transfer mode
- 7.5µm square pixels provide cost effective compromise between resolution and full well capacity
- One output register clocked at 40MHz allows 30 frames per second in 1Kx1K progressive scan mode
- Bi-directional output register allows single axis mirror readout
- Vertical antiblooming handles overexposure and highlights
- Low dark current, high dynamic range, high fill factor
- 2/3 inch image diagonal allows the use of standard off-the-shelf lenses
- Electronic shutter capability

2.2 Structure

The FT18 is a progressive scan frame transfer sensor. The active image area of 1K x 1K pixels contains square pixels of 7.5µm. The FT18 can also function as a 1K x 2K interlaced sensor. The sensor consists of 4 main areas: the image area, storage area, horizontal register and output buffers.

The device has one bi-directional output register located below the storage region. For normal image display the image lines are shifted to the left and read out of the left output buffer. To produce an image mirrored about the vertical axis, the right output buffer is used.

Frame Transfer Mode:

Normal operation of a frame transfer device includes capturing an image in the image area during a fixed integration time and then transferring the image into the storage section where it can be read out. While one image is integrated in the image area, the previous image now located in the storage region is read out line by line through the horizontal output register.

Each line in the register is shifted pixel by pixel towards the left or right output buffer and is converted into a voltage at the output of the CCD. The image should not be transferred to the storage region until all lines of the previous image are readout. Figure 1 shows the main areas of the device and some of the control signals.

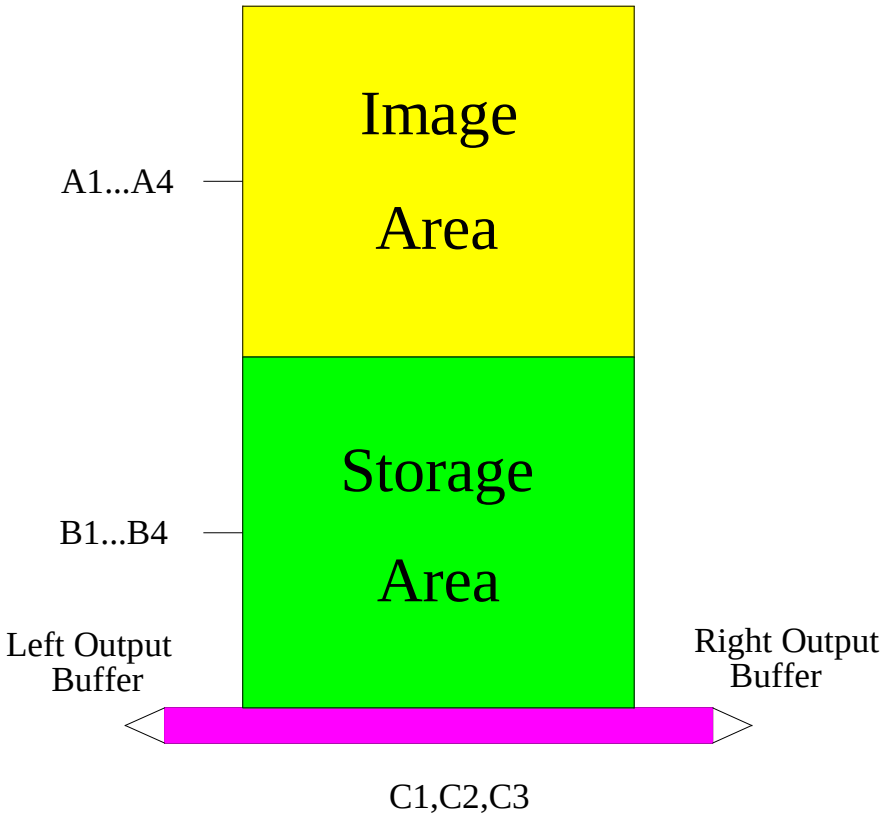


Figure A: FT18 Structure

2.3 Image Section

The image section of the device contains 1024 active image lines as well as a number of lines and pixels which are not active or image producing. The additional lines placed above and below the active lines are either black reference lines or contour lines. Contour lines are sometimes referred to as dummy lines. Black reference lines are located above and below the image lines and are covered with an aluminum light shield. They are used by the video processing electronics to establish a reference with which to compare the output video signal. This process of re-establishing a zero signal reference is also known as black clamping. The dummy or contour lines are found between the image and black lines. They may contain some charge in them due to reflections and partial exposure in the transition area of the light shield and active image area.

Horizontally, each line also contains a number of overscan and black reference pixels. If the black level must be refreshed faster than twice per frame, then the black pixels may be sampled. Overscan pixels are essentially the same as contour lines. They arise due to the transition from the active image area to the shielded black pixels. The diagram below shows the location of the various components of the image area. The signal lines or image gates labeled A1,A2,A3 and A4 control the operation of the image section.

Image Area Summary

Number of active pixels per line:	1024
Number of total pixels per line:	1072
Number of black reference pixels per line:	40 (2x20)
Number of overscan pixels per line:	8 (2x4)
Number of active lines:	1024
Number of black reference lines:	8 (top), 11 (bottom)
Number of dummy lines:	4 (top), 1 (bottom)
Number of total lines:	1048
Number of gates per pixel:	4, in the order A2, A3, A4, A1
First gate at the top:	A2
Last gate at the bottom:	A1

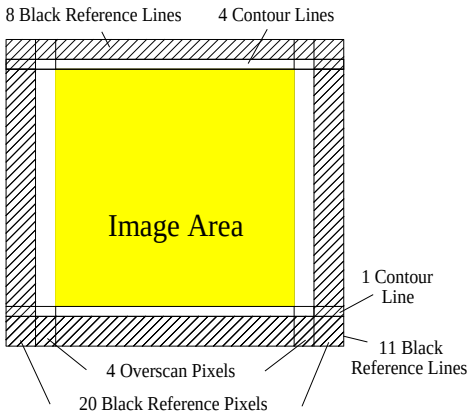


Figure B: Image Area

2.4 Storage Section

The storage section of the FT18 is an exact copy of the image area. It contains an identical number of pixels and lines. This enables the image to be transferred to and temporarily stored in the storage area while it is read out. Control of the storage section is reserved for the storage gates labeled B1,B2,B3, and B4. All image lines, black reference lines and pixels, as well as contour lines and overscan pixels are transferred to the storage region. The storage area is covered with an aluminum light shield to prevent additional exposure during the image readout.

Storage Area Summary:

Number of active pixels per line:	1024
Number of black reference pixels per line:	40 (2x20)
Number of overscan pixels per line:	8 (2x4)
Number of total pixels per line:	1072
Number of total lines:	1048
Number of gates per pixel:	4, in the order B2, B3, B4, B1
First gate (top), last gate (bottom):	B2, B1

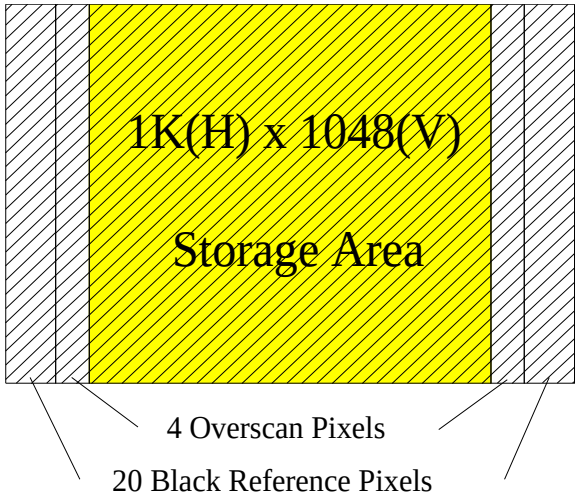


Figure C: Storage Area

2.5 Horizontal Register

The horizontal register contains an identical number of pixels as there are columns in the image and storage area. This allows the register to accept a complete line of pixels for readout. Additional dummy pixels are required in order to physically attach the output buffer to the output shift register. As the horizontal readout starts these additional dummy pixels give the output buffer time to stabilize before active image data can be sampled.

The register can operate in two different modes: shifting all pixels to the left or shifting pixels to the right. The output gate (OG) is connected to a DC-voltage as indicated in the data sheet. Control of the output register is assigned to the register gates labeled C1, C2, and C3. The detail which describes the gate sequence at both ends of the register is shown below. A definition of the "blocking gate" (shown in Figure 4) is included in a subsequent section of the application note.

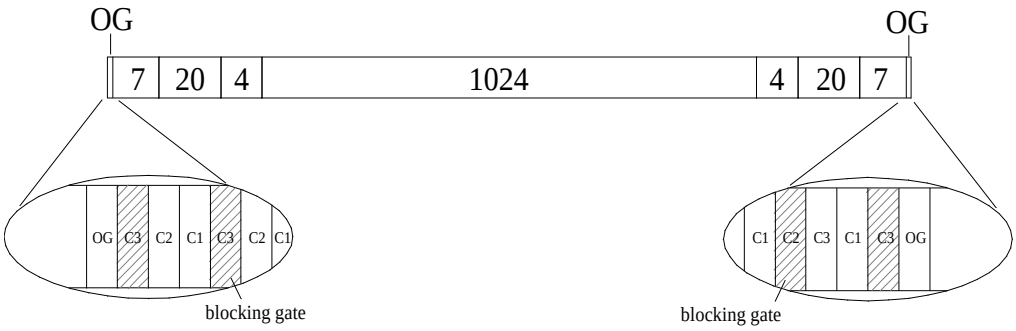


Figure D: Horizontal Register

Horizontal Register Summary:

Number of register cells (active video):	1024
Number of register cells (overscan):	8 (2x4)
Number of register cells (black reference):	40 (2x20)
Number of dummy cells:	14 (2x7)
Number of register cells (total):	1086 (1072+14)
Number of phases per cell:	3, in the order C3, C2, C1
Last clocked gate to the left/right:	C3

3. Operating the Sensor

3.1 The Potential Well

The sensor is able to convert incident photons into charge packets, which represent image data. The voltage levels applied to the image gates allows the charge packets to be collected and their position within the CCD controlled. These packets or pixels are defined by the A1-A4 image gates.

Each pixel consists of four poly silicon gates The image area gates are labeled A1-A4. These gates determine the behavior of a pixel. Depending on the applied gate voltage, a potential well (bucket) or electron barrier forms beneath the gate.

All Philips' CCD image sensors are buried channel devices combined with a vertical antiblooming feature. Buried N-channel devices allow the accumulated charge packets to travel beneath the silicon surface. Charge packets which travel deeper in the silicon are not easily trapped by the Si-SiO_2 interface states. This results in higher speed devices as well as devices with much better transfer efficiency. The vertical antiblooming structure allows the device to withstand an overexposure condition which would ordinarily result in blooming. This is a condition where excess charge (pixel sites generating electrons >> Qmax) spills over the channel stop barriers and blocking gate barriers into adjacent pixel sites.

The shape of the potential curve in the potential diagram shown in figure 5 is influenced by the applied gate voltage as well as the structure of the device. The drawing illustrates the potential profile in Volts versus depth in the silicon substrate for various applied gate voltages. Curve 1 represents an empty well under a positive biased gate during integration. Electrons generated in the upper part of the silicon will be collected in the potential well, electrons generated deeper will be absorbed into the n-type substrate. Holes are collected in the p-well. A blocking gate or barrier gate is biased during integration at 0V, as depicted by curve 2. The small potential well underneath this gate produces an active barrier gate. Electrons generated underneath the active barrier gate will be collected into neighboring potential wells. If all gates of the image cells are biased to 0V, there will no longer be any potential well in the silicon, and no electrons can be stored. Curve 3 shows this situation. The non collecting behavior of a pixel can be reinforced by biasing all gates to -5V as shown in curve 4. In this case all electrons will flow to the substrate.

The behavior of a CCD is not only influenced by the gate voltage, but also by the DC-voltages VNS for the n-substrate and VPS for the p-well. The initial approach is to set VPS and VNS to their typical voltage levels as given in the data sheet. To optimize the sensor performance VPS is fixed at the typical value while VNS is allowed to vary.

A higher VNS-voltage leads to better antiblooming performance, but decreases the well capacity and the light sensitivity. On the other hand a lower VNS-voltage increases the well capacity, but lowers the antiblooming performance. The optimum adjustment is achieved, when VNS is set as low as possible, while at the same time guaranteeing the specified antiblooming performance.

To verify this condition, a light level corresponding to the specified overexposure limit is projected onto the sensor. The VNS is adjusted while the first shielded lines above and below the image section are monitored for charge content. Proper antiblooming is achieved when the shielded lines are void of charge. This light level can be computed using the following equation:

light level = overexposure x full-well capacity / responsivity

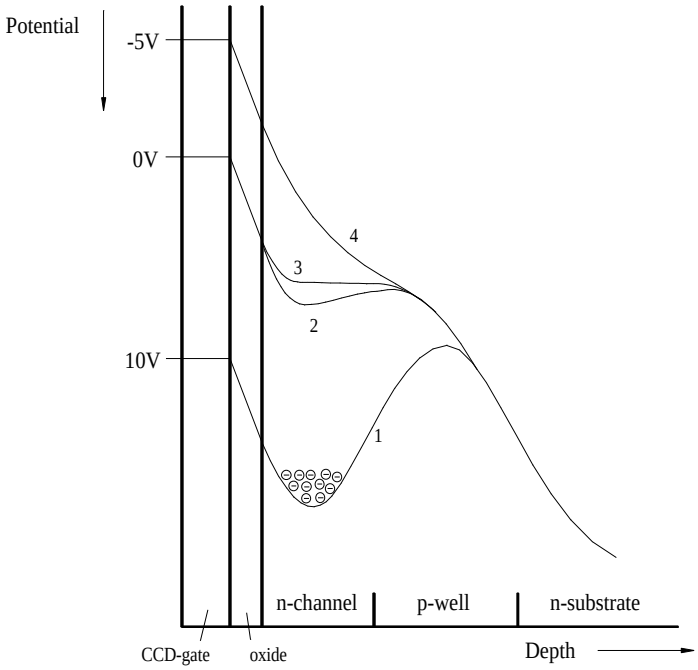


Figure E: Potential Well Diagram

3.2 Integration

Integration takes place in the image area only. Applying the specified voltage levels to gates A1 - A4 allows pixel sites to be formed. Applying the typical high voltage level (10V) (typical low voltage level plus typical voltage swing) to a gate results in a potential well being formed beneath it, and permits the collection or integration of electrons. When the typical low voltage level (0V) is applied to a gate, this gate forms a barrier underneath the gate and is therefore blocking (active barrier). The typical voltage levels can be found in the data sheet in the table *clock conditions*.

To form a cell, neighboring pixels have to be separated from each other. Channel stops prevent electrons from moving to the left or to the right, thus forming the pixel boundaries in the horizontal direction. Vertically one gate is set to its low voltage level in order to prevent electrons from moving up or down this column. The first gate at the top of the image section is an A2-gate, the last gate at the bottom is an A1-gate. For the FT18 sensor the normal operating mode during integration has 3 gates integrating (A2,A3,A4 set to 10V) and one gate (the A1 gate) functioning as the blocking gate.

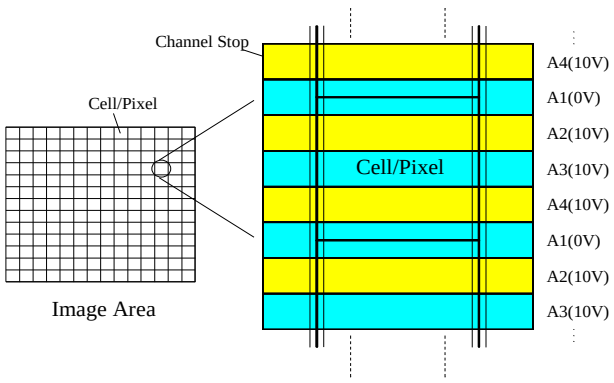


Figure F: Cell/Pixel Definition

Some applications may find it beneficial to perform integration under two gates instead of three. This leads to a loss in sensitivity, but increases the vertical MTF. The changes in the timing are not discussed in this application note, but can be derived from the information presented. When integration under two gates is desired, either A1/A4 or A2/A3 can be used as blocking gates, the other two gates are integrating.

3.3 Interlacing

Interlacing can be implemented in order to produce images with higher vertical resolution. Two fields can be captured in succession and displayed interlaced on a monitor, i.e. one field is written to all the odd lines of the monitor, the next field to all the even lines.

Interlacing with the FT18 can be realized in two ways. The first method involves the implementation with 3 gates integrating for each field. During field 1 integration, the A4 gate blocks while the rest integrate. And for field 2, the A2 gate is set low as the blocking gate while the rest integrate. The result is an interlaced image which has the same sensitivity as a 1Kx1K progressive scanned image, however the interlacing is implemented in such a way that the lines of each field overlap. The overlap results in a less than ideal vertical MTF for a 1Kx2K scan.

The second approach involves integration under only two gates for each field. During field 1 A1 and A2 could serve as the integrating gates while gates A3 and A4 block. Field 2 would then be integrated by A3 and A4 while A1 and A2 serve as the blocking gates. The second technique will result in a lower sensitivity however the vertical MTF will improve because the lines of field 1 and 2 do not overlap. **An interlaced application example is not given in this note.**

3.4 Black Reference

The FT18 sensor contains a number of black reference pixels and lines. The image area diagram of figure 2 illustrates the locations of the black references. There are 8 black reference lines at the top of the image area and 11 at the bottom. Restoring the black level can be accomplished at some point in the video processing stage of the electronics. If a restoration is required faster than every frame, then the 20 black pixels located to the left and right of each line may be used.

3.5 Charge Storage

The pixel structure in the storage area is similar to that in the image area. The charge from each pixel in the image area is contained in the storage area by the B1...B4 gates. The same principles apply to charge storage as for the integration of the image. When the typical high voltage level (typical low voltage level plus typical voltage swing) is applied to the gate, a potential well forms underneath the gate, the typical low voltage level forms an active barrier. Storing the charge packets in the FT18 storage area is accomplished by keeping B2...B4 high and gate B1 low . The first gate in the storage section is a B1-gate, the last gate is a B1-gate as well.

If interlacing is employed, then the storage region should store charge using the same scheme selected for interlacing in the image section. Pay close attention to the waveforms as the charge transitions from the image region to the storage region to assure that the information is not corrupted during the transfer. The complete charge packets can be stored under only two active gates in the storage section of the CCD. This might be a desirable way to operate the CCD because dark current generation is lower under two storage gates than it would be for three. More than two blocking gates should not be used, because it would leave just one storage gate. One gate does not have the ability to store a complete charge packet.

3.6 Charge Pumping

Charge pumping (CP) is an optional technique involving the consecutive pulsing of the image gates (temporarily inverting the area under each gate) to the minimum low level in order to reduce dark current build up.

Interface states in the semiconductor bulk and at the Si-SiO_2 interface are responsible for the generation of dark current. Pulsing each gate causes these states to be filled with holes or emptied of electrons. These holes are likely to recombine with electrons possessing the energy to fill an interface state but not enough energy to become free electrons.

Controlling the temperature of the device will result in substantial reductions in the dark current generation. The dark current will reduce by half for each 8 degrees C of cooling. However not all applications can implement cooling. Therefore charge pumping is economical and easy to implement for cooled as well as ambient applications.

To refill (re-empty) the interface states, the charge pumping pulse is repeated every line blanking period. The length of a charge pumping pulse depends on the timing implemented and on the read out frequency. Because charge pumping takes place during the line blanking period the time required to keep each gate low can be very short. In this case it is useful to apply a voltage level between the minimum low voltage level and the typical value to the gates during charge pumping to obtain satisfactory results. The low voltage change can be realized with the help of one additional pulse (in this example the pulse is named ALOWCP).

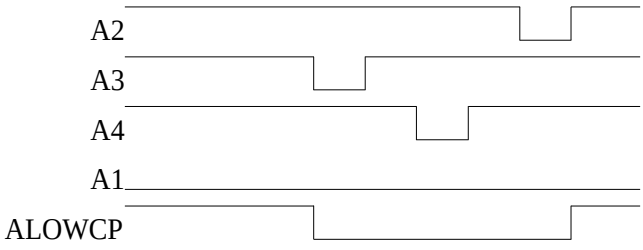


Figure G: Charge Pumping

3.7 Charge Reset or Electronic Shutter

Charge reset (CR) is used to drain all integrated electrons in the image area to the substrate. All A-gates are set simultaneously to the typical charge reset low voltage level. The charge flows towards the silicon substrate. Charge reset can be done after each frame transport to completely empty the image area of any remaining charges. This eliminates possible smear artifacts generated during the previous frame shift and resets each frame at the beginning of the integration period. The best results are obtained by allowing the gates to stay low for a period of time greater than or equal to the minimum charge reset time.

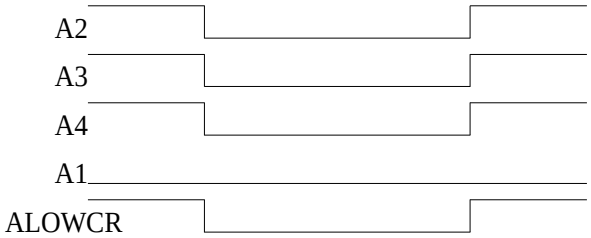


Figure H: Charge Reset

Charge reset is often referred to as electronic shuttering. The technique can be used to shorten integration periods thus producing various electronic shutter speeds. Charge which is already integrated can be dumped by a charge reset to begin a new shorter integration period during the same frame time. In this case the charge reset should be performed during the line blanking period, because the charge dumped to the substrate will influence the readout of the image in the storage area.

Two charge reset methods can be offered. The first method has all four A-gates set to the typical low voltage level (0V), while for the minimum charge reset time a 10V CR-pulse is applied on top of the n-substrate voltage VNS. The second method uses all four A-gates set to the minimum low voltage level (-5V) for at least the minimum charge reset time. The ALOWCR-pulse can be used again to switch the low voltage level from the typical to the minimum value. All Values are specified in the data sheet under *clock conditions* and *performance.*

3.8 Frame Transport

The frame transport is the transfer of the complete image from the image area to the storage area. It takes place during the video frame blanking period. Special attention should be paid to the frame transport, because the image and storage area interact with each other during this operation.

Transporting the charge packets through the image and storage area is done by controlling the voltages on the A1... A4 and B1... B4 gates. During integration A2...A4 are high and A1 is low. Shortly (5µs) before the frame shift starts A2 is set low, so that the charge packet is contained under two gates, A3 and A4. When starting the image gates A1/A2 are low and A3/A4 are high, in the storage section the gates B1/B2 are low and B3/B4 are high. First A1/B1 are set high, then A3/B3 low, A2/B2 high, A4/B4 low, A3/B3 high, A1/B1 low, A4/B4 high, A2/B2 low and so on. The charge packet has moved down one line. During the frame transport the A-pulses and the B-pulses are clocked identically. This assures that the image is transferred intact to the storage region. To reach a sufficient overlap during the transport, a duty cycle of 5:8 is used, for 5 time units the pulse is high, for three time units it is low. The delay from pulse rising edge to edge is 2 time units or 90°.

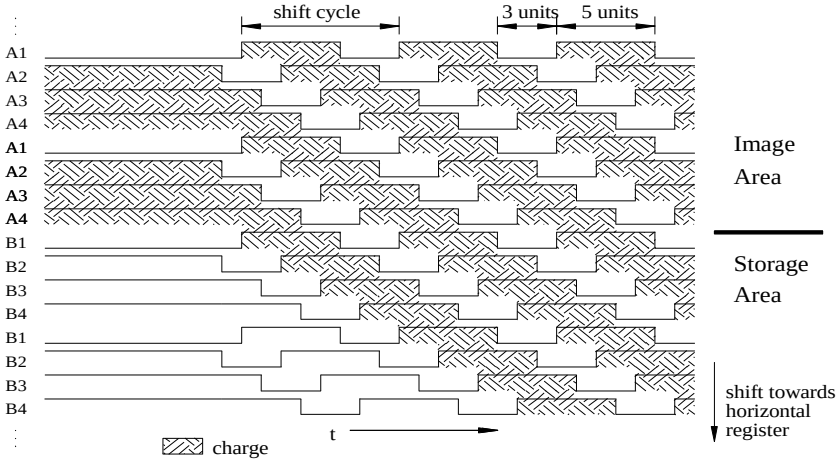


Figure I: Frame Transport

In the image area the typical high (10V)and low voltage (0V) levels are applied to the gates during integration, then during the frame transport, the high level of the A and B clocks can be switched to a maximum of 12V. This results in a higher Qmax and is a trick which can be used to get additional performance from the device. These tri- level clocks (0V,10V,12V) do not have to be implemented and a much simpler electronic design results if standard clocking is implemented (0V,10V). The storage area uses the typical low voltage level and the typical high voltage level (10V) also. The low voltage level for the A- and B-pulses remains at the typical low voltage level, when the frame transport occurs.

The number of shift cycles is equal to the number of lines in the storage area, 1048. To maintain the typical well capacity Q_{max} , it is recommended to transport the charge no faster than the typical transport speed as specified in the FT18 data sheet. The maximum frame transport frequency corresponds to a sensor operating at 30 frames per second, while the typical value is used in 25 frames per second applications.

3.9 Line Transport

The line transport operation transfers charge from a line in the storage area (using the B-gates) to the horizontal register (C-gates) during the line blanking period. The shift mechanism is identical to that of the frame transport, changing the gate voltages from low to high and vice versa to move charge from one location to the next. It is recommended that the maximum high voltage level (12V) for the B-pulses be used during the line transport.

It is assumed that the gate voltages of B1 is low when storing an image. The last gate in the storage section is a B1-gate. To shift exactly one line, the following settings are applied: B2 is brought low, B1 high, B3 low, B2 high, B4 low, B3 high and B1 low then B4 high. The moment B1 goes low, the charge is completely shifted into the horizontal register. The horizontal register takes over the charge packets from the last line of the storage area and starts shifting them towards the output buffer.

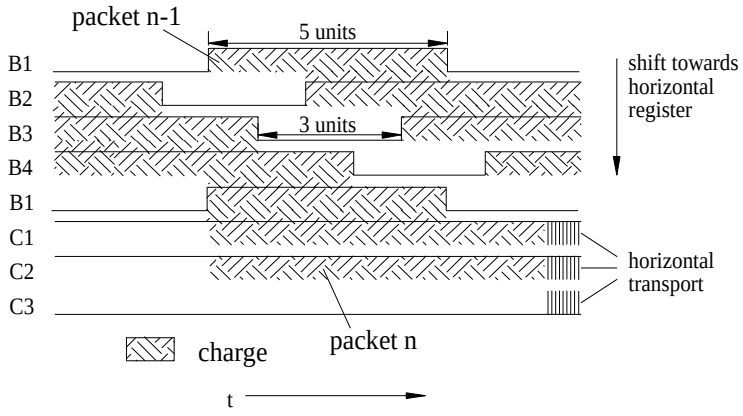


Figure J: Line Transport / Vertical Transport of 1 Line

3.10 Horizontal Transport, Output Buffer and Output Signal

Horizontal Transport:

During the line blanking, gates C1 and C2 are set high, gate C3 is low. The horizontal register receives the charge packets under the gates C1 and C2, when the line transport takes place. The C3 gate is used as a blocking gate. After a line is transported into the horizontal register, the charge packets of this line are shifted towards the output amplifier. The horizontal transport discussed here refers to shifting towards the left through the left output buffer. This results in an image readout which is a normal view (not mirrored). To shift the packets to the right output buffer (horizontal mirror view), the pulses on gates C1 and C2 interchange

The maximum transport frequency is given in the data sheet as 40MHz. This clock frequency should be used to operate the device at 30 frames per second. The 36 MHz operating condition applies to sensors operating at 25 frames per second. The duty cycle used for the horizontal transport is 3:6 (or 50%), for 3 time units the pulse is high, the other 3 units it is low. The delay from one pulse to the next is 2 time units or 120°.

The transport mechanism is again similar to the shifting in the image and storage region. The difference here is that the output register is operated as a 3 phase CCD register. Changing the gate voltages in a defined order forces the charge packets to move. After gate C1 and C2 receive the charge packet, C1 goes low, then C3 high, C2 low, C1 high, C3 low, C2 high and so on. The charge has moved exactly one pixel to the left. Producing the clocks for the output register can be the trickiest part of the camera design. Section 5.2 of the application note describes a techniques which can be used to generate fast C pulses using time delays. Operating the CCD at its limits, using a 40MHz pixel clock, makes it very difficult to generate the C pulses in a programmable logic device. Therefore a discrete solution is most practical. The other slower logic can be implemented easily in EPLDs.

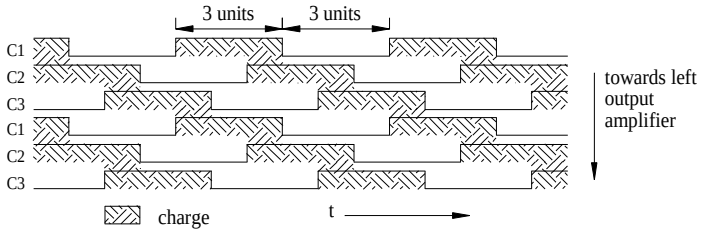


Figure K: Horizontal Transport Towards Left Output Buffer

Output Buffer:

The output buffer is shown schematically below. The output gate (OG) is connected to a DC-voltage (typically 5.4V). The typical value can be found in the data sheet. The output gate voltage produces a barrier that prevents the charge packets from flowing onto the floating diffusion while the C3 gate is high. When this C3 gate is brought low the charge packet flows to the floating diffusion node and produces a voltage output which is proportional to the number of electrons in the packet. ($\Delta V=nq/C$)

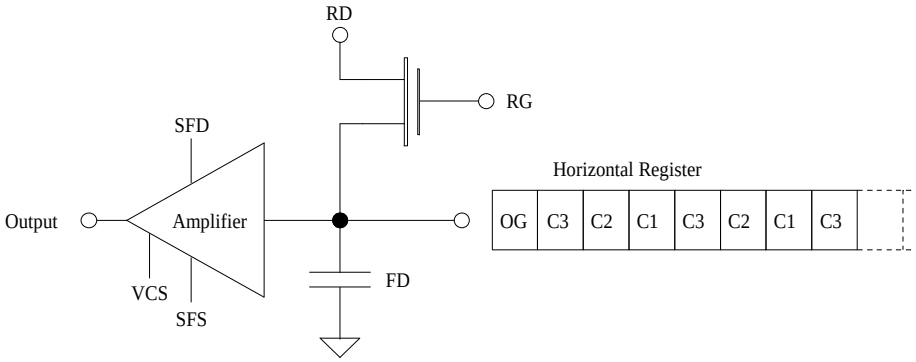


Figure L: Functional View of Output Buffer, Floating Diffusion, Horizontal Register

The FT18 data sheet defines the low voltage levels and voltage swings of the C-pulses. The output buffer is a three stage source follower. The floating diffusion converts the charge into a voltage which is then amplified and buffered. SFD is the DC-drain voltage of the source follower, SFS the DC-source voltage. VCS controls the current source of the first and second stage of the amplifier. **It is recommended that the typical values shown in the data sheet be used.**

Reset Gate:

The reset gate (RG) input pin is connected to a MOS-transistor gate. If RG is high, the charge on the floating diffusion is drained towards reset drain (RD), which is connected to a positive DC-voltage. The recommended voltages for all DC biases can be found in the FT18 data. The pulse on RG is derived from the C-pulses. It has a width of approximately 1/6 Tp (T_{RG}). For a 40MHz shift frequency Tp is 25ns, therefore timing of the RG-pulse in relation to the C-pulses is very critical and needs a carefully designed circuit.

When RG is brought high the electrons on the FD are drained off. This occurs before a new charge packet is shifted onto the floating diffusion (when C3 goes low). The reset gate pulse causes cross talk with the output signal of the CCD. This can be seen in the output waveform and is depicted below in figure 13. More information on RG crosstalk and its elimination can be found in the discussion of pre-processing.

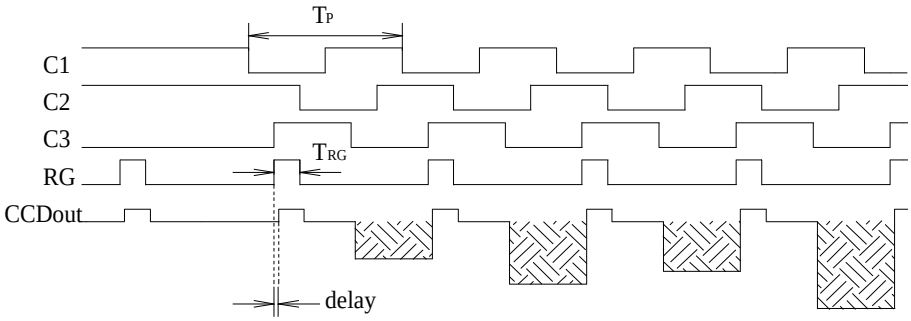


Figure M: The Reset Gate Pulse

The output signal of the CCD contains a small delay relative to the RG and C3 pulses. This delay is introduced by the output buffer and is approximately 5 - 7ns.

The Output Signal of the CCD:

The output signal of the CCD is depicted here as it can be seen on an oscilloscope. It has to be processed by a pre-processing circuit to eliminate noise and demodulate the video signal. The signal can be divided into three main parts, the cross talk from the reset gate pulse, the reset hold level, which is used as a zero electron reference for the pre-processing and the actual video signal.

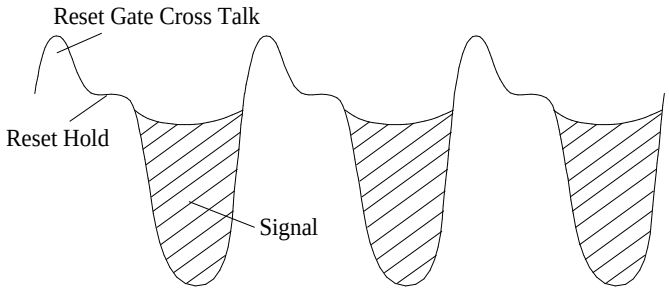


Figure N: Output Signal

3.11 Pixel Binning

Pixel binning is supported vertically by the FT18 sensor but not horizontally. Binning can be done vertically by shifting two lines into the horizontal register during the line blanking, instead of only one (see chapter 3.9). The charge storage capacity of the output register can reliably store 2 lines of charge. More lines can be binned if the total charge capacity of the output register can accept them. After the line transport is complete, the horizontal shift transports the charge packets to the output buffer.

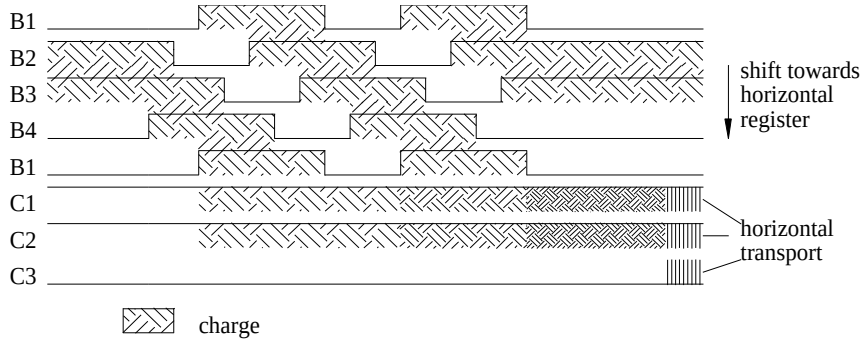


Figure O: Vertical Pixel Binning

The output register of the FT18 does not contain a summing gate, therefore traditional horizontal binning is not supported. The following technique may be incorporated to accomplish horizontal binning , however, external circuitry must be utilized. Adding a high speed sample and hold amplifier between the output buffer and the CDS preprocessor will allow horizontal binning to be implemented. First, the reset gate (RG) pulse is applied while the S&H is in sample mode. The CDS preprocessor then samples the reset level. The first pixel is read out of the buffer followed by the second pixel. The S&H is placed in hold mode at the output level produced by the two pixels. Then the CDS samples this signal level and amplifies the difference between it and the reset level. The RG pulse is chosen in a way that the duty cycle of the actual video signal is again 50%. The delay caused by the output buffer is the same as mentioned before without the binning. T_{RG} is 1/6Tp with Tp = 25ns. The delay is caused by the output buffer of the CCD as already mentioned in section 3.10.

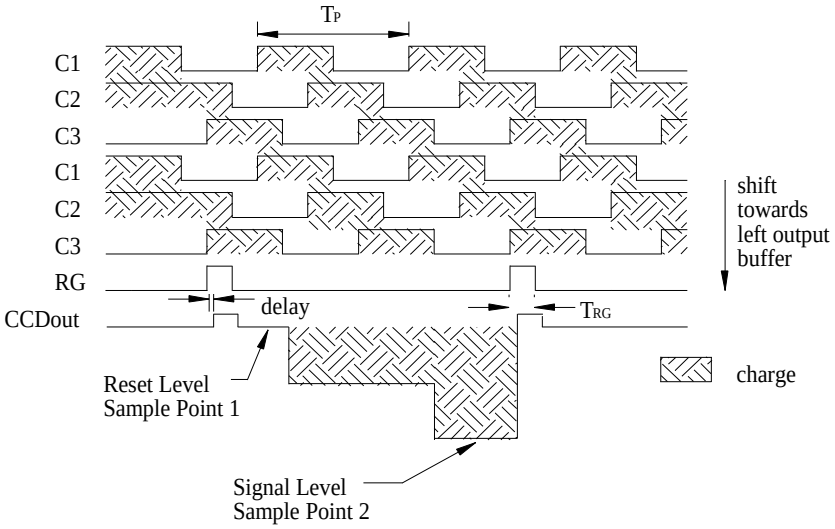


Figure P: Horizontal Pixel Binning

4. Application Example

4.1 Definitions

The FT18 can be operated at many different frame rates. When you consider the various requirements for frame rate and horizontal readout frequency, the number of design examples can become enormous. As a design example, a common operating mode is selected. As an application example, the situation where the CCD is scanned at 30 frames per second is presented. This readout mode demonstrates the device operating at it's targeted performance specification.

To begin the design some items require definition.:

- Format: 1024 x 1024 progressive scan
- Readout: through the lower left output (normal video)
- During integration: A1 serves as the blocking gate, while the integrating gates are A2...A4, Gate voltage levels: low voltage level of 0V, high voltage level 10V
- During Storage: B1 serves as the blocking gate, B2..B4 Transfer the image charge Gate Voltage levels: low voltage level 0V, high voltage level 10V
- Neither horizontal nor vertical binning will be implemented
- Charge pumping: pulse width 700ns, applied with -5V low voltage level, 12V high level
- Charge reset: pulse width 3.875µs, applied prior to each integration with -5V voltage level
- Black reference: Restored before active frame video readout. Scan line 49.
- Frame transport: 1048 lines with a speed of 714kHz, low voltage A- and B-pulses 0V, swing 12V
- Horizontal output register: pixel clock 40MHz, low voltage 3V, swing 5V
- Reset gate (RG): low voltage 0V, swing 10V
- Sensor DC-voltages: typical values as given in the data sheet
- Synchronization pulses: VD, HD (≡SSC), FDV, LDV
- Processing pulses: PB, BLC, BPC, ALOWCP, ALOWCR, AHIGH, BHIGH, SSC (≡HD)

4.2 Design Overview

The design of a camera module as described here using the FT18 consists of six different blocks. The PPG is responsible for generating all the timing of the sensor pulses as well as pulses for processing and synchronization purposes. The sensor needs a number of DC-voltages, which have to be generated. To prevent the sensor from being destroyed adjustable voltages should be limited to the max. and min. limits specified in the data sheet. The DC-values must never exceed the maximum voltage ratings with respect to VPS and VNS, **even when turning on the camera.**

The pre-processing is necessary to demodulate the video signal and suppress reset and amplifier noise. Different pre-processing constructions are possible, e.g. correlated double sampling or soft clamp pre-processing (described later). In order to optimize the performance of the FT18 careful design of the pre-processing circuitry is essential. All implementations should follow best design practices for high speed circuits, regardless of which construction is chosen. The post-processing requirements are application dependent and can even be implemented in the digital domain. Some of the post processing functions include variable gain, black level control, white and black clipping, and in some cases sync insertion.

The following pulses are based on the application definition given in chapter 4.1, several synchronization and processing pulses are offered. The shape of these pulses depends on the application and on the camera design, not all of these pulses are necessarily needed, others may have to be added. But the description of the sensor together with the application note timing makes an adaptation rather simple.

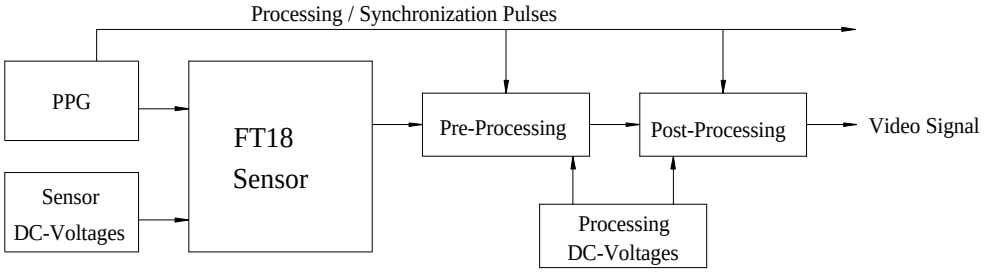


Figure Q: Block Diagram of Application Example

Sensor pulses:

- C1... C3 the 3 gates of the horizontal register
- RG the reset gate of the output buffer
- A1... A4 the 4 gates of the image section
- B1... B4 the 4 gates of the storage section

Synchronization pulses:

- HD Horizontal Drive (Same as SSC)
- VD Vertical Drive
- FDV Frame Data Valid
- LDV Line Data Valid

Processing pulses:

- SSC start/stop C (determines horizontal transport, high → new line is shifted into the horizontal register, low → horizontal transport takes place
- PB pre-blanking (determines active, black and timing/overscan pixels)
- BLC Black line clamp, determines black reference line per frame
- BPC Black pixel clamp, determines black reference pixel per line
- ALOWCP Switches low voltage of A-pulses from 0V to -5V during Charge Pumping
- ALOWCR Switches low voltage of A-pulses to -5V for Charge Reset
- AHIGH Switches the high voltage of the A pulses from 10V to 12V during frame shift and charge pumping.
- BHIGH Switches the high voltage of the B pulses from 10V to 12V during frame shift and line transport.

4.3 Calculations

The pulse timing for this application example will be computed based on the selection of the 40MHz pixel clock and the defined pulse width limits and shift frequency limits for the FT18. To begin the timing design the line time and frame time are first computed.

To compute the line time the following intervals have to be added. Readout times for the complete output register as well as a blanking interval are added together. The output register contains 1024 active pixels + 40 black reference pixels + 8 overscan pixels + 7 dummy pixels. This adds up to 1079 pixel clocks. A period of 153 clocks is reserved for horizontal blanking. The total including blanking equals 1232 pixel clocks.

The frame frequency can be computed in the same way. The frame rate is computed by adding the time to readout the storage region plus the amount of time required to shift the image to the storage region (the shift time is computed in section 4.6 as 58688 pixel clocks or 47 lines + 784 clocks). The frame time expressed in terms of horizontal line time is 1048 lines from storage region + 48 lines to perform frame transfer = 1096 lines.

line time = 1232/40MHz

= 30.8μs/line

⇒ the line frequency is 32.467kHz

frame frequency = 1 / (1096lines x 30.8μs/line)

= 29.62Hz

4.4 Horizontal Timing

The horizontal timing describes the synchronization, processing, and A- and B- pulses as they are generated relative to the line timing. A video line including blanking consists of 1232 pixels or has a length of 30.8 µs. The drawing shows where the rising and the falling edges of the pulses appear with respect to the number of pixels per line. '*' Indicates PB is delayed 2 pixels due to video processing delays with respect to the SSC pulse.

In the timing diagram below, the following explanations are in order.

CR(A1-A4) - Refers to the state of the image gates as they perform a charge reset operation. The pulse edges rise and fall during the line blanking in order to limit the disturbance on the active image as it is readout.

An(CP) - Illustrates the charge pumping sequence implemented by the image gates during the line blanking period. Obviously, charge reset and charge pumping cannot occur at the same time. One or the other takes place. Usually charge reset is assigned priority over charge pumping.

B(n)LTR - Describes the storage gate pulse sequence which transfers an image line from the storage section to the serial output register. See figure 10 also.

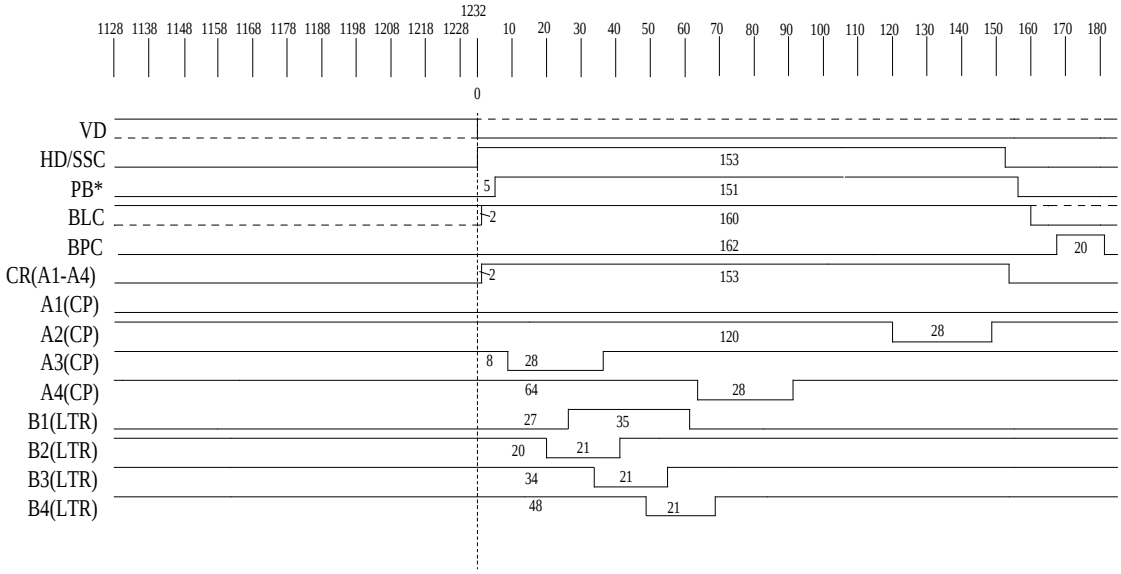


Figure R: Horizontal Timing

4.5 Vertical Timing

The vertical timing describes the pulses for each frame. A frame including blanking consists of 1102 lines, this results in a frame time of 32.62ms. The following drawing shows when the rising and the falling edges of the pulses appear in relation to the video lines. The '*' again indicates the pulse which has a delay of 2 pixels caused by the video processing. The black filled area shows the frame transport from the image to the storage area.

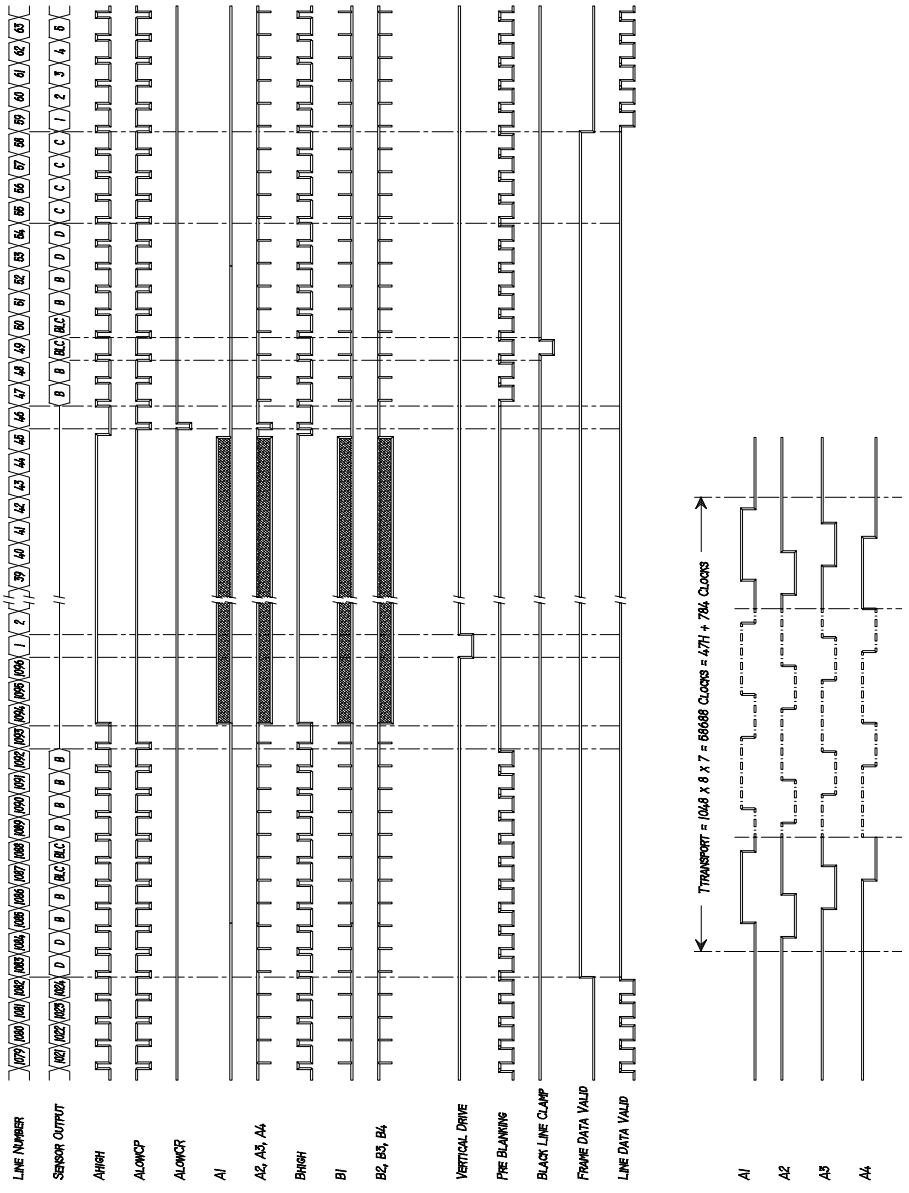


Figure S: Vertical Timing

4.6 Frame Transport or Vertical Transport

The frame transport timing diagram is illustrated in the previous figure. The transport pulses are derived from the pixel clock by dividing it by 56. This gives a transport frequency of approximately 714KHz. The transport waveform has a period of 1/714KHz = 1.4uSec. This corresponds to 56 pixels. To generate the required 5:3 duty cycle the pulse must be high for 35 pixel clocks and low for 21 clocks. The transport time is:

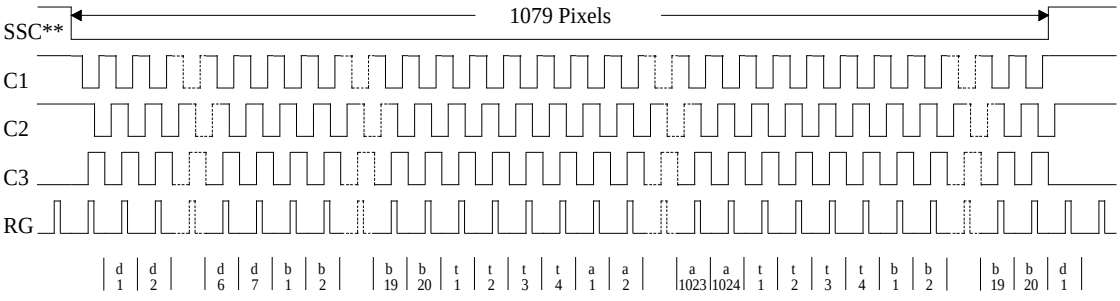
(H= 30.8us = 1232 clocks)

$$T_{Transport} = 1048 \times 56 = 58688 \text{ pixel clocks or } 47H + 784 \text{ clocks}$$

4.7 Fast C Pulse Timing - C1, C2, C3 and RG

The SSC pulse can be used to control a multiplexor. The mux allows selection of the fast C pulses or the fixed C pulse levels. The implementation is pictured schematically in section 5.2. When SSC is low the register shifts a line out of the CCD. When the SSC pulse is high the C pulses assume the state required to accept line data from the storage region. The SSC pulse is synchronized through a DFF which is clocked with the C1 pulse. The synchronization assures that the transfer remains uncorrupted by pulse misalignments.

Selecting an EPLD with fast propagation delays (in the <=7nsec range) will assure that the SSC pulse will remain synchronized to the C pulses. Timing glitches or waveforms which lose there phase relationship in the operation of the output register produce poor images. Special care should be given to this portion of the design.



d - dummy pixels, b - black pixels, a - active pixels, t - timing or overscan pixels

Figure T: Pixel Timing of the Horizontal Transport

Each line consists of 1079 pixels in the following order: 7 dummy pixels, 20 black pixels, 4 timing pixels, 1024 active pixels, 4 timing pixels, 20 black pixels. The total number of pixel clocks per line is 1232, and the blanking period is 153 pixels. Again the clock numbers add up to equal the line time as a check. During the line blanking period C3 is low (blocking gate), and C1 and C2 are high.

In the shifting mode the following items are important. A charge packet appears on the floating diffusion when C3 goes low. The reset gate (RG) pulse first discharges the floating diffusion and then it is ready to accept the next charge packet. The duty cycle of the C-pulses is 3:6 (50%) while the duty cycle of the RG-pulse is 1:6 (pulse width of ~4ns). At a transport frequency of 40MHz the resulting shift cycle is 25ns. The delay from one C-pulse to the next is 25/3ns = ~8.3nSec (phase shift is 2/6 or 120°).

5. Pulse Pattern Generator

5.1 Block Diagram

The structure of the Pulse Pattern Generator is shown in the block diagram below. The definition of the pulse pattern generator in this instance will include the digital pulse generator (EPLD) and the associated circuitry required to generate all of the sensor pulses (i.e. the level shifters, buffers and drivers). An Erasable Programmable Logic Device (EPLD) is used to generate the pulses, with the exception of the fast pulses C1...C3, and RG, which are high frequency pulses (max. 40MHz) and therefore in this case too fast for the EPLD to synchronize.

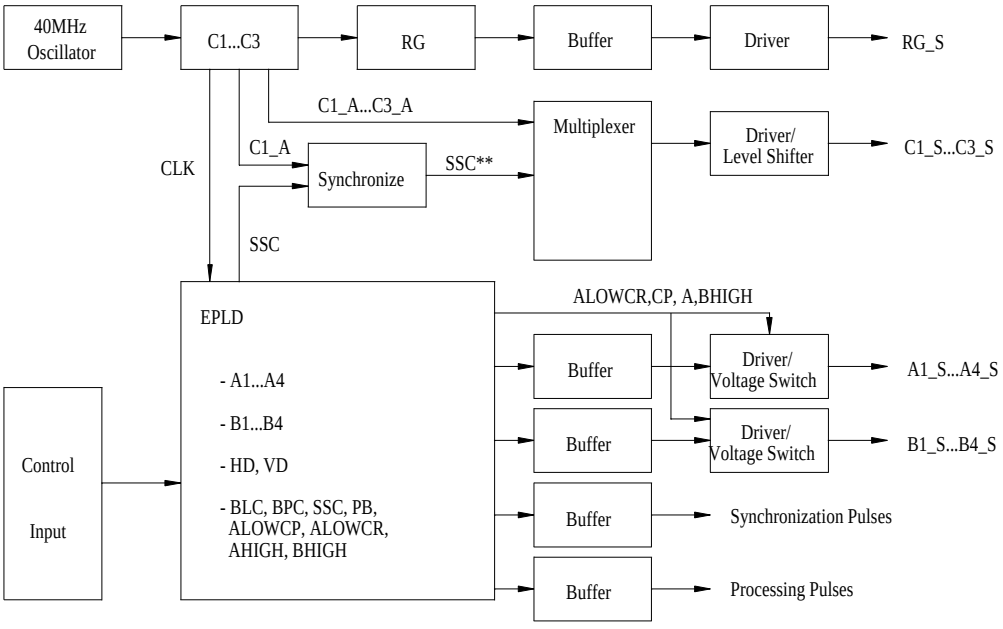


Figure U: Block Diagram of Pulse Pattern Generator

The control inputs might consist of pins which decode to various exposure time settings, inputs which turn on line binning as well as inputs which determine additional features unique for each application. The block diagram represents a typical configuration and is intended primarily to familiarize first time camera designers with the basic operating requirements for Philips' CCD image sensors.

5.2 Sensor Pulses C1 - C3

The fast C-pulses are generated from the 40MHz oscillator using delay lines. Because the horizontal register has 3 phases, the delay is computed to be 1/40MHz/3 = 8.33ns. This delay produces pulses with the overlapping waveforms shown in figure 11. The clock input for the EPLD (CLK) is derived from the phase C1_A. The inverter comes from the AC logic family. Silicon delay lines can be purchased from manufacturers such as Dallas Semiconductor, Data Delay Devices and ESC Electronics Inc.

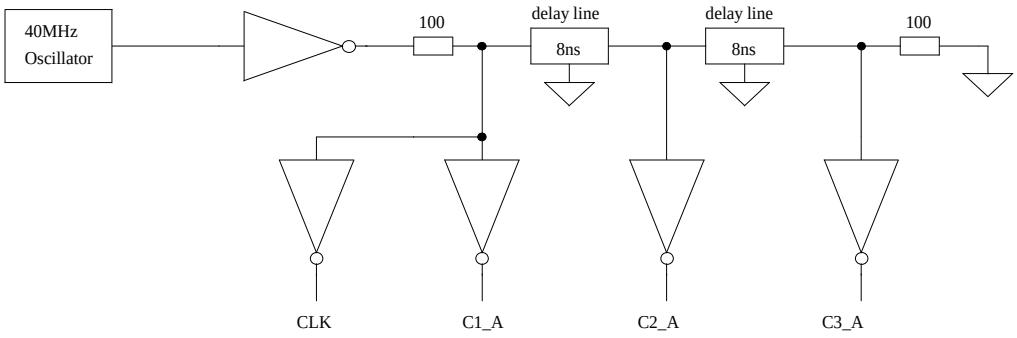


Figure V: Generation of C-Pulses

The pulse C1_A and the SSC pulse generated by the EPLD are synchronized with a flip-flop to achieve a smooth transition from the line transport state to the line shifting operation. The multiplexor switches the voltage levels from +5V (C1, C2) and 0V (C3) to the 40MHz shift cycles. Both devices preferably come from the AC logic family.

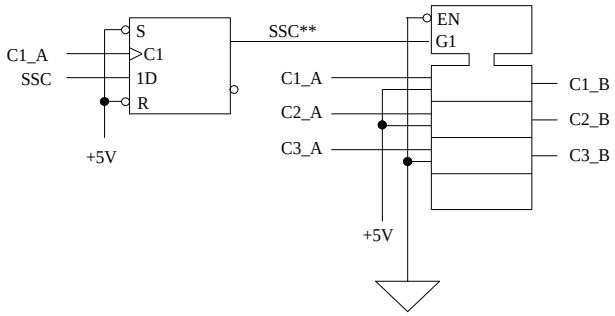


Figure W: Synchronization of SSC-Pulse / Multiplexing C-Pulses

The drivers need to be able to drive the gate capacity of ~85pF, while maintaining the proper pulse shape and a swing of 5V. This can realized with the TI CDC204 low skew clock drivers. Devices can be connected in parallel to increase drive capacity. To reach the specified high and low voltage level for the three C pulses, diodes clamp the pulses to VCH. The level shifting moves the high voltage level to 8V and the low voltage level to 3V. C1_S, C2_S and C3_S can be connected directly to the sensor pins C1, C2 and C3 respectively.

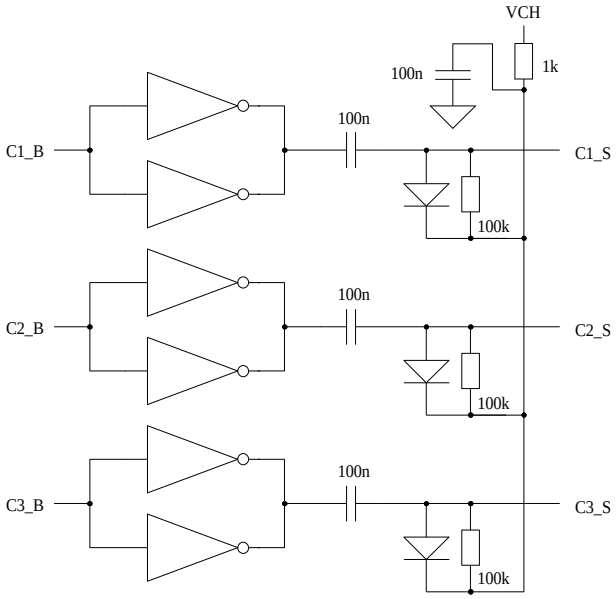


Figure X: Driver / Level Shifter C-Pulses

5.3 Sensor Pulse - RG

The RG-pulse is generated from the C-pulses C2 and C3, using a simple AND from the AC logic family. To shift the RG-pulse and adjust the pulse width, additional short delays can be used, which then delay the pulses C2 and C3 to get an equal propagation delay for the C pulses and RG.

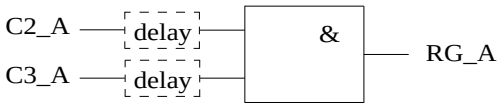


Figure Y: Generating RG

The driver configuration generates the voltage swing of 5V or 10V to drive the capacity of the reset gate (RG). The RG pulse is clamped to the high voltage level VRGH. The RG pulse should encounter the same delays caused by multiplexors, buffers and drivers as the C pulses C2 and C3 which generated RG. Therefore additional circuitry may be necessary to fine tune the delay.

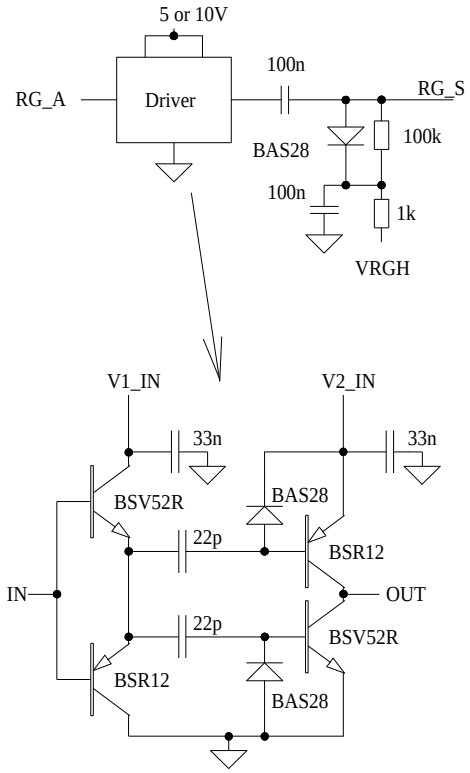
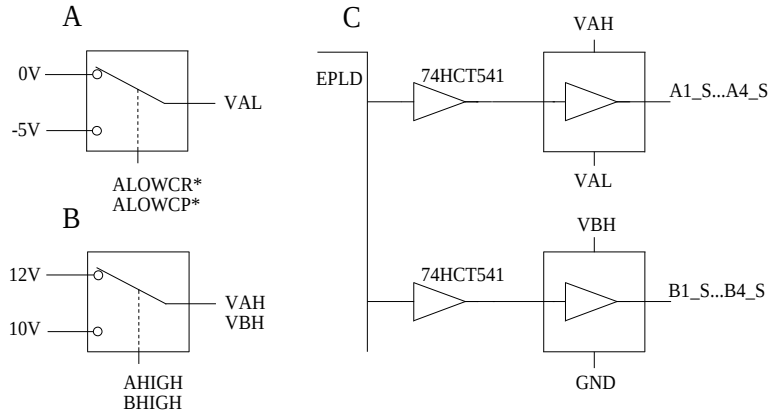


Figure Z: Driver / Level Shifter for RG

5.4 Sensor Pulses A1 - A4 and B1 - B4

The circuitry "A" shown in figure 27 switches the low voltage level for the A-pulses from 0V to -5V during charge pumping and charge reset. Drawing "B" illustrates a possible switching implementation of the high voltage level from 10V to 12V. This would occur during the frameshift operation and would apply to the A and B clocks. A 2-channel analog multiplexor can be used as the switching device.

The A and B digital pulse patterns are generated within the EPLD as depicted in figure 27 "C". After the pulses are buffered, a driver delivers the voltage swing for the individual gate capacities (~3.75nF). The driver recommended is the Elantec EL7212C inverting MOSFET driver. The non-inverting version is the EL7202C. If inverting drivers are selected then the digital pulse pattern must be inverted in the design stage or if true logic is implemented inverting buffers should be used between the EPLD and the MOSFET drivers. In total 8 drivers are needed. The Elantec drivers are dual channel devices.



*Additional logic is required to gate ALOWCP and ALOWCR prior to the mux control input
Logic selected depends on the active level of the mux control pin.

Figure AA: Generation of A- and B-Pulses

5.5 Synchronization Pulses and Processing Pulses

The EPLD generates the synchronization pulses and the processing pulses. All pulses are buffered using the 74HCT541. The synchronization pulses HD and VD can be used to synchronize a frame grabber or a monitor to the video signal. The processing pulses PB, BLC, and BPC are applied to the processing circuitry. AHIGH, BHIGH and ALOWCR,ALOWCP are switching pulses which affect the image and storage gate levels. The pulse SSC is not buffered, it is applied directly for synchronization with the C1-pulse.

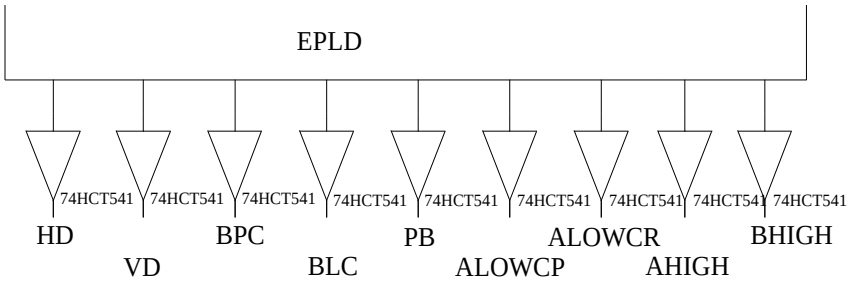


Figure BB: Synchronization / Processing Pulses

6. Sensor DC-Voltages

To generate the sensor DC-voltages low noise operational amplifiers with or without buffering should be used. The voltage levels should neither exceed the minimum nor the maximum value. All voltages have to provide the specified maximum current. No maximum ripple peak to peak value is given in the data sheet, but in general it can be said that the better the voltage performance, the better the sensor performance. All sensor DC-voltages should be decoupled by a 100nF capacitor near the sensor pin. The voltages VNS and VPS need an additional decoupling capacitor of about 1µF.

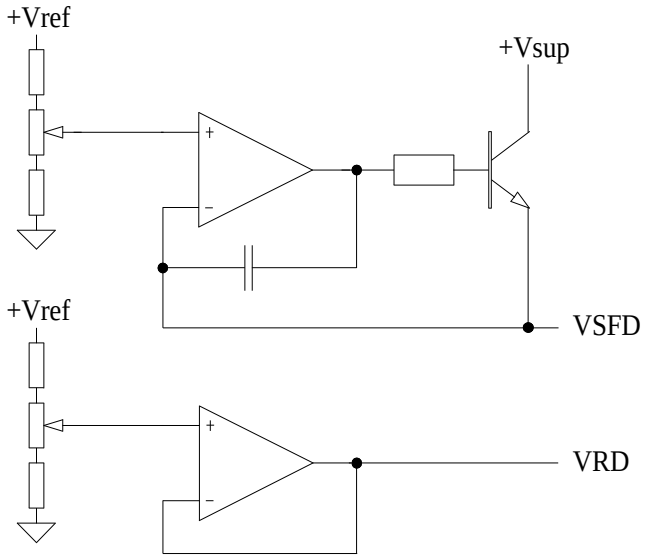


Figure CC: Sensor DC-Voltages

Two possible examples are given. One shows the SFD voltage, which is a high current voltage of some mA's. The other is the RD voltage and therefore a rather low current voltage of several hundred's of µA's. Additional diode protection clamps to guard against violating the minimum and maximum ratings are not shown but recommended..

Caution! Prevent VPS from rising above RD and prevent RD from rising above either SFD or VNS (Nsub). This must also be guaranteed when the power of the camera is switched on. Schottky diodes can be used to clamp the bias voltages to assure the maximum voltage limits are not exceeded.

7. Pre-Processing

The pre-processing can be realized in many different ways. The figures show three different processing techniques, an inverting buffer with a simple low pass filter, a soft clamp pre-processing and a correlated double sampler.

Caution! Never load the output of a sensor directly with remote electronics. Instead use a buffer circuit as close as possible to the sensor output. The pre-processing schematics which follow use a fast transistor and three resistors to construct an emitter follower buffer. Measure the output signal after this stage!

Inverting Amplifier and Low Pass Filter:
The reset and amplifier noise is not suppressed. The performance is rather poor. The low pass filter limits the video bandwidth to 20MHz or half the pixel frequency.

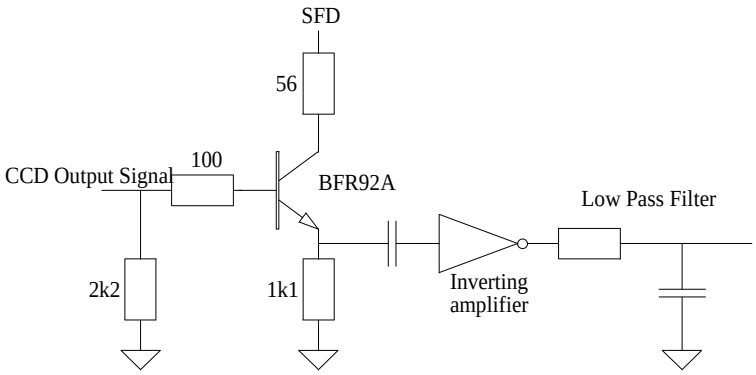


Figure DD: Simple Pre-Processor

Soft-Clamp Pre-processing:
The output is first buffered and then amplified to increase the amplitude of the output signal. The soft-clamp circuitry suppresses 1/f- and reset-noise. This is done by clamping the reset hold level into the series capacitor before the pixel information passes this capacitor. The combination of the low pass filter and notch filter limits the bandwidth of the video signal (pre-processing out) to 20MHz and suppresses the 40MHz clock carrier.

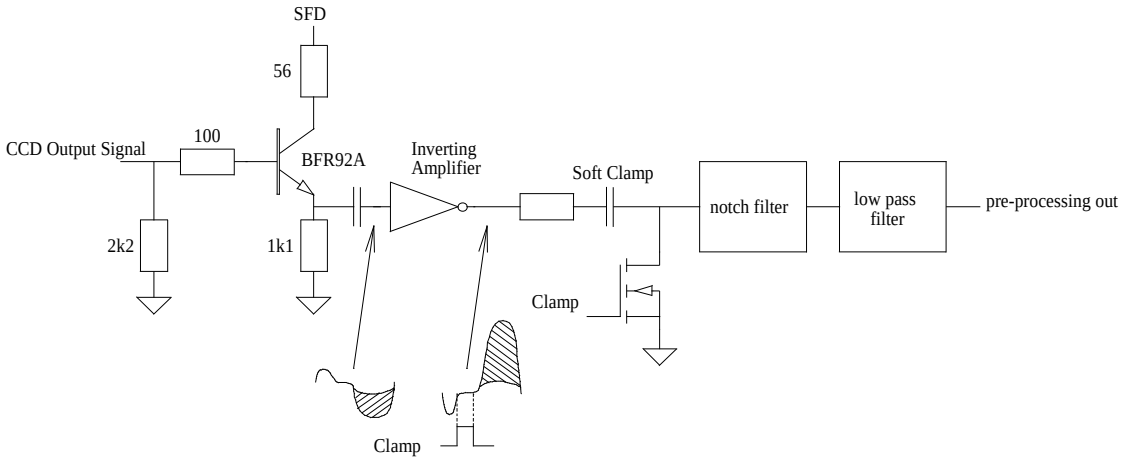


Figure EE: Soft Clamp Pre-Processing

Correlated Double Sampling:

The output signal is first amplified. Then the signal is sampled twice by the correlated double sampler or CDS. The first sample is taken during the reset hold period, the second when the actual signal is present. The op-amp amplifies the difference between the CCD signal output and the reset hold level. In this way the reset noise or cross talk and the 1/f noise are suppressed.

A correlated double sampler is available in chip form from e.g. Kodak (KASP-140G, KASP-305M) as well as from other IC manufacturers. The maximum sampling frequencies of such devices vary, however, some are capable of processing at 40MHz. The exact sample pulse widths and shapes should be obtained from the respective data sheets. CDS functions can always be constructed using discrete devices and / or high speed sampling amplifiers.

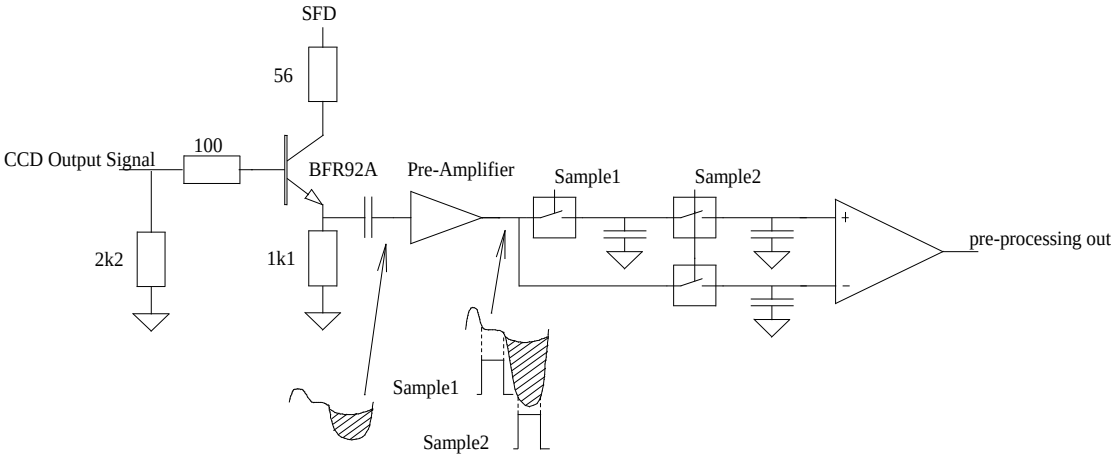


Figure FF: Correlated Double Sampler

8. Post-Processing Block Diagram

The post-processing can be implemented in either analog or in the digital domain. Post processing implementation are functions which tend to be unique for each application, therefore, detailed application information is not given in this application note.

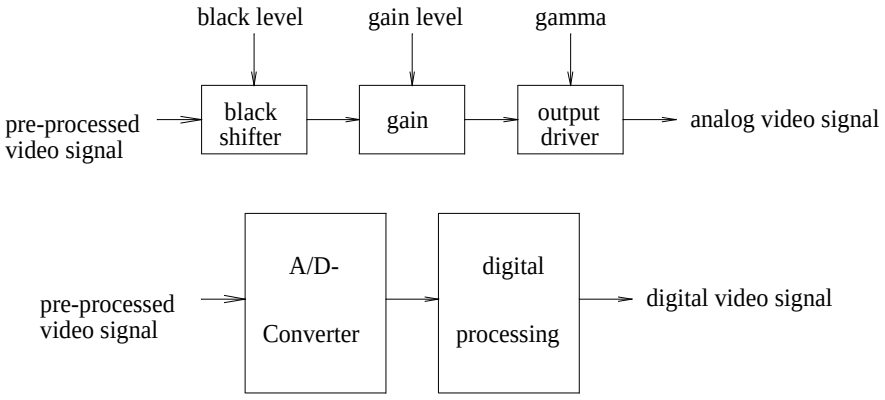


Figure GG: Post-Processing Block Diagram

9. Mechanical Dimensions

Information regarding the pin-out of the FT18 sensor can be found in the data sheet. The figure shown contains critical dimensions which are crucial to centering the optical system relative to the CCD package.

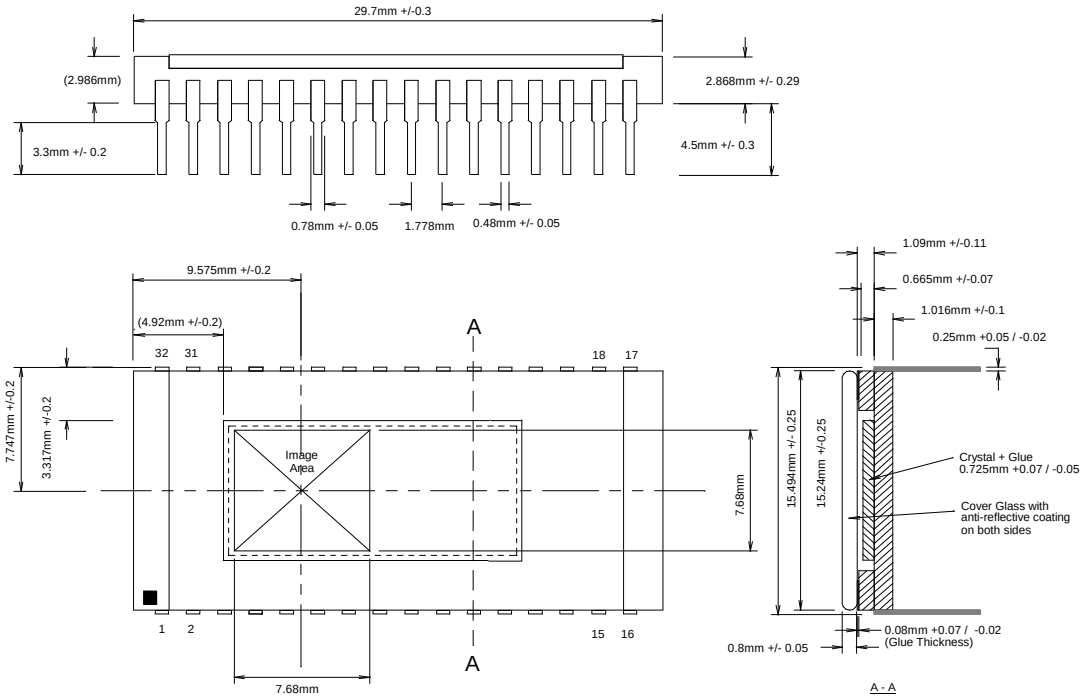


Figure HH: Package Mechanical Dimensions

The optical format of the FT18 is 2/3". The flange distance between the lens and the surface of the CCD depends on the lens used. It is 12.5mm for CS-mount or 17.52mm for C-mount lenses. The distance between the cover glass and the CCD surface is 0.505mm +/- 10%. To compute the flange distance more precisely, the following calculation can be made.

$$f = s + d/3$$

'f' = flange distance, 's' = 12.5mm for CS-mount or 17.52mm for C-mount, 'd' = cover glass thickness

Ideally, the opto-mechanical interface should be designed in a way that it is possible to align the sensor in x- and y-direction with the lens. If this is not possible, then the optical axis of both CCD and lens should be centered as accurately as possible for best imaging results. Assure that the plane of the lens and CCD are parallel. The area between the lens interface and the CCD should be shielded from light and painted black to avoid image contamination due to light reflections.

10. Philips CCD Applications Engineering Support

Philips CCD Applications Engineering support can be obtained at the following facilities. For the United States, Canada, Central and South America please contact Philips Components Group. For Europe, Asia, Africa and Australia contact Philips Professional Imaging.

Philips Semiconductors Image Sensors:

Prof. Holstlaan 4 (WAG 05)
5656 AA Eindhoven
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phone: +31-40-2744418
fax: +31-40-2744090

Philips Components Group (PCG):

- CCD Applications Lab -
100 Providence Pike
Slatersville, RI 02876
USA
phone: +1-401-762-3800
fax: +1-401-767-4493