- **1.8-V Phase Lock Loop Clock Driver for Double Data Rate (DDR II) Applications**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 125 MHz to 400 MHz**
- **Low Jitter (Cycle-Cycle): ±40 ps**
- **Low Static Phase Offset: ±50 ps**
- **Distributes One Differential Clock Input to Ten Differential Outputs**
- **52-Ball μBGA (TI's Micro Star Junior™ BGA, 0.65mm pitch) and 40-Pin MLF**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) are Used to Synchronize the Outputs to the Input Clocks**
- **Single-Ended Input and Single-Ended Output Modes**
- **Meets or Exceeds JEDEC Specification for DDR II Memory PLLs**
- **JEDEC Specification Numbers**

description

The CDCU877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pairs of clock outputs (Yn, $\overline{\text{Yn}}$) and one differential pair of feedback clock output (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS control pins (OE, OS) and the analog power input (AV_{DD}). When OE is low, the clock outputs, except FBOUT/$\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or V_{DD}. When OS is high, OE functions as previously described. When OS and OE are both low, OE has no affect on Y7/$\overline{\text{Y7}}$, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

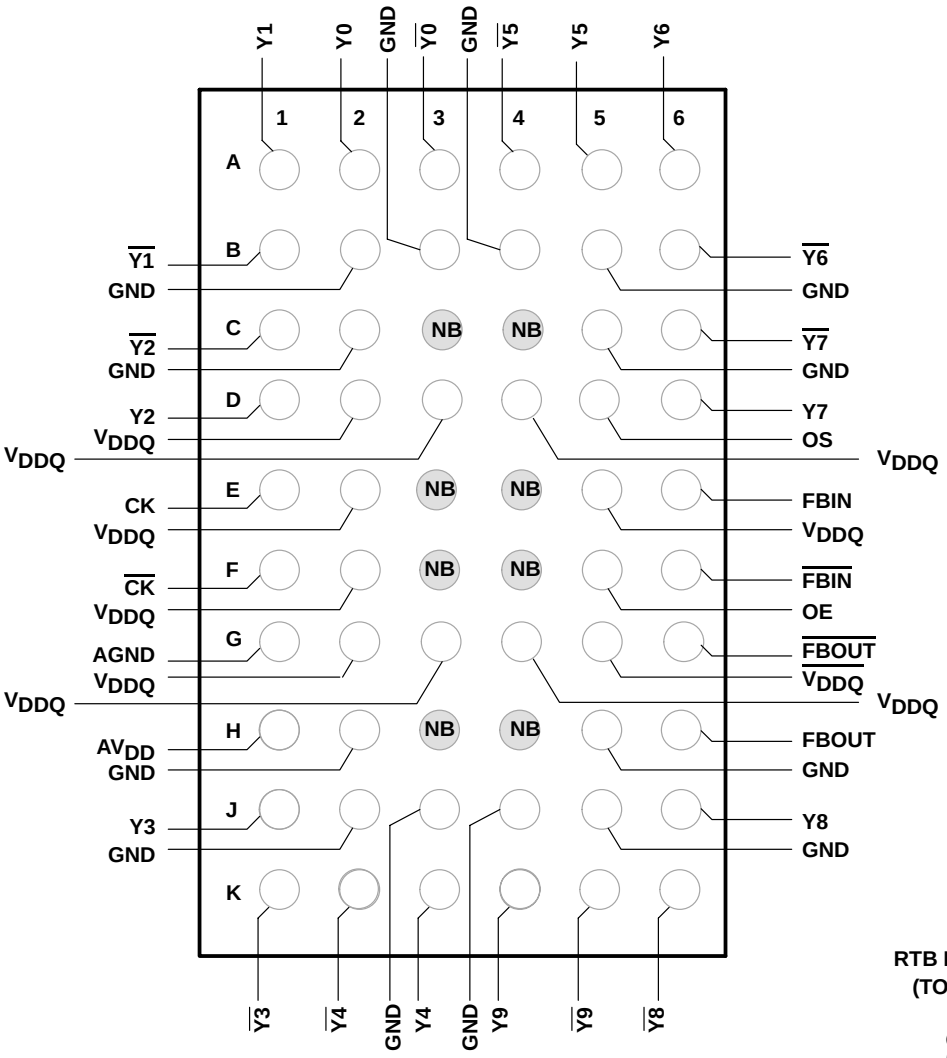
When both clock inputs (CK, $\overline{\text{CK}}$) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the clock input pair (CK, $\overline{\text{CK}}$) within the specified stabilization time.

CDCU877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from –40°C to 85°C

PRODUCT PREVIEW

PRODUCT PREVIEW

MicroStar™ Junior (GQL) Package
(TOP VIEW)



NC – No Connection
NB – No Ball

RTB PACKAGE
(TOP VIEW)

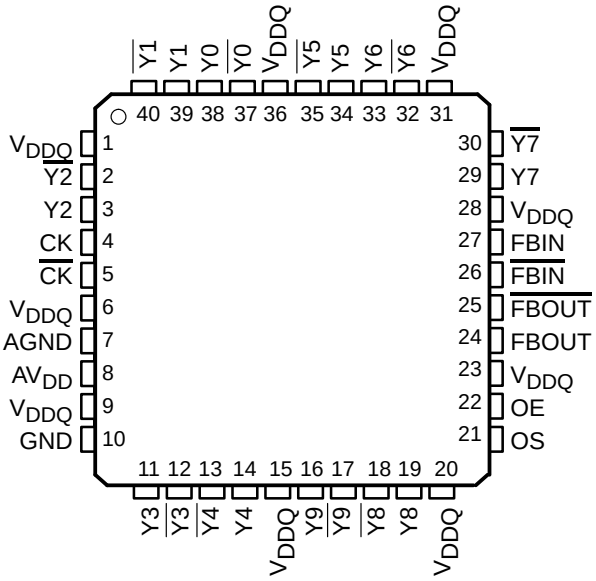


Table 1. Terminal Functions

NAME	BGA	MLF	I/O	DESCRIPTION
AGND	G1	7		Analog ground
AV_{DD}	H1	8		Analog power
CK	E1	4	I	Clock input with a (10 kΩ – 100 kΩ) pull-down resistor
$\overline{CK}$	F1	5	I	Complementary clock input with a (10 kΩ – 100 kΩ) pull-down resistor
FBIN	E6	27	I	Feedback clock input
$\overline{FBIN}$	F6	26	I	Complementary feedback clock input
FBOUT	H6	24	O	Feedback clock output
$\overline{FBOUT}$	G6	25	O	Complementary feedback clock output
OE	F5	22	I	Output enable (asynchronous)
OS	D5	21	I	Output select (tied to GND or V_{DD})
GND	B2, B3, B4, B5, C2, C5, H2, H5, J2, J3, J4, J5	10		Ground
V_{DDQ}	D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36		Logic and output power
Y[0:9]	A2, A1, D1, J1, K3, A5, A6, D6, J6, K4	38, 39, 3, 11, 14, 34, 33, 29, 19, 16	O	Clock outputs
$\overline{Y[0:9]}$	A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	37, 40, 2, 12, 13, 35, 32, 30, 18, 17	O	Complementary clock outputs

Table 2. Function Table

INPUTS					OUTPUTS				PLL
AV_{DD}	OE	OS	CK	$\overline{CK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	H	X	L	H	L	H	L	H	Bypassed/ Off
GND	H	X	H	L	H	L	H	L	Bypassed/ Off
GND	L	H	L	H	L_Z	L_Z	L	H	Bypassed/ Off
GND	L	L	H	L	L_Z Y7 Active	$\overline{L_Z}$ Y7 Active	H	L	Bypassed/ Off
1.8 V Nom	L	H	L	H	L_Z	L_Z	L	H	ON
1.8 V Nom	L	L	H	L	L_Z Y7 Active	$\overline{L_Z}$ Y7 Active	H	L	ON
1.8 V Nom	H	X	L	H	L	H	L	H	ON
1.8 V Nom	H	X	H	L	H	L	H	L	ON
1.8 V Nom	X	X	L	L	L_Z	L_Z	L_Z	L_Z	OFF
X	X	X	H	H	Reserved				

PRODUCT PREVIEW

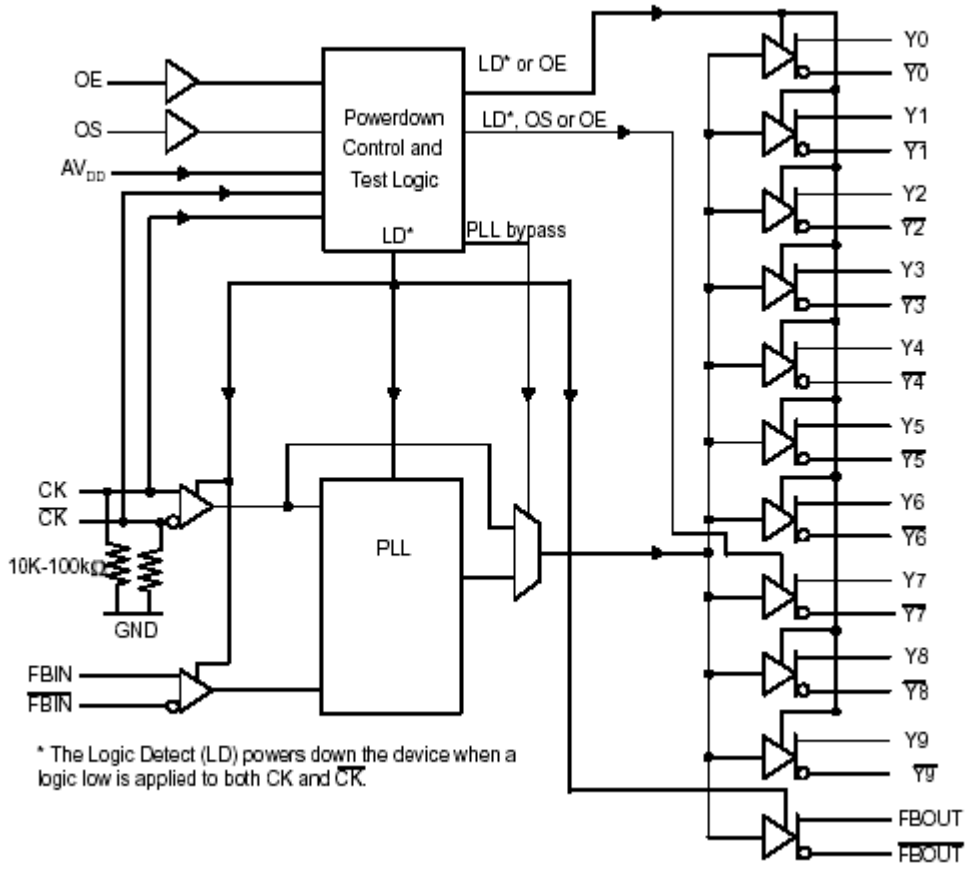


Figure 1. Logic Diagram (Positive Logic)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DDQ} or AV_{DD} . . . . . –0.5 V to 2.5 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ}) . . . . . ±50mA
Output clamp voltage, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50mA
Continuous current through each V_{DDQ} or GND . . . . . ±100mA
Storage temperature range, T_{STG} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed
2. This value is limited to 2.5 V maximum.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{DDQ}	Output supply voltage			1.7	1.8	1.9	V
AV_{DD}	Supply voltage	See Note 1			V_{DDQ}		
V_{IL}	Low-level input voltage (see Note 2)	OE, OS				$0.35 \times V_{DDQ}$	V
V_{IH}	High-level input voltage (see Note 2)	CK, $\overline{CK}$		$0.65 \times V_{DDQ}$			V
I_{OH}	High-level output current (see Figure 2)					–9	mA
I_{OL}	Low-level output current (see Figure 2)					9	mA
V_{IX}	Input differential-pair cross voltage			$(V_{DDQ}/2)$ –0.15		$(V_{DDQ}/2)$+ 0.15	V
V_I	Input voltage level			–0.3		V_{DDQ}+0.3	V
V_{ID}	Input differential voltage (see Note 2 and Figure 9)	DC		0.3		V_{DDQ}+0.4	V
		AC		0.6		V_{DDQ}+0.4	V
T_A	Operating free-air temperature			0		70	°C

NOTE 1: The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and no timing parameters are ensured.
2. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$, see Figure 9 for definition. The CK and $\overline{CK}$ V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	AV_{DD}, V_{DDQ}	MIN	TYP	MAX	UNIT
V_{IK}	Input cl inputs)		I_I = 18 mA	1.7 V			–1.2	V
V_{OH}	High-level output voltage		I_{OH} = –100 μA	1.7 V to 1.9 V	V_{DDQ} – 0.2			V
			I_{OH} = –9 mA	1.7 V	1.1			
V_{OL}	Low-level output voltage		I_{OL} = 100 μA				0.1	V
			I_{OL} = 9 mA	1.7 V			0.6	
$I_{O(DL)}$	Low-level output current, disabled		$V_{O(DL)}$ = 100 mV, OE = L	1.7 V	100			μA
V_{OD}	Differential output voltage (see Note 1)			1.7 V	0.5			V
I_I	Input current	CK, $\overline{CK}$		1.9 V			±250	μA
		OE, OS, FBIN, $\overline{FBIN}$		1.9 V			±10	
$I_{DD(LD)}$	Supply current, static (I_{DDQ} + I_{ADD})		CK and $\overline{CK}$ = L	1.9 V			500	μA
I_{DD}	Supply current, dynamic (I_{DDQ} + I_{ADD}) (see Note 2 for C_{PD} calculation)		CK and $\overline{CK}$ = 270 MHz, All outputs are open (not connected to a PCB)	1.9 V			300	mA
C_I	Input capacitance	CK, $\overline{CK}$	V_I = V_{DD} or GND	1.8 V	2		3	pF
		FBIN, $\overline{FBIN}$	V_I = V_{DD} or GND	1.8 V	2		3	
$C_{I(Δ)}$	Change in input current	CK, $\overline{CK}$	V_I = V_{DD} or GND	1.8 V			0.25	pF
		FBIN, $\overline{FBIN}$	V_I = V_{DD} or GND	1.8 V			0.25	

NOTE 1: V_{OD} is the magnitude of the difference between the true and complimentary outputs. See Figure 9 for a definition.

2. Total $I_{DD} = I_{DDQ} + I_{ADD} = f_{CK} \times C_{PD} \times V_{DDQ}$, solving for $C_{PD} = (I_{DDQ} + I_{ADD})/(f_{CK} \times V_{DDQ})$ where f_{CK} is the input frequency, V_{DDQ} is the power supply, and C_{PD} is the power dissipation capacitance.

timing requirements over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CK}	Clock frequency (operating, see Notes 1 and 2)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V	125		400	MHz
f_{CK}	Clock frequency (application, see Notes 1 and 3)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V	160		370	MHz
	Duty cycle, input clock	AV_{DD}, V_{DD} = 1.8 V ±0.1 V	40%		60%	
t_L	Stabilization time (see Note 4)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V			15	μs

NOTE 1: The PLL must be able to handle spread spectrum induced skew.

2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low speed system debug).
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and $\overline{CK}$ go to a logic low state, enter the power-down mode and later return to active operation. CK and $\overline{CK}$ may be left floating after they have been driven low for one complete clock cycle.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{en}	Enable time, OE to any Y/$\overline{Y}$	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 11			8	ns
t_{dis}	Disable time, OE to any Y/$\overline{Y}$	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 11			8	ns
	Cycle-to-cycle period jitter	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 4	0		40	ps
		AV_{DD}, V_{DD} = 1.8 V ±0.1 V	0		–40	ps
	Static phase offset time (see Note 2)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 5	–50		50	ps
	Dynamic phase offset time	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 10	TBD		TBD	ps
tsk(o)	Output clock skew	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 6			40	ps
	Period jitter (see Note 3)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 7	–40		40	ps
	Half-period jitter (see Notes 3 and 4)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 8	–75		75	ps
SR	Slew rate, OE	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figures 3 and 9	0.5			V/ns
	Input clock skew rate	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figures 3 and 9	1	2.5	4	V/ns
	Output clock slew rate (see Notes 5 and 6)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figures 3 and 9	1.5	2.5	3	V/ns
	Output differential-pair cross voltage (see Note 7)	AV_{DD}, V_{DD} = 1.8 V ±0.1 V, See Figure 2	$(V_{DDQ}/2)$ – 0.1		$(V_{DDQ}/2)$ + 0.1	V
	SSC modulation frequency	AV_{DD}, V_{DD} = 1.8 V ±0.1 V	30		33	kHz
	SSC clock input frequency deviation	AV_{DD}, V_{DD} = 1.8 V ±0.1 V	0%		–0.5%	
	PLL loop bandwidth	AV_{DD}, V_{DD} = 1.8 V ±0.1 V	2			MHz

NOTE 1: There are two different termination that are used with the following tests. The load/board in Figure 2 is used to measure the input and output differential-pair cross voltage only. The load/board in Figure 3 is used to measure all other tests. For consistency, equal length cables should be used.

2. Phase static offset time does not include jitter.
3. Period jitter, half-period jitter specifications are separate specifications that must be met independently of each other.
4. The design target is 60 ps.
5. The output slew rate is determined from the IBIS model into the load shown in Figure 3.
6. To eliminate the impact of input slew rates on static phase offset, the input skew rates of reference clock input CK and CK and feedback clock inputs FBIN and $\overline{FBIN}$ are recommended to be nearly equal. The 2.5-V/ns skew rates are shown as a recommended target. Compliance with these typical values is not mandatory if it can adequately shown that alternative characteristics meet the requirements of the registered DDR2 DIMM application.
7. Output differential-pair cross voltage specified at the DRAM clock input or the test load.

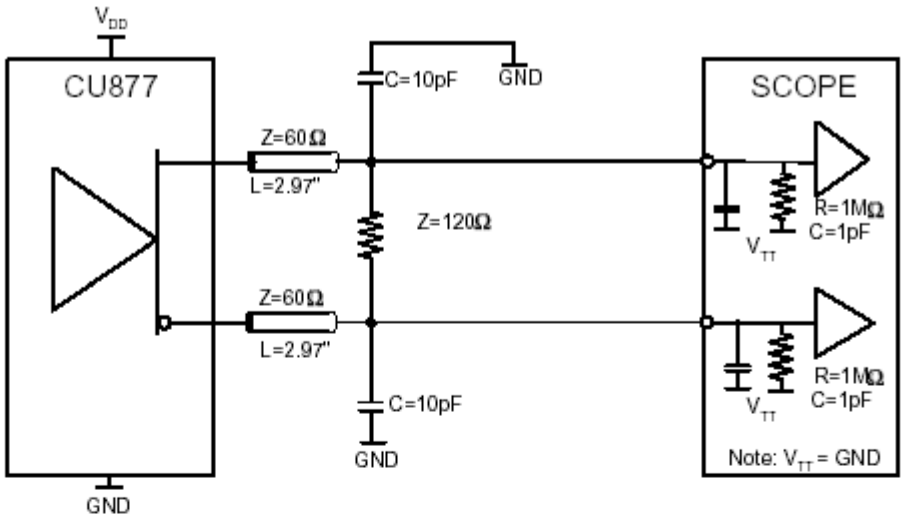


Figure 2. Output Load Test Circuit 1

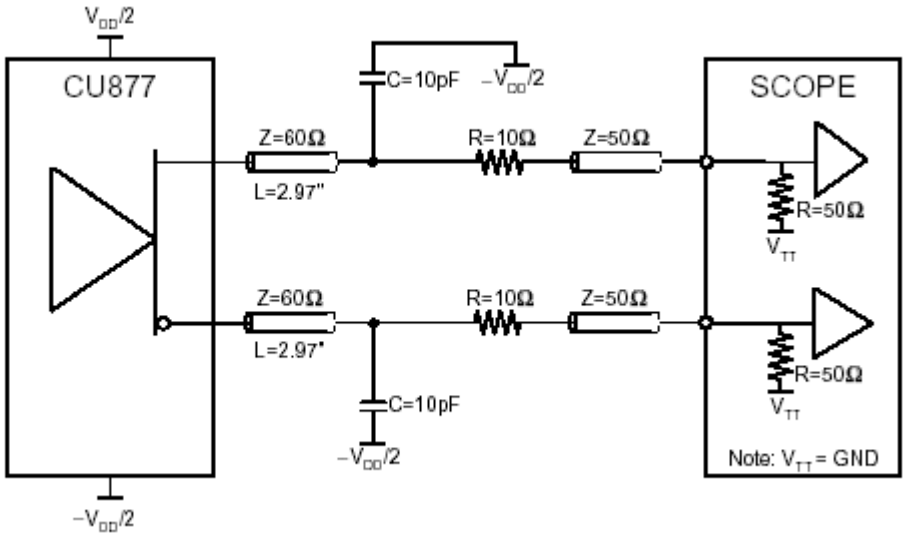


Figure 3. Output Load Test Circuit 2

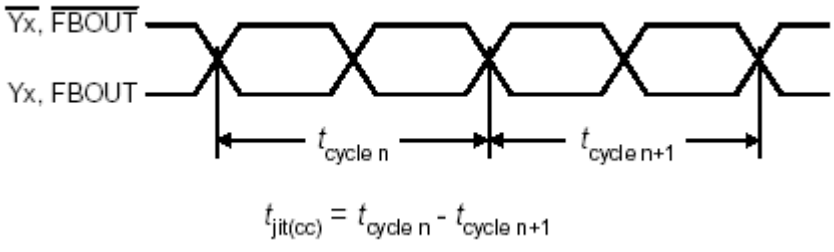
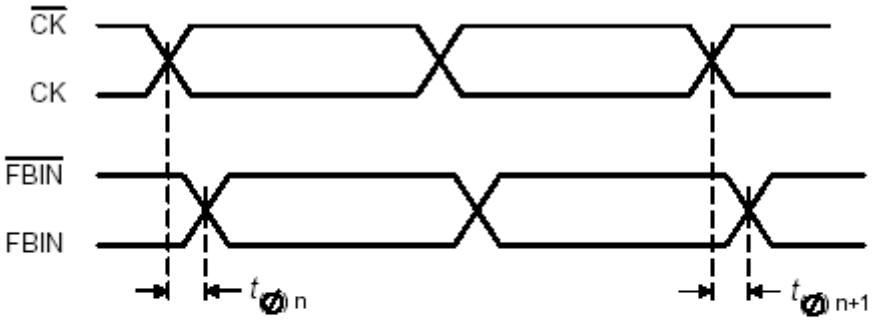


Figure 4. Cycle-To-Cycle Period Jitter



$$t_{\phi} = \frac{\sum_{1}^{n=N} t_{\phi n}}{N}$$

(N is a large number of samples)

(N>1000 samples)

Figure 5. Static Phase Offset

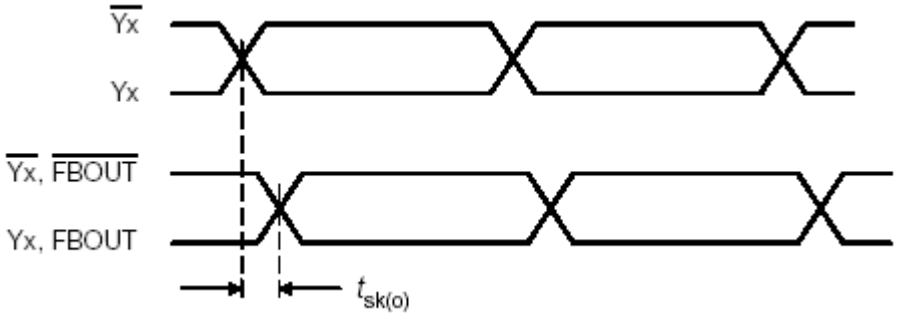
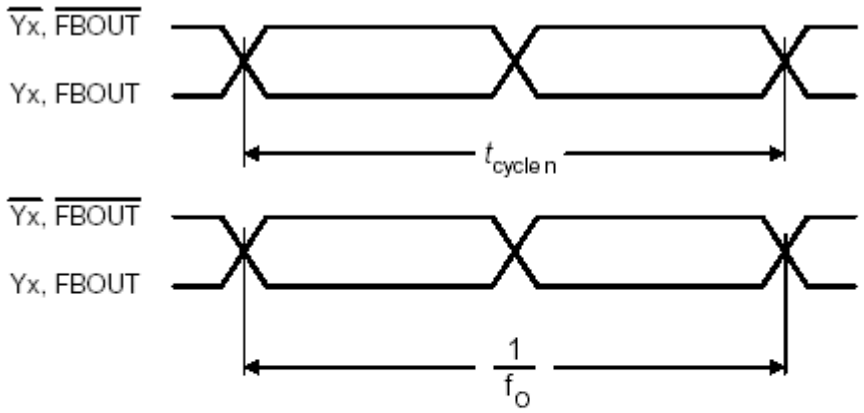


Figure 6. Output Skew

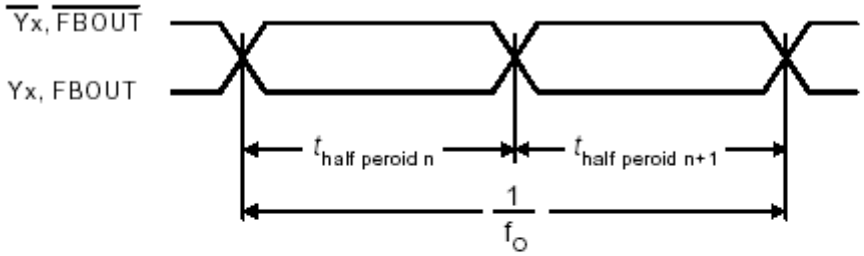
PRODUCT PREVIEW



$$t_{jit(per)} = t_{cycle\ n} - \frac{1}{f_O}$$

(f_O = average input frequency measured at CK/$\overline{CK}$)

Figure 7. Period Jitter



$$t_{jit(hper)} = t_{half\ period\ n} - \frac{1}{2*f_O}$$

n = any half cycle

(f_O = average input frequency measured at CK/$\overline{CK}$)

Figure 8. Half-Period Jitter

PRODUCT PREVIEW

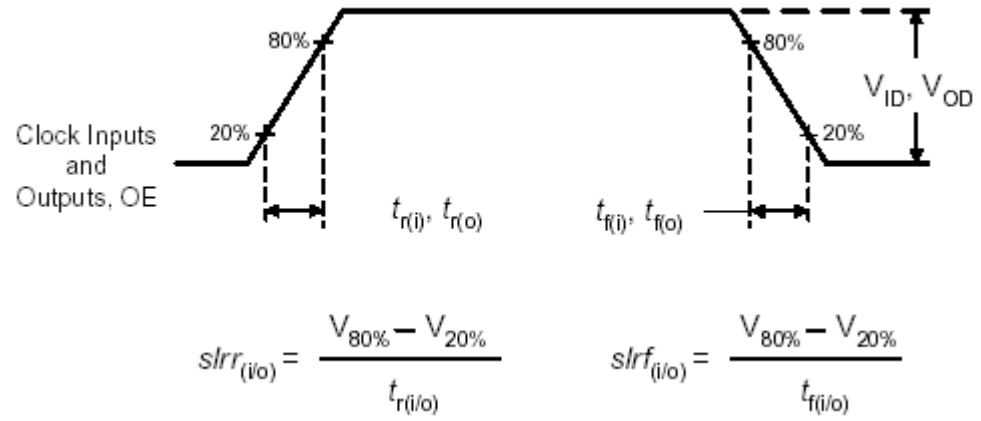


Figure 9. Input and Output Slew Rates

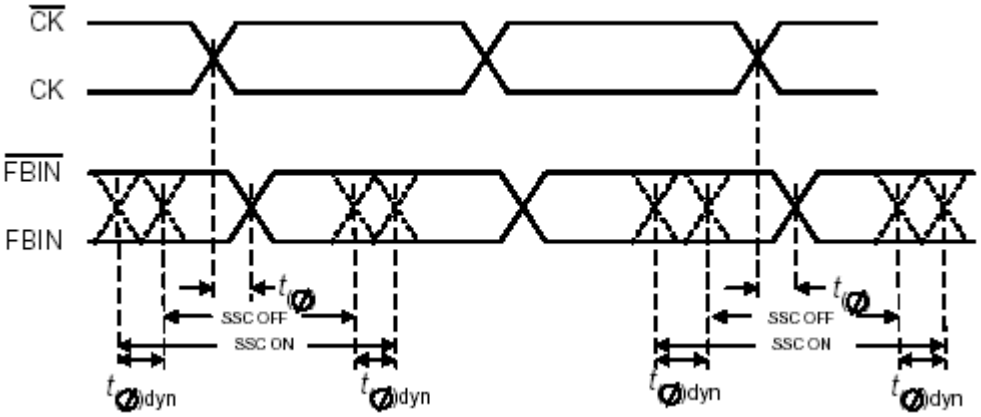


Figure 10. Dynamic Phase Offset

PRODUCT PREVIEW

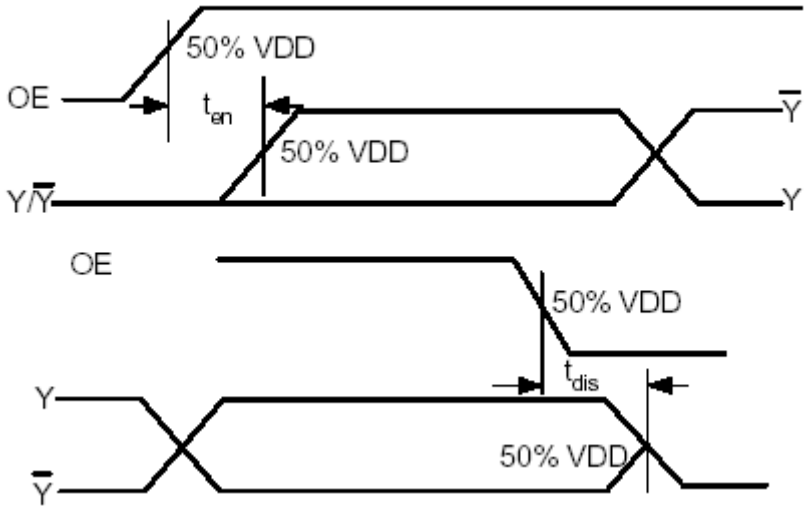
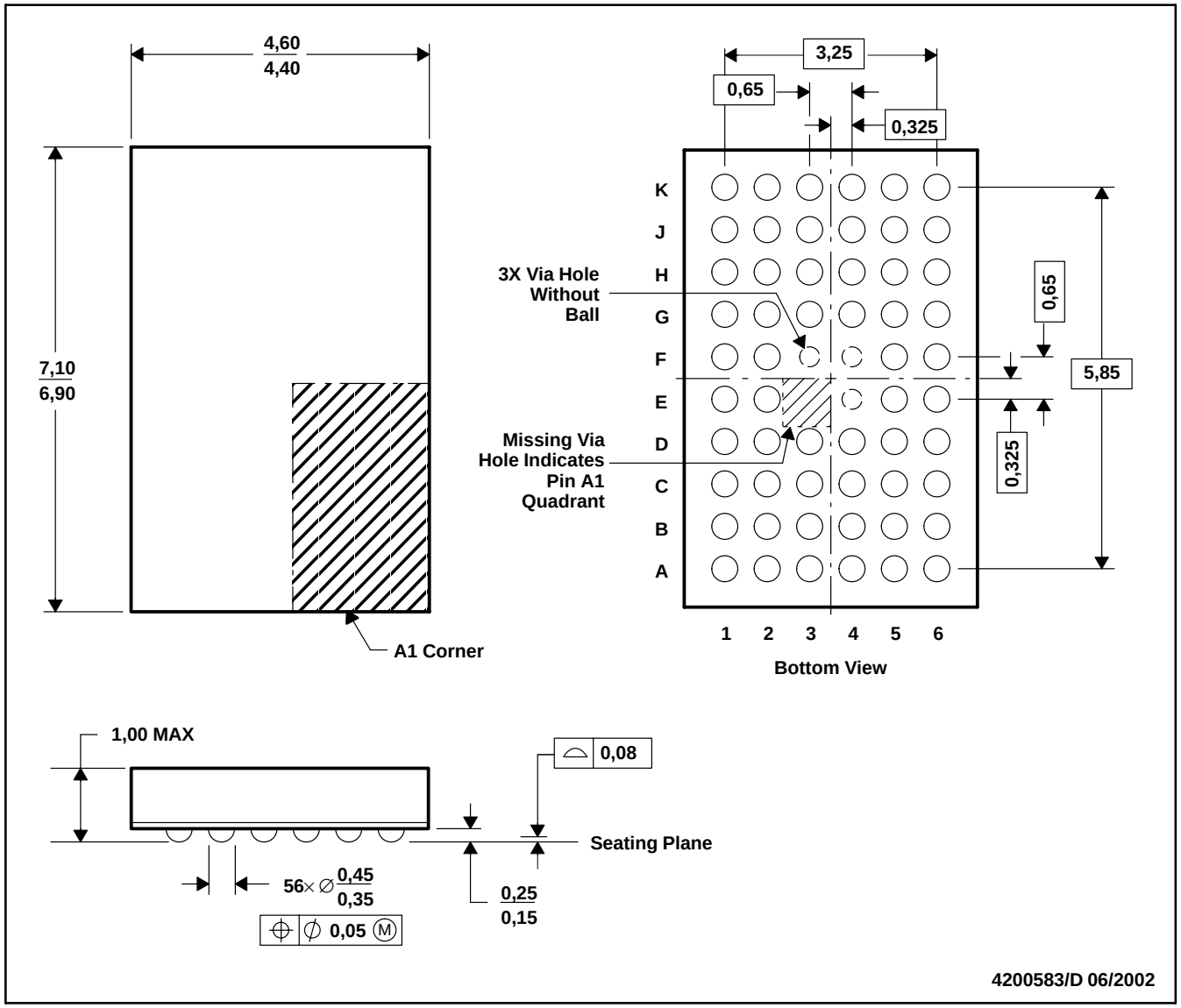


Figure 11. Time Delay Between OE and Clock Output (Y, $\overline{Y}$)

PRODUCT PREVIEW

MECHANICAL DATA

GQL (R-PBGA-N56) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225 variation BA.
E. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

PRODUCT PREVIEW

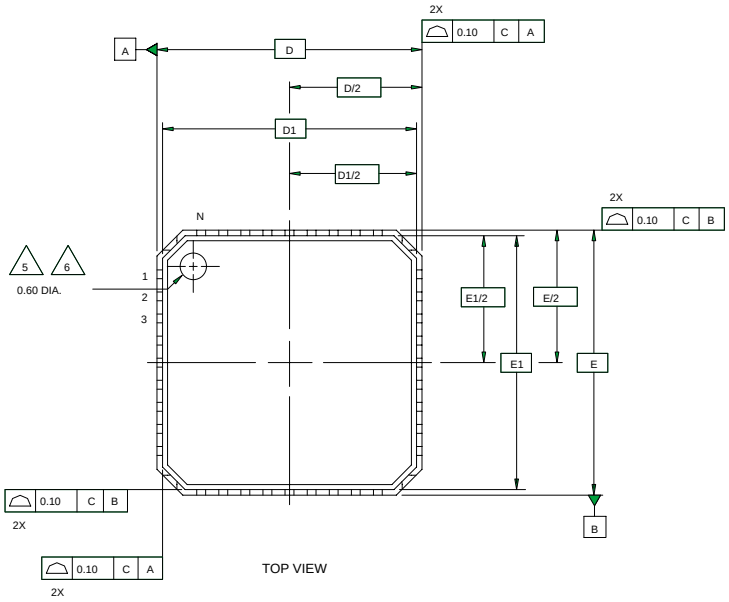
MicroStar Junior is a trademark of Texas Instruments.

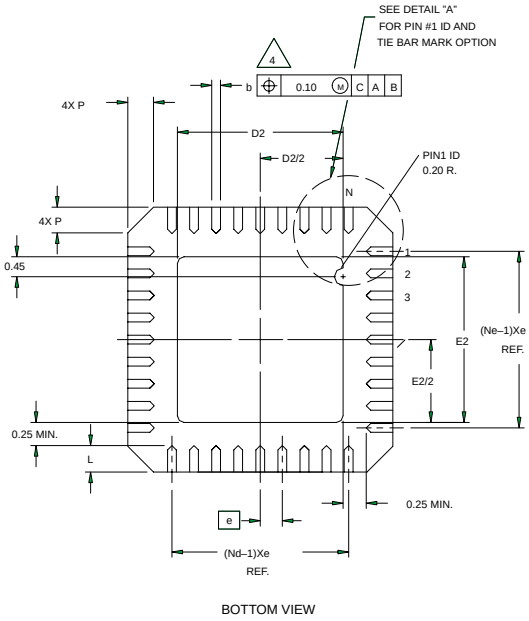
PRODUCT PREVIEW

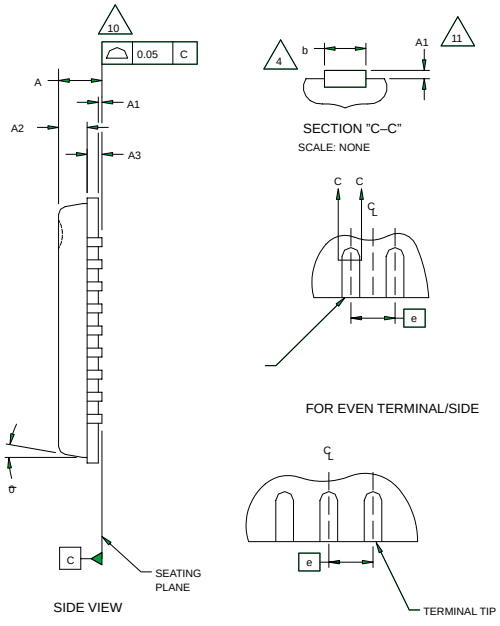
MECHANICAL DATA

RTB (MLF2-N40)

HIGH-DENSITY MATRIX LEADFRAME







SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	0.90	
A1	0.00	0.01	0.05	D
A2	–	0.65	0.80	
A3		0.20 REF.		
D		6.00 BSC		
D1		5.75 BSC		
E		6.00 BSC		
E1		5.75 BSC		
θ			12	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	C

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		40		A
Nd		10		A
Ne		10		A
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	B
Q	0.00	0.20	0.45	C
D2	2.75	2.90	3.05	
E2	2.75	2.90	3.05	

NOTES: A. N is the number of terminals
B. Dimension b applies to the plated terminal and is measured
C. Q and R apply only for the straight tiebar shapes.
D. Applied only for terminals
E. 40-pin HP-VFQFP-N, 6.0 × 6.0 mm body size, 0.5-mm pitch, variation VJJD-2, E2 & D2 = 2.9 mm ±0.15 mm

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