

## MM80C95 • MM80C97 • MM80C98

### 3-STATE Hex Buffers • 3-STATE Hex Inverters

#### General Description

The MM80C95, MM80C97 and MM80C98 gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM80C95 and the MM80C97 convert CMOS or TTL outputs to 3-STATE outputs with no logic inversion, the MM80C98 provides the logical opposite of the input signal. The MM80C95 has common 3-STATE controls for all six devices. The MM80C97 and the MM80C98 have two 3-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to  $V_{CC}$  and GND.

#### Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45  $V_{CC}$  (typ.)
- TTL compatible: Drive 1 TTL Load

#### Applications

- Bus drivers: Typical propagation delay into 150 pF load is 40 ns

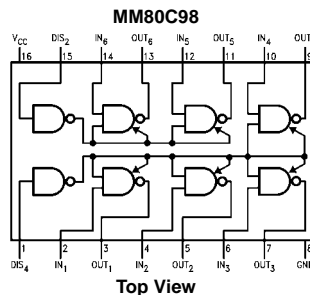
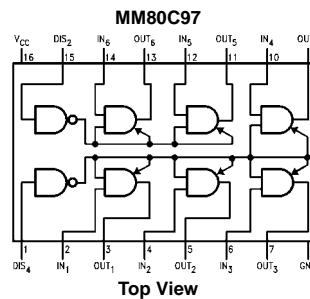
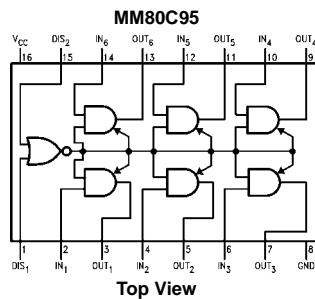
#### Ordering Code:

Order Number	Package Number	Package Description
MM80C95N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM80C97M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM80C97N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM80C98N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

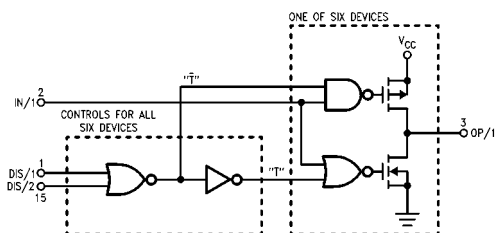
#### Connection Diagrams

##### Pin Assignments for DIP

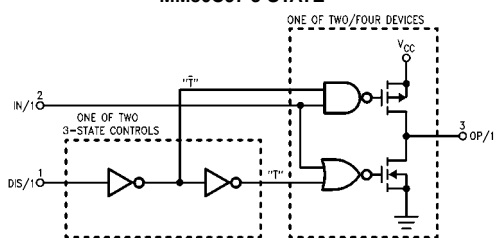


## Schematic Diagrams

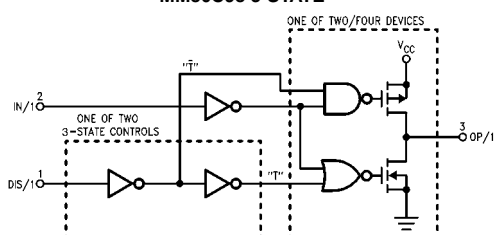
### MM80C95 3-STATE



### MM80C97 3-STATE



### MM80C98 3-STATE



## Truth Tables

### MM80C95

Disable DIS <sub>1</sub>	Input DIS <sub>2</sub>	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

### MM80C97

Disable DIS <sub>4</sub>	Input DIS <sub>2</sub>	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H-z (Note 1)
1	X	X	H-z (Note 2)

### MM80C98

Disable DIS <sub>4</sub>	Input DIS <sub>2</sub>	Input	Output
0	0	0	1
0	0	1	0
X	1	X	H-z (Note 1)
1	X	X	H-z (Note 2)

X = Irrelevant

**Note 1:** Output 5–6 only

**Note 2:** Output 1–4 only

**Absolute Maximum Ratings**(Note 3)

Voltage at Any Pin	−0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW

Power Supply Voltage ( $V_{CC}$ )

18V

Lead Temperature

(Soldering, 10 seconds)

260°C

**Note 3:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

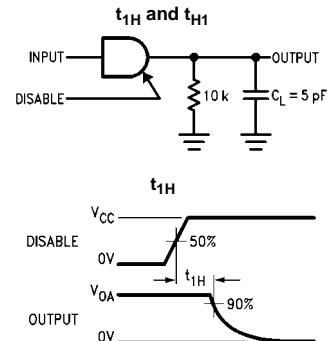
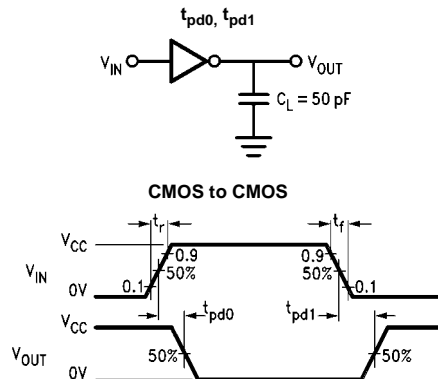
**DC Electrical Characteristics**

Min/Max limits apply across temperature range unless otherwise noted

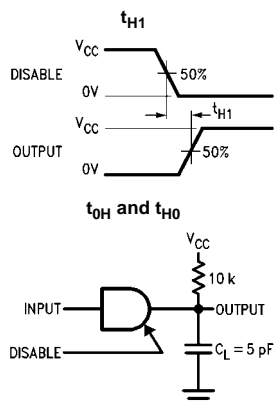
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	−0.005		μA
$I_{OZ}$	Output Current in High Impedance State	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	−1.0	0.005 −0.005	1.0	μA
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.01	15	μA
<b>TTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$ , $I_O = -1.6 \text{ mA}$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$ , $I_O = 1.6 \text{ mA}$			0.4	V
<b>OUTPUT DRIVE (Short Circuit Current)</b>						
$I_{SOURCE}$	Output Source Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25^\circ\text{C}, V_{OUT} = 0V$	−4.35			mA
$I_{SOURCE}$	Output Source Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25^\circ\text{C}, V_{OUT} = 0V$	−20			mA
$I_{SINK}$	Output Sink Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25^\circ\text{C}, V_{OUT} = V_{CC}$	4.35			mA
$I_{SINK}$	Output Sink Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25^\circ\text{C}, V_{OUT} = V_{CC}$	20			mA

**AC Electrical Characteristics** (Note 4) $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0}$ , $t_{pd1}$	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output MM80C95, MM80C97  MM80C98	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		60 25 70 35	100 40 150 75	ns
$t_{pd0}$ , $t_{pd1}$	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output MM80C95, MM80C97  MM80C98	$V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$ $V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$ $V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		85 40 95 45	160 80 210 110	ns
$t_{1H}$ , $t_{0H}$	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0") MM80C95  MM80C97  MM80C98	$R_L = 10\text{k}$ , $C_L = 5\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		80 50 70 50 90 70	135 90 125 90 170 125	ns
$t_{H1}$ , $t_{H0}$	Delay from Disable Input to Logical "1" Level (from High Impedance State) MM80C95  MM80C96  MM80C98	$R_L = 10\text{k}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		120 50 130 60 120 50	200 90 225 110 200 90	ns
$C_{IN}$	Input Capacitance	Any Input (Note 5)		5.0		pF
$C_{OUT}$	Output Capacitance 3-STATE	Any Output (Note 5)		11		pF
$C_{PD}$	Power Dissipation Capacitance	(Note 6)		60		pF

**Note 4:** AC Parameters are guaranteed by DC correlated testing.**Note 5:** Capacitance is guaranteed by periodic testing.**Note 6:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.**AC Test Circuits and Switching Time Waveforms**

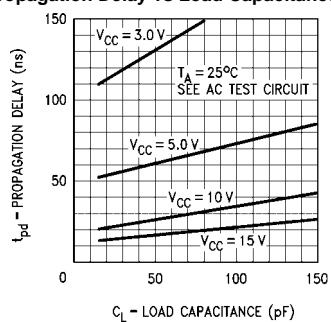
## AC Test Circuits and Switching Time Waveforms (Continued)



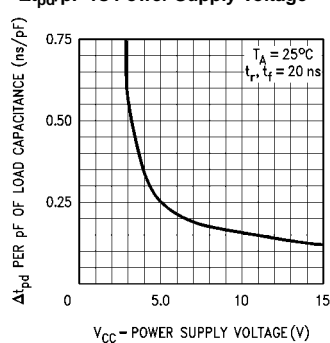
Note: Delays measured with input  $t_r$ ,  $t_f \leq 20$  ns.

## Typical Performance Characteristics

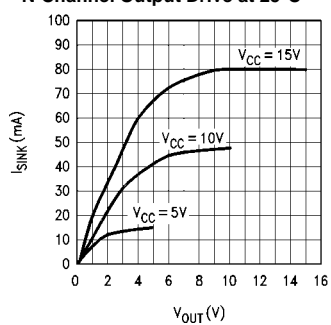
Propagation Delay vs Load Capacitance



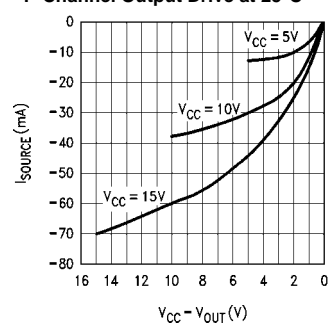
$\Delta t_{pd}/pF$  vs Power Supply Voltage



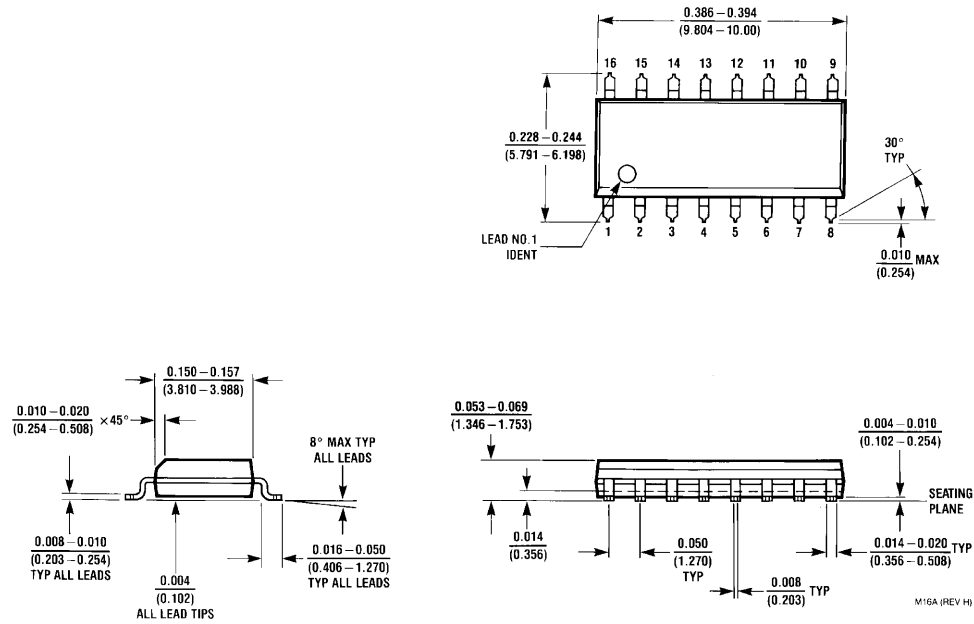
N-Channel Output Drive at  $25^\circ\text{C}$



P-Channel Output Drive at  $25^\circ\text{C}$

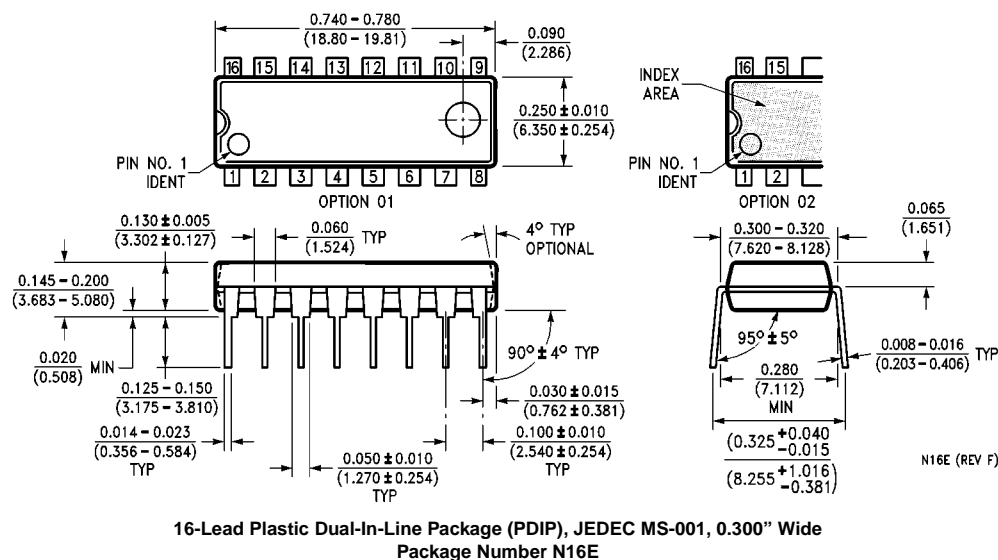


# Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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