DATA SHEET

MAX6400/MAX6401/MAX6402/ MAX6403/MAX6404/MAX6405

Ultra-low-power microprocessor reset circuit in 4-bump Chip-Scale package

Product data

2003 May 27

Philips
Semiconductors

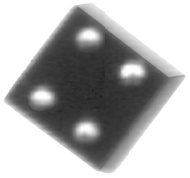
PHILIPS

Ultra-low-power microprocessor reset circuit in 4-bump Chip-Scale package

MAX6400/MAX6401/MAX6402/ MAX6403/MAX6404/MAX6405

DESCRIPTION

The MAX6400/MAX6401//MAX6402/MAX6403/MAX6404/MAX6405 microprocessor (μP) reset circuits monitor power supplies in μP and digital systems. These devices eliminate external components and adjustments while providing excellent circuit reliability and low cost solution. They are used to monitor 2.5 V, 3 V, 3.3 V and 5 V power supplies. A manual reset input is also available.



MAX6400-MAX6405 assert a reset signal when the V_{DD} supply voltage falls below a preset reset threshold voltage. The reset signal remains asserted for at least 100 ms after the V_{DD} rises above the reset threshold. The reset threshold are factory trimmable from 2.2 V to 4.63 V in approximately 100 mV increments. All these parts are guaranteed to assert a reset for V_{DD} down to 1 V. They have excellent immunity to fast transients on V_{DD}.

The devices vary in their output configuration. The MAX6400/MAX6403 have push-pull, active-LOW reset output; while the MAX6402/MAX6405 have open drain, active-LOW reset output. The MAX6401/MAX6404 have push-pull, active-HIGH reset output.

The lower threshold MAX6400/MAX6401/MAX6402 have ultra-low supply current of typically 500 nA, making them ideal for battery powered applications. All six devices are available in the 4-bump Chip-Scale (WL-CSP4) package.

FEATURES

- Ultra-Low 1 μA (max) supply current
- Precision monitoring of 2.5 V, 3 V, 3.3 V, and 5 V power supply voltages
- Reset thresholds available from 2.2 V to 4.63 V
- ±2.5% threshold accuracy from –40 °C to +85 °C
- 100 ms (min) Power-on-Reset delay time
- Manual Reset input
- Power transient immunity
- Available in three versions: push-pull $\overline{\text{RESET}}$, push-pull RESET, and open-drain $\overline{\text{RESET}}$
- Guaranteed reset valid to V_{DD} = 1.0 V
- Ultra-small 4-bump Chip-Scale packages

APPLICATIONS

- PDAs and pagers
- MP3 players
- Portable/battery-powered equipment
- Cellular phones

SIMPLIFIED SYSTEM DIAGRAM

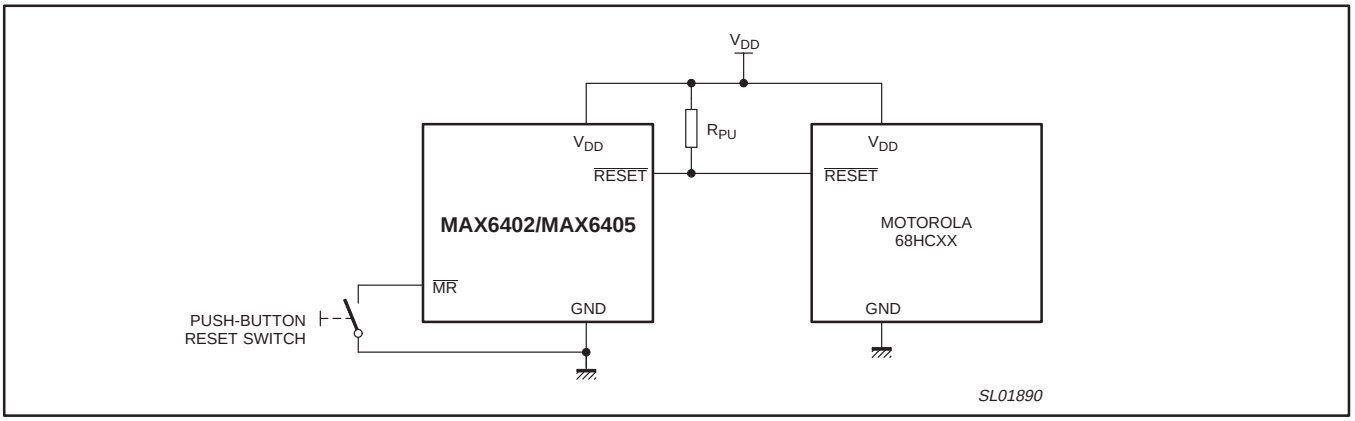


Figure 1. Simplified system diagram.

ORDERING INFORMATION

MAX6400/MAX6401/MAX6402

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
MAX6400-**XX**UK	WL-CSP4	Wafer-level, chip-scale package; 4 bumps; surface mount	–40 °C to +85 °C
MAX6401-**XX**UK	WL-CSP4	Wafer-level, chip-scale package; 4 bumps; surface mount	–40 °C to +85 °C
MAX6402-**XX**UK	WL-CSP4	Wafer-level, chip-scale package; 4 bumps; surface mount	–40 °C to +85 °C

NOTE:
Each device has 5 standard voltage options, indicated by **'XX'** on the 'Type number'.
Additional voltage options may be available (see Table 1 for details).

XX (type number suffix)	Reset threshold voltage (V) (Typical)
22	2.200
23	2.320
26	2.630
29	2.930
31	3.080

MAX6403/MAX6404/MAX6405

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
MAX6403-**XX**UK	WL-CSP4	Wafer-level, chip-scale package; 4 bumps; surface mount	–40 °C to +85 °C
MAX6404-**XX**UK	WL-CSP4	Wafer-level, chip-scale package; 4 bumps; surface mount	–40 °C to +85 °C
MAX6405-**XX**UK	WL-CSP4	Wafer-level, chip-scale package; 4 bumps; surface mount	–40 °C to +85 °C

NOTE:
Each device has 2 standard voltage options, indicated by **'XX'** on the 'Type number'.
Additional voltage options may be available (see Table 1 for details).

XX (type number suffix)	Reset threshold voltage (V) (Typical)
44	4.380
46	4.630

Table 1. Factory-trimmed reset thresholds (note 1)

Part number	Suffix (XX)	Reset Threshold Voltage, V_{th} (V)				
		T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C	
		Min	Typ	Max	Min	Max
MAX6400-**XX**UK MAX6401-**XX**UK MAX6402-**XX**UK	22	2.167	2.200	2.233	2.145	2.250
	23	2.285	2.320	2.355	2.262	2.375
	24 (Note 2)	2.364	2.400	2.436	2.340	2.460
	25 (Note 2)	2.462	2.500	2.537	2.437	2.562
	26	2.591	2.630	2.669	2.564	2.696
	27 (Note 2)	2.660	2.700	2.741	2.633	2.768
	28 (Note 2)	2.758	2.800	2.842	2.730	2.870
	29	2.886	2.930	2.974	2.857	3.000
	30 (Note 2)	2.955	3.000	3.045	2.925	3.075
	31	3.034	3.080	3.126	3.003	3.150
MAX6403-**XX**UK MAX6404-**XX**UK MAX6405-**XX**UK	33 (Note 2)	3.250	3.300	3.350	3.217	3.383
	34 (Note 2)	3.349	3.400	3.451	3.315	3.485
	35 (Note 2)	3.447	3.500	3.552	3.412	3.587
	36 (Note 2)	3.546	3.600	3.654	3.510	3.690
	37 (Note 2)	3.644	3.700	3.755	3.607	3.792
	38 (Note 2)	3.743	3.800	3.857	3.705	3.895
	39 (Note 2)	3.841	3.900	3.958	3.802	3.997
	40 (Note 2)	3.940	4.000	4.060	3.900	4.100
	41 (Note 2)	4.038	4.100	4.161	3.997	4.202
	42 (Note 2)	4.137	4.200	4.263	4.095	4.305
	43 (Note 2)	4.235	4.300	4.364	4.192	4.407
	44	4.314	4.380	4.446	4.270	4.489
	45 (Note 2)	4.432	4.500	4.567	4.387	4.612
	46	4.560	4.630	4.699	4.3514	4.746

NOTES:
1. Factory-trimmed reset thresholds are available in 100 mV increments with ±1.5% tolerance at room temperature.
2. Consult factory for availability.

PINNING

MAX6400/MAX6402/MAX6403/MAX6405

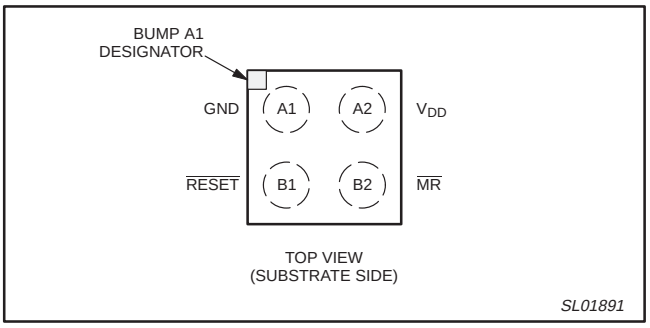


Figure 2. MAX6400/MAX6402/MAX6403/MAX6405 pin configuration.

MAX6401/MAX6404

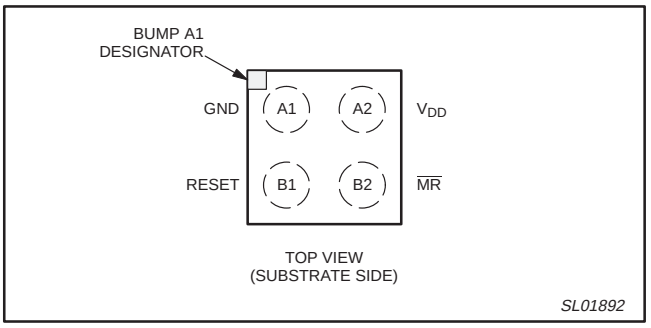


Figure 3. MAX6401/MAX6404 pin configuration.

MAX6400/MAX6402/MAX6403/MAX6405 Pin description

BUMP	SYMBOL	DESCRIPTION
A1	GND	Device ground.
A2	V_{DD}	Positive supply voltage.
B1	$\overline{\text{RESET}}$	Active-LOW Reset output. $\overline{\text{RESET}}$ remains LOW while V_{DD} is below the reset threshold and for a reset delay time of at least 100 ms after V_{DD} rises above the reset threshold. MAX6402/MAX6405 have open-drain output and the MAX6400/MAX6403 are push-pull output.
B2	$\overline{\text{MR}}$	Active-LOW Manual Reset. Internal 50 kΩ pull-up resistor to V_{DD}. Pull LOW to assert a reset condition. As long as $\overline{\text{MR}}$ is LOW, the reset remains asserted. Reset is released in typically 185 ms (reset delay time) after $\overline{\text{MR}}$ goes HIGH. When unused, the $\overline{\text{MR}}$ pin is connected to V_{DD} or left floating.

MAX6401/MAX6404 Pin description

BUMP	SYMBOL	DESCRIPTION
A1	GND	Device ground.
A2	V_{DD}	Positive supply voltage.
B1	RESET	Active-HIGH Reset Output. RESET remains HIGH while V_{DD} is below the reset threshold and remains HIGH for at least 100 ms after V_{DD} rises above the reset threshold.
B2	$\overline{\text{MR}}$	Active-LOW Manual Reset. Internal 50 kΩ pull-up resistor to V_{DD}. Pull LOW to assert a reset condition. As long as $\overline{\text{MR}}$ is LOW, the reset remains asserted. Reset is released in typically 185 ms (reset delay time) after $\overline{\text{MR}}$ goes HIGH. When unused, the $\overline{\text{MR}}$ pin is connected to V_{DD} or left floating.

MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage		–0.3	+6	V
	Voltage RESET, $\overline{\text{RESET}}$ (push-pull)		–0.3	V_{DD} + 0.3	V
	Voltage $\overline{\text{RESET}}$ (open drain)		–0.3	+6	V
	Voltage manual reset, $\overline{\text{MR}}$		–0.3	V_{CC} + 0.3	V
I_{IN}	Input current (any pin)		–	20	mA
I_{OUT}	Output current (any pin)		–	20	mA
T_{amb}	Ambient temperature range		–40	+85	°C
T_{stg}	Storage temperature range		–65	+150	°C
P_D	Power dissipation, 4-bump WL–CSP	Derate 3.8 mW/°C above T_{amb} = 70 °C	–	303	mW

ELECTRICAL CHARACTERISTICS

V_{DD} = full range (T_{amb} = –40 °C to +85 °C) unless otherwise specified. Typical values are at T_{amb} = +25 °C and V_{DD} = 3 V (Note 1).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage range	T_{amb} = 0 °C to +70 °C	1.0	–	5.5	V
		T_{amb} = –40 °C to +85 °C	1.2	–	5.5	V
I_{DD}	Supply current	V_{DD} = 3.0 V for $V_{th} \leq$ 2.93 V; V_{DD} = 3.2 V for $V_{th} \geq$ 2.93 V, no load	–	0.5	1.0	µA
		V_{DD} = 5.5 V, no load	–	1.0	1.75	µA
V_{th}	Reset threshold (see Table 1)	T_{amb} = +25 °C	V_{th} – 1.5%	V_{th}	V_{th} + 1.5%	V
		T_{amb} = –40 °C to +85 °C	V_{th} – 2.5%	V_{th}	V_{th} + 2.5%	V
ΔV_{th}/°C	Reset threshold temperature coefficient		–	40	–	ppm/°C
V_{hys}	Reset threshold hysteresis	MAX6400/MAX6401/MAX6402	–	6.3	–	mV
		MAX6403/MAX6404/MAX6405	–	9.5	–	mV
t_{RD}	V_{DD} to Reset release delay	V_{DD} = (V_{th} + 100 mV) to (V_{th} – 100 mV)	–	20	–	µs
t_{RP}	Reset active time-out period		100	185	280	ms
V_{IL}	LOW-level input voltage on $\overline{MR}$ pin	V_{th} > 4.0 V	–	–	0.8	V
		$V_{th} \leq$ 4.0 V	–	–	0.2 × V_{DD}	V
V_{IH}	HIGH-level input voltage on $\overline{MR}$ pin	V_{th} > 4.0 V	2.0	–	–	V
		$V_{th} \leq$ 4.0 V	0.7 × V_{DD}	–	–	V
t_{MD}	$\overline{MR}$ minimum input pulse width		1	–	–	µs
	$\overline{MR}$ glitch rejection		–	100	–	ns
t_{MR}	$\overline{MR}$ to Reset time delay		–	200	–	ns
	$\overline{MR}$ pull-up resistance		25	50	75	kΩ
$V_{OL(\overline{RESET})}$	LOW-level output voltage on $\overline{RESET}$ pin (MAX6400/MAX6402/ MAX6403/MAX6405)	I_{SINK} = 1.6 mA; V_{DD} > 2.1 V; $\overline{RESET}$ asserted	–	–	0.3	V
		I_{SINK} = 100 µA; V_{DD} > 2.1 V; $\overline{RESET}$ asserted	–	–	0.4	V
$V_{OH(\overline{RESET})}$	HIGH-level output voltage on $\overline{RESET}$ pin (MAX6400/MAX6403)	I_{SOURCE} = 500 µA; V_{DD} = 3.2 V; MAX6400 only; $\overline{RESET}$ released	0.8 × V_{DD}	–	–	V
		I_{SOURCE} = 800 µA; V_{DD} = 4.5 V; $V_{th} \leq$ 4.38 V; $\overline{RESET}$ released	0.8 × V_{DD}	–	–	V
		I_{SOURCE} = 800 µA; V_{DD} = $V_{th(max)}$; $V_{th} \geq$ 4.5 V; $\overline{RESET}$ released	0.8 × V_{DD}	–	–	V
$V_{OH(RESET)}$	HIGH-level output voltage on RESET pin (MAX6401/MAX6404)	I_{SOURCE} = 500 µA; $V_{DD} \geq$ 2.1 V; RESET asserted	0.8 × V_{DD}	–	–	V
		I_{SOURCE} = 50 µA; $V_{DD} \geq$ 1.2 V; RESET asserted	0.8 × V_{DD}	–	–	V
$V_{OL(RESET)}$	LOW-level output voltage on RESET pin (MAX6401/MAX6404)	I_{SINK} = 1.2 mA, $V_{DD} \geq$ 3.2 V; RESET released; MAX6401 only	–	–	0.3	V
		I_{SINK} = 3.2 mA, $V_{DD} \geq$ 4.5 V; $V_{th} \leq$ 4.38 V; RESET released	–	–	0.4	V
		I_{SINK} = 3.2 mA, V_{DD} = $V_{th(max)}$; Vth ≥ 4.5 V; RESET released	–	–	0.4	V
	Open drain $\overline{RESET}$ output leakage current (Note 2)	$\overline{RESET}$ released	–	–	0.1	µA

NOTES:
1. Over-temperature limits are guaranteed by design and are not production tested.
2. Guaranteed by design; not production tested.

TIMING DIAGRAM

The timing diagram in Figure 4 depicts the operation of the device. Letters indicate events on the TIME axis.

On power-up, when V_{DD} reaches 1 V, $\overline{RESET}$ is guaranteed to be a logic LOW.

At Event A, V_{DD} rises to reset threshold voltage, V_{th}. At this time, the internal reset delay timer is initiated. $\overline{RESET}$ and remains asserted for a reset delay time, t_{RP} of typically 180 ms after the supply voltage rises above the reset threshold, V_{th}.

Event B: At this time, the reset is released. $\overline{RESET}$ goes HIGH. The reset delay time helps to ensure valid reset signals with erratic changes in supply voltage.

Events C–E: At Event C, under brown-out conditions, V_{DD} falls below the reset threshold minus the hysteresis voltage, V_{hys}, the reset signal is asserted. When power recovers and V_{DD} rises above the reset threshold, it once again initiates the reset delay timer (Event D). At Event E, V_{DD} falls below the reset threshold before the reset delay time is reached, and reset remains asserted.

At F, the V_{DD} rises above the reset threshold and remains above the reset threshold for typically 185 ms. At G, the reset is once again released.

At H, the $\overline{MR}$ is externally pulled LOW for greater than 1 µs (minimum $\overline{MR}$ pulse width, t_{MD} for V_{DD} = +5 V).

At I, the manual reset is asserted in 200 ns (typical $\overline{MR}$ to reset out delay time, t_{MR} for V_{CC} = +5 V).

At J, the $\overline{MR}$ pin returns HIGH. At this point, reset delay timer is initiated and in typically 180 ms (at K), the reset condition is released.

Event L: On power-down, when V_{DD} falls below $V_{th} – V_{hys}$, $\overline{RESET}$ is guaranteed to be asserted until V_{DD} falls below 1 V.

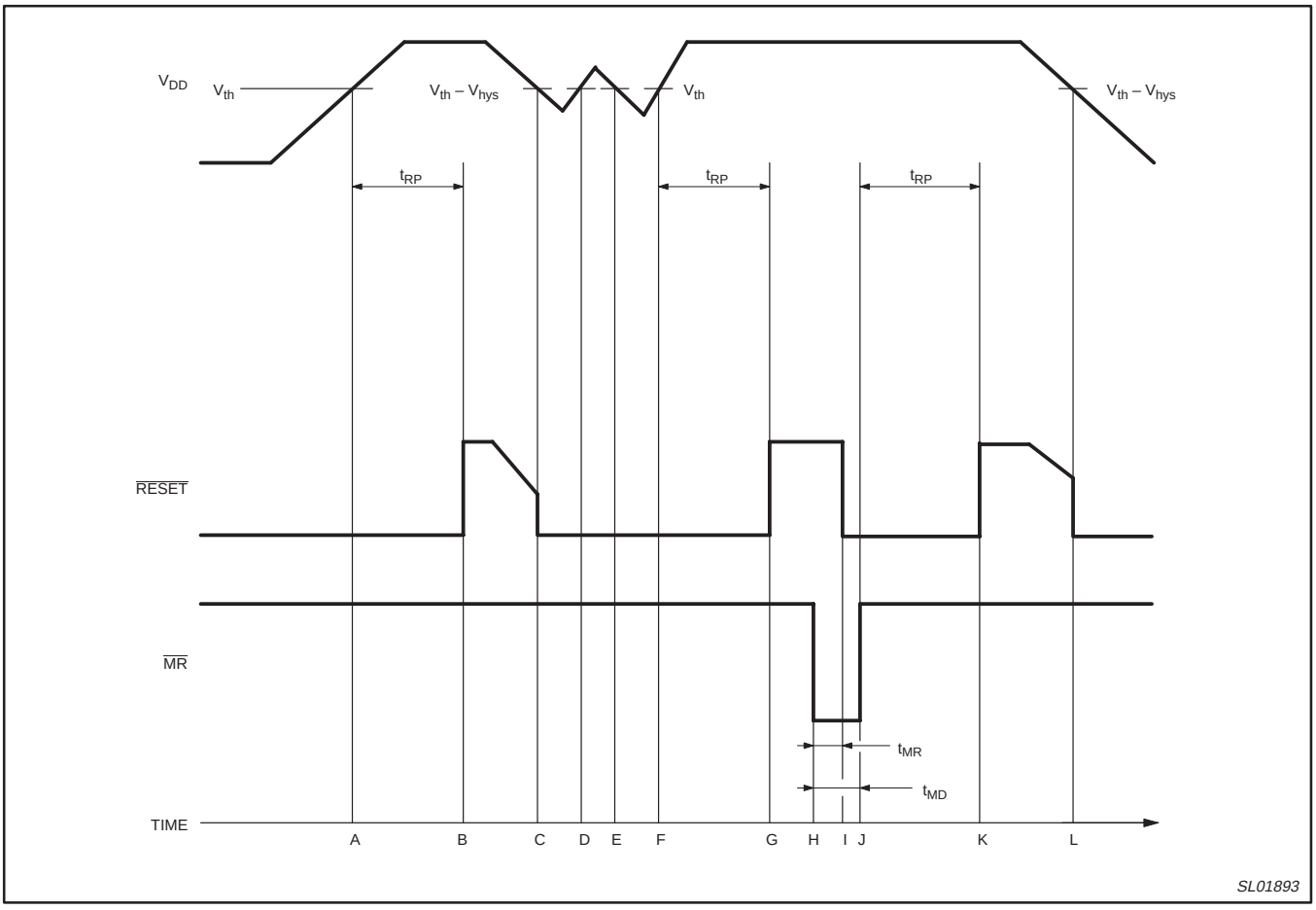


Figure 4. Timing diagram.

TECHNICAL DISCUSSION

General discussion

MAX6400–MAX6405 microprocessor (μP) supervisory ICs provide system protection by monitoring power supply voltage and asserting a reset signal if the supply falls below the specified threshold. The MAX6402/MAX6405 have an active-LOW open drain output. The MAX6400/MAX6403 have an active-LOW, push-pull output; while the MAX6401/MAX6404 have an active-HIGH, push-pull output. The reset state is guaranteed to remain valid as long as V_{DD} is above +1 V.

Threshold levels

The reset threshold voltages are factory trimmable from 2.2 V to 4.63 V in approximately 100 mV increments. Sample stock is available for all standard threshold voltages shown in Table 1, “Factory-trimmed reset thresholds”. Guaranteed threshold voltage tolerance is ±1.5% at T_{amb} = 25 °C and ±2.5% over the operating ambient temperature, T_{amb} = –40 °C to +85 °C.

Manual Reset

The manual reset input, $\overline{MR}$ is active-LOW logic. It allows the $\overline{RESET}$ to be asserted by a pushbutton switch. A mechanical pushbutton switch is effectively debounced by the glitch filter. The typical glitch rejection is 100 ns. $\overline{MR}$ may be driven from an external logic circuit since it is TTL/CMOS compatible. The minimum $\overline{MR}$ input pulse is 1 μs for V_{DD} = +1.2 V to +5.5 V. When not in use, the pin is left floating or tied to V_{DD}.

APPLICATION INFORMATION

Interfacing to µPs with bi-directional reset pins

The MAX6402/MAX6405 RESET outputs are open drain and are easily interfaced with microprocessors which have bi-directional reset pins, such as the Motorola 68HC11. Directly connecting the MAX6402/MAX6405 RESET output to the µP's reset input and providing a pull-up resistor to V_{DD} allows either device to independently assert reset (Figure 5).

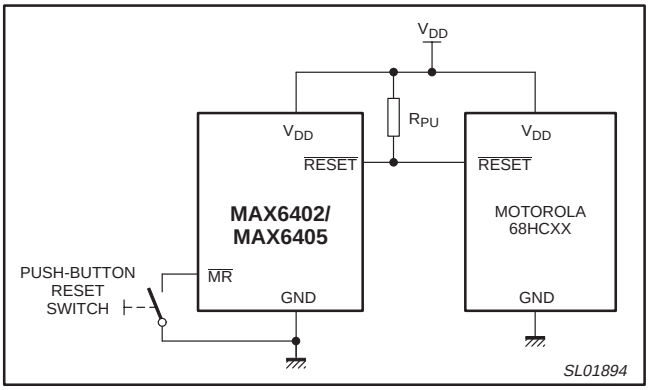


Figure 5. Interfacing to µPs with bi-directional reset pins.

Negative-going V_{DD} transients

The MAX6400–MAX6405 Series resets are relatively immune to short duration, negative-going V_{DD} transients or power glitches. This capability greatly reduces false resets with short -duration pulses.

Figure 6, "Maximum transient duration versus reset comparator overdrive" shows the maximum transient condition for which reset signals are not generated. The graph shows the maximum pulse width that a negative-going transient may have before it will generate a reset signal. **Note:** as the amplitude of the transient increases, the maximum allowable transient pulse width decreases.

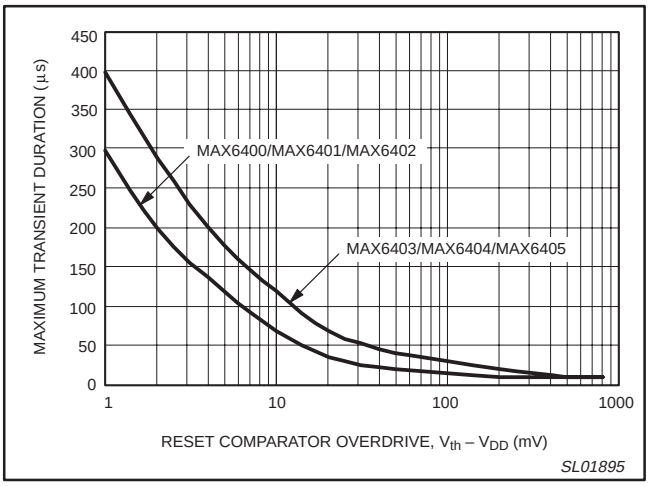
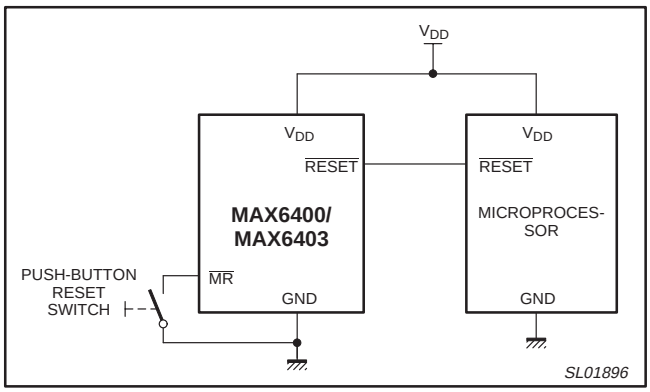


Figure 6. Maximum transient duration versus reset comparator overdrive.

System configurations with various µPs

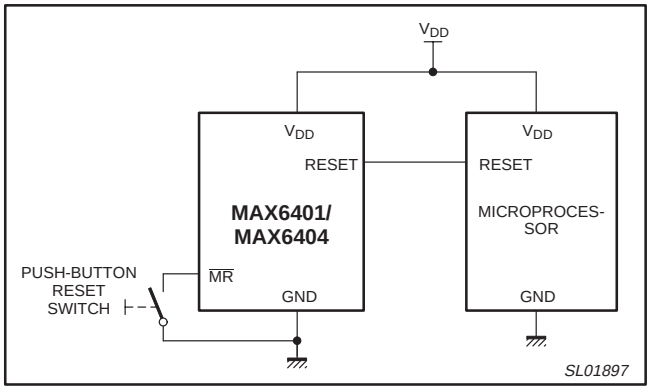
The MAX6400–MAX6405 Series resets provide a system solution for various µPs. Figures 7 and 8, respectively, reference the Philips µPs which are compatible with the MAX6400/MAX6403 and MAX6401/MAX6404 system resets.



NOTE:

1. Philips microprocessors with active-LOW resets: All 16-bit devices from the XA family (XA-Cxx, XA-Gxx, XA-Sxx, XA-Hxx), all LPC7xx devices (P87LPC760/761/762/767/768/769, P80C591/P87C591 (with on-chip CAN controller).

Figure 7. µP system diagram using MAX6400/MAX6403 push-pull, active-LOW resets.



NOTE:

1. Philips microprocessors with active-HIGH resets: 8xC5x, 8xC3x, 8xC5xX2, 8xC3xX2, 8xC51Fx, 8xC51Rx+, 89C51Rx2, 89C66x, 8xC554, 8xC552, etc.

Figure 8. µP system diagram using MAX6401/MAX6404 push-pull, active-HIGH resets.

PACKING METHOD

The MAX6401–MAX6405 Series are packed in reels, as shown in Figure 9.

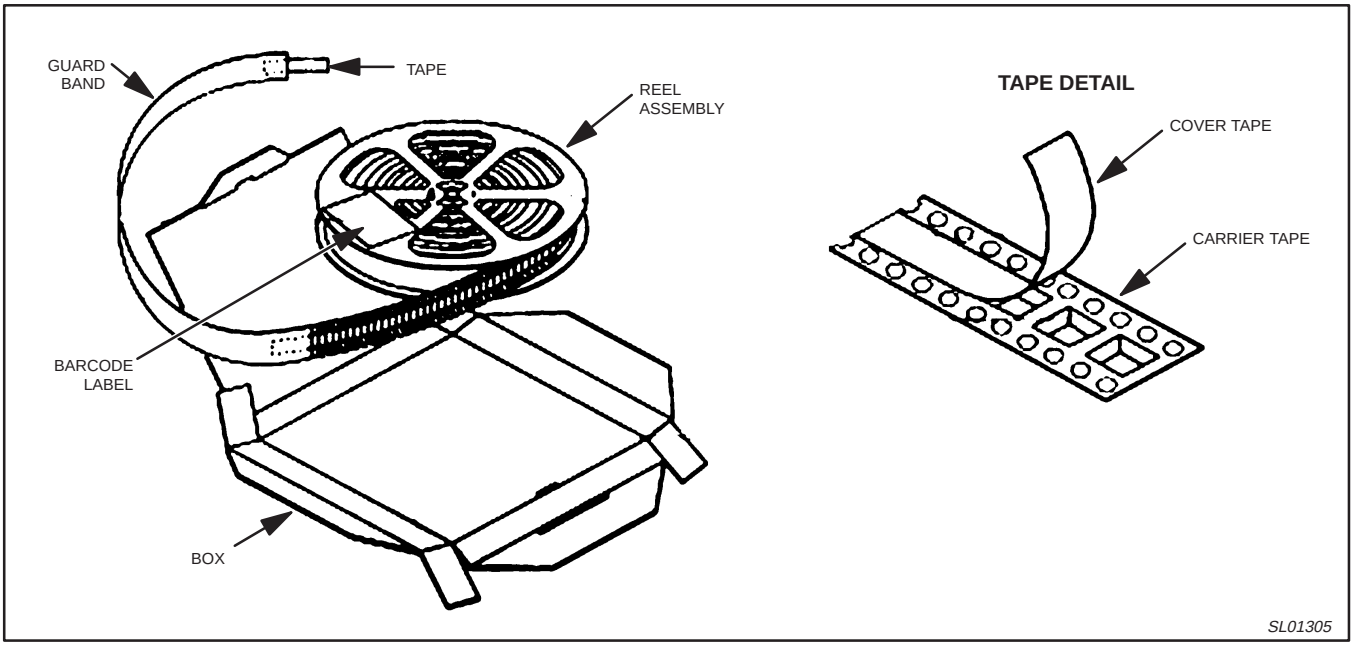
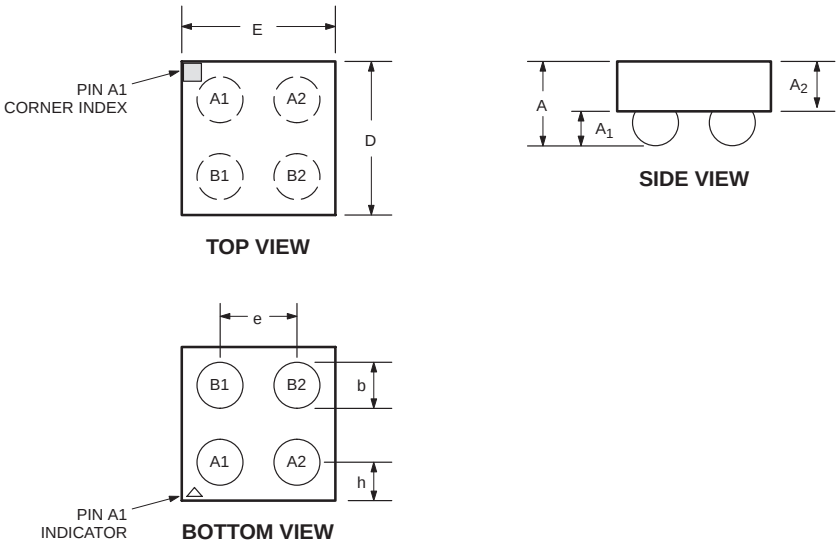


Figure 9. Tape and reel packing method.

WL-CSP4: wafer level, chip-scale package; 4 bumps



DIMENSIONS

UNIT	A	A_1	A_2	b	D	E	e	h
inch	0.024 0.020	ϕ 0.009 ±0.0015	0.013 reference	0.0120 BASIC	0.042 0.038	0.042 0.038	0.0197 BASIC	0.010 reference

Meets JEDEC MO195.

REVISION HISTORY

Rev	Date	Description
_1	20030527	**Product data (9397 750 10644); ECN 853-2428 29962 of 27 May 2003**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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