CMOS 0 to 36 MHz Single Chip 8–bit Microcontroller

1. Description

TEMIC's 80C52 and 80C32 are high performance CMOS versions of the 8052/8032 NMOS single chip 8 bit Microcontroller.

The fully static design of the TEMIC 80C52/80C32 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The 80C52 retains all the features of the 8052: 8 K bytes of ROM; 256 bytes of RAM; 32 I/O lines; three 16 bit timers; a 6-source, 2-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuits. In addition, the 80C52 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial port and the interrupt system continue to function. In the power down mode the RAM is saved and all other functions are inoperative.

The 80C32 is identical to the 80C52 except that it has no on-chip ROM. TEMIC's 80C52/80C32 are manufactured using SCMOS process which allows them to run from 0 up to 36 MHz with VCC = 5 V.

- 80C32: Romless version of the 80C52
- 80C32/80C52-12: 0 to 12 MHz
- 80C32/80C52-30: 0 to 30 MHz
- 80C32/80C52-36: 0 to 36 MHz
- 80C32E-30: 0 to 30 MHz Radiation Tolerant

2. Features

- Power control modes
- 256 bytes of RAM
- 8 Kbytes of ROM (80C52)
- 32 programmable I/O lines
- Three 16 bit timer/counters
- 64 K program memory space
- 64 K data memory space

3. Interface

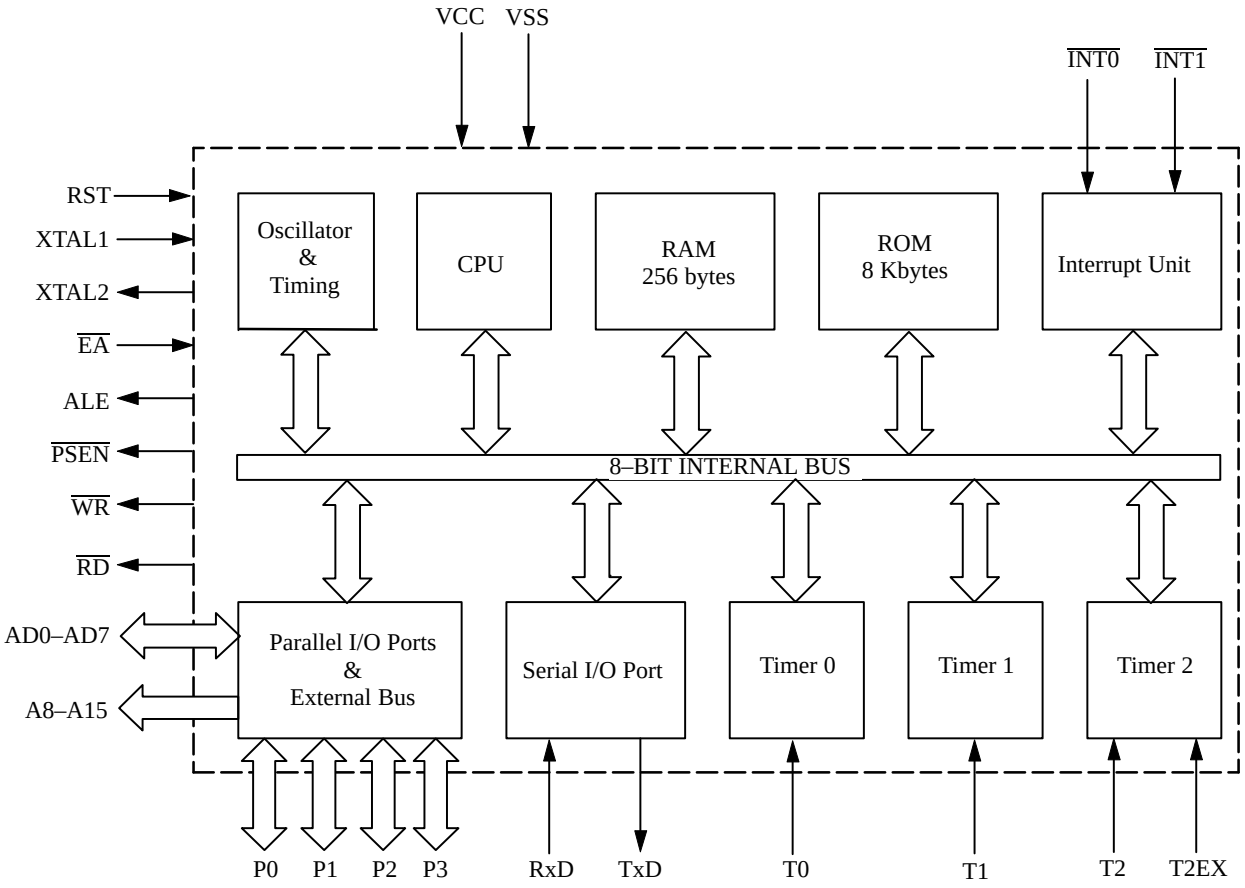
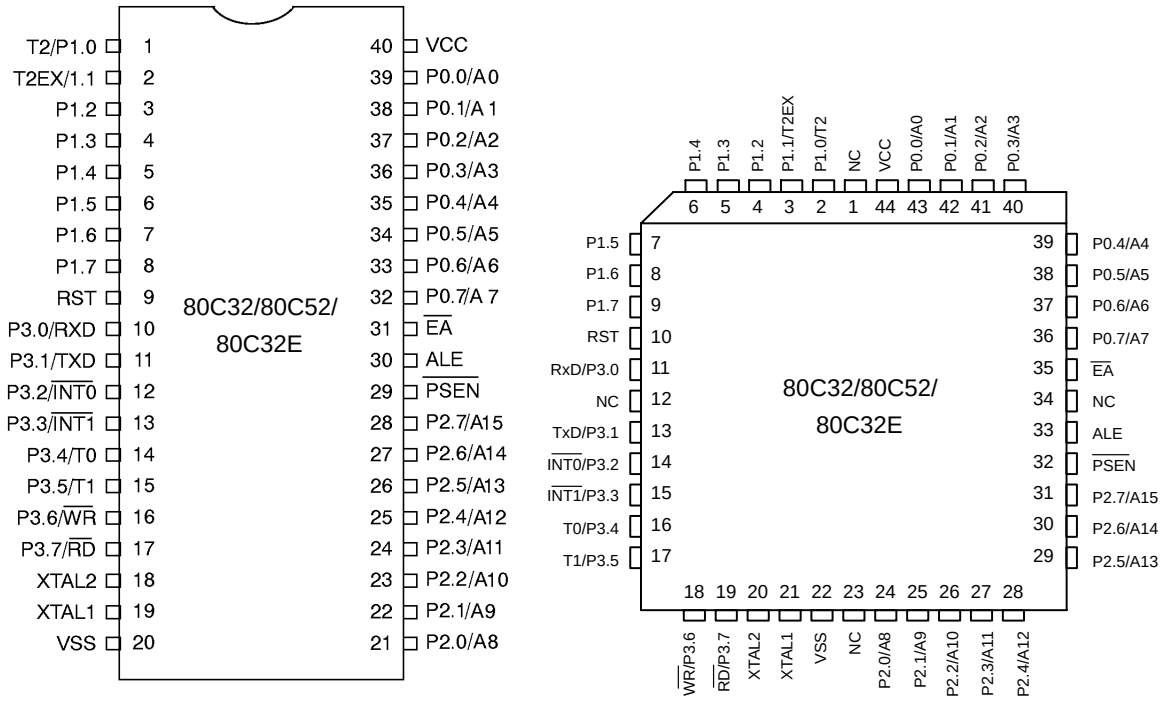


Figure 1. Block Diagram



CDIL JLCC

Diagrams are for reference only. Package sizes are not to scale.

Figure 2. Pin Configuration

4. Pin Description

4.1. VSS

Circuit ground potential.

4.2. VCC

Supply voltage during normal, Idle, and Power Down operation.

4.3. Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C52. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

4.4. Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the 80C52, Port 1 can sink/ source three LS TTL inputs. It can drive CMOS inputs without external pullups.

2 inputs of PORT 1 are also used for timer/counter 2 :

P1.0 [T2]: External clock input for timer/counter 2. P1.1 [T2EX]: A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

4.5. Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the 80C52. Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

4.6. Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the TEMIC 51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	TD (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

4.7. RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to VCC. As soon as the Reset is applied (Vin), PORT 1, 2 and 3 are tied to one. This operation is achieved asynchronously even if the oscillator does not start-up.

4.8. ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

4.9. $\overline{PSEN}$

Program Store Enable output is the read strobe to external Program Memory. $\overline{PSEN}$ is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of $\overline{PSEN}$ are skipped during each access to external Data Memory). $\overline{PSEN}$ is not activated during fetches from internal Program Memory. $\overline{PSEN}$ can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

4.10. $\overline{EA}$

When $\overline{EA}$ is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 1 FFFH). When $\overline{EA}$ is held low, the CPU executes only out of external Program Memory. $\overline{EA}$ must not be floated.

4.11. XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

5. Idle And Power Down Operation

Figure 3. shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function, while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

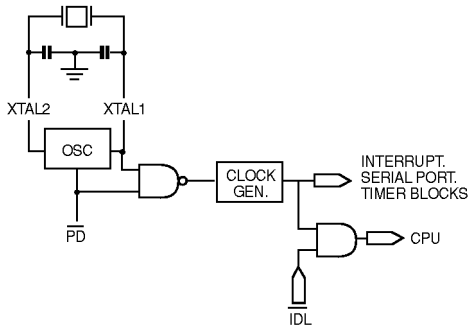


Figure 3. Idle and Power Down Hardware

PCON: Power Control Register

(MSB) **(LSB)**

7	6	5	4	3	2	1	0
SMOD	**–**	**–**	**–**	**GF1**	**GF0**	**PD**	**IDL**

Symbol	Position	Name and Function
SMOD	PCON.7	**Double Baud rate bit** When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
–	PCON.6	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
–	PCON.5	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
–	PCON.4	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
GF1	PCON.3	**General–purpose flag bit**
GF0	PCON.2	**General–purpose flag bit**
PD(1)	PCON.1	**Power Down bit. Setting this bit activates power down operation** Cleared by hardware when an interrupt or reset occurs. Set to activate the Power–Down mode. If IDL and PD are both set, PD takes precedence.
IDL(1)	PCON.0	**Idle mode bit** Cleared by hardware when an interrupt or reset occurs. Set to activate the Idle mode. If IDL and PD are both set, PD takes precedence.

1. *If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).*

5.1. Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. Table 1. describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

5.2. Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The hardware reset initiates the Special Fucntion Register. In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which freezes the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 1. describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in Figure 4.

Table 1. Status of the external pins during idle and power down modes

Mode	Program Memory	Ale	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

5.3. Stop Clock Mode

Due to static design, the TEMIC 80C32/C52 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

5.4. I/O Ports

The I/O buffers for Ports 1, 2 and 3 are implemented as shown in Figure 4.

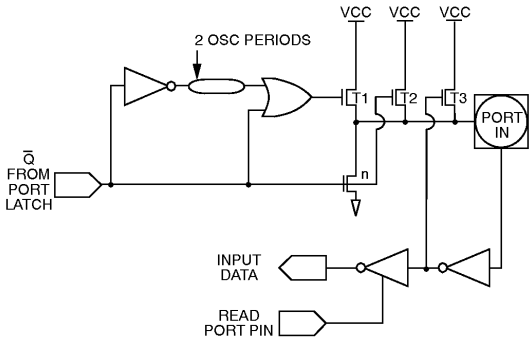


Figure 4. I/O Buffers in the 80C52 (Ports 1, 2, 3)

When the port latch contains a 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the IOH source current. This inverter and T form a latch which holds the 1 and is supported by T2.

When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

5.5. Oscillator Characteristics

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in Figure 5. Either a quartz crystal or ceramic resonator may be used.

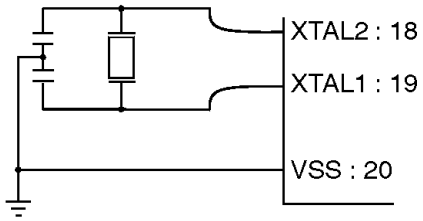


Figure 5. Crystal Oscillator

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 6. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

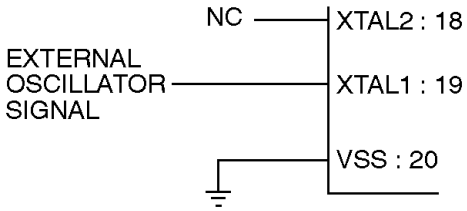


Figure 6. External Drive Configuration

6. Hardware Description

Same as for the 80C51, plus a third timer/counter.

6.1. Timer/Event Counter 2

Timer 2 is a 16 bit timer/counter like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Figure 1.). It has three operating modes : “capture”, “autoload” and “baud rate generator”, which are selected by bits in T2CON as shown in Table 2.

In the capture mode there are two options which are selected by bit EXEN2 in T2CON; If EXEN2 = 0, then Timer 2 is a 16 bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively, (RCAP2L and RCAP2H are new Special Function Register in the 80C52). In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.

Table 2. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16 bit auto-reload
0	1	1	16 bit capture
1	X	1	baud rate generator
X	X	0	(off)

The capture mode is illustrated in Figure 7.

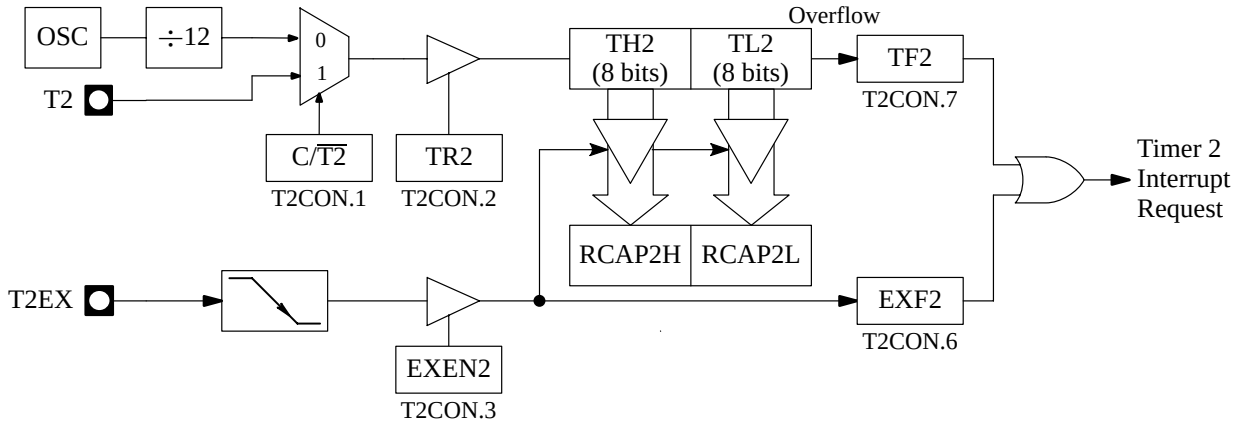


Figure 7. Timer 2 in Capture Mode

In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON.If EXEN2 = 0, then when Timer 2 rolls over it does not only set TF2 but also causes the Timer 2 register to be reloaded with the 16 bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16 bit reload and set EXF2.

The auto-reload mode is illustrated in Figure 8.

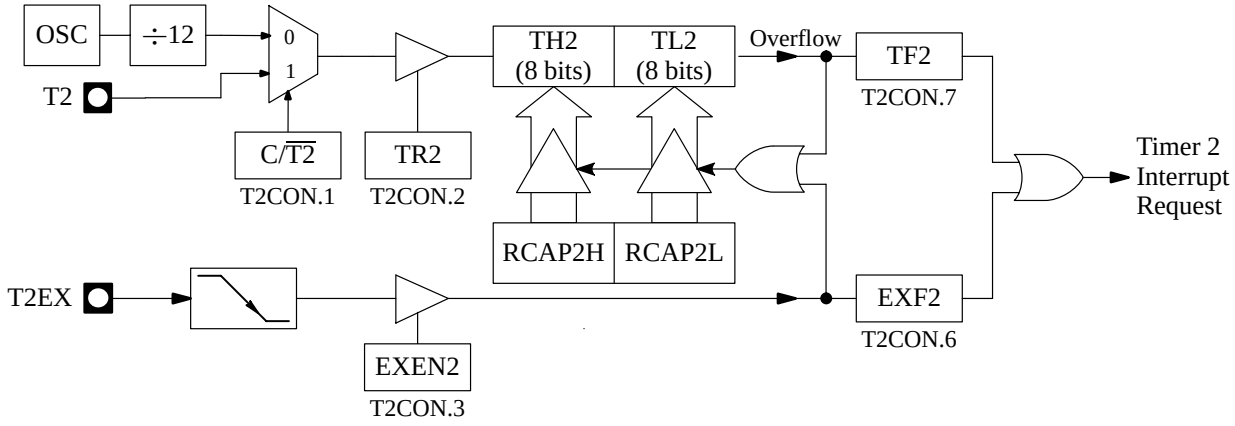


Figure 8. Timer in Auto–Reload Mode

T2CON (S:C8h)
Timer/Counter 2 Control Register

7	6	5	4	3	2	1	0
TF2	**EXF2**	**RCLK**	**TCLK**	**EXEN2**	**TR2**	**C/T2#**	**CP/RL2#**

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 Overflow flag** TF2 is not set if RCLK= 1 or TCLK= 1. Set by hardware when Timer 2 overflows. Must be cleared by software
6	EXF2	**Timer 2 External flag** EXF2 does not cause an interrupt in up/down counter mode (DCEN= 1). Set by hardware if EXEN2= 1 when a negative transition on T2EX pin is detected.
5	RCLK	**Receive Clock bit** Clear to select Timer 1 as the Timer Receive Baud Rate Generator for the Serial Port in modes 1 and 3. Set to select Timer 2 as the Timer Receive Baud Rate Generator for the Serial Port in modes 1 and 3.
4	TCLK	**Transmit Clock bit** Clear to select Timer 1 as the Timer Transmit Baud Rate Generator for the Serial Port in modes 1 and 3. Set to select Timer 2 as the Timer Transmit Baud Rate Generator for the Serial Port in modes 1 and 3.
3	EXEN2	**Timer 2 External Enable bit** Clear to ignore events on T2EX pin for Timer 2. Set to cause a capture or reload when a negative transition on T2EX pin is detected unless Timer 2 is being used as the Baud Rate Generator for the Serial Port.
2	TR2	**Timer 2 Run Control bit** Clear to turn off Timer 2. Set to to turn on Timer 2.
1	C/T2#	**Timer 2 Counter/Timer Select bit** Clear for Timer operation: Timer 2 counts the divided–down system clock. Set for Counter operation: Timer 2 counts negative transitions on external pin T2.
0	CP/RL2#	**Capture/Reload bit** CP/RL2# is ignored and Timer 2 is forced to auto–reload on Timer 2 overflow if RCLK= 1 or TCLK= 1. Clear to auto–reload on Timer 2 overflows or negative transitions on T2EX pin if EXEN2= 1. Set to capture on negative transitions on T2EX pin if EXEN2= 1

Reset Value= 0000 0000b

7. Electrical Characteristics

7.1. Absolute Maximum Ratings(1)

Ambiant Temperature Under Bias:
M = military . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to + 150°C
Voltage on VCC to VSS . . . . . –0.5 V to + 7 V
Voltage on Any Pin to VSS . . . . . –0.5 V to VCC + 0.5 V
Power Dissipation . . . . . 1 W(2)

Notes:

1. *Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.*
2. *This value is based on the maximum allowable die temperature and the thermal resistance of the package·*

7.2. DC parameters –Military

Table 3. DC Parameters

TA= –55°C + 125°C; VSS= 0 V; VCC= 5 V ± 10 %; F= 0 to 36 MHz

Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5	0.2 VCC – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 1.4	VCC + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.45	V	IOL= 1.6 mA(4)
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	IOL= 3.2 mA(4)
VOH	Output High Voltage (Port 1, 2 and 3)	2.4		V	IOH= – 60 µA VCC= 5 V ± 10 %
		0.75 VCC		V	IOH= – 25 µA
		0.9 VCC		V	IOH= – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, PEN)	2.4		V	IOH= – 400 µA VCC= 5 V ± 10 %
		0.75 VCC		V	IOH= – 150 µA
		0.9 VCC		V	IOH= – 40 µA
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 75	µA	Vin= 0.45 V
ILI	Input leakage Current		+/– 10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin= 2.0 V
IPD	Power Down Current		75	µA	VCC= 2.0 V to 5.5 V(3)
RRST	RST Pulldown Resistor	50	200	KΩ	
CIO	Capacitance of I/O Buffer		10	pF	MHz, Ta= 25°C
ICC	Power Supply Current Freq= 1 MHz Icc op Icc idle Freq= 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op= 1.25 Freq (MHz) + 5 mA Icc idle= 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	VCC= 5.5 V

Notes:

1. *ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL= 5 ns, VIL= VSS + .5 V, VIH= VCC –.5 V; XTAL2 N.C. ; EA= RST= Port 0= VCC. ICC would be slighty higher if a crystal oscillator used.*
2. *Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL= 5 ns, VIL= VSS + 5 V, VIH= VCC –.5 V ; XTAL2 N.C; Port 0= VCC; EA= RST= VSS.*
3. *Power Down ICC is measured with all output pins disconnected; EA= PORT 0= VCC; XTAL2 N.C. ; RST= VSS.*
4. *Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V may exceed 0,45 V with maxi VOL peak 0.6 V. A Schmitt Trigger use is not necessary.*

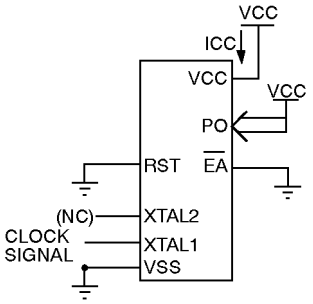


Figure 9. ICC Test Condition, Idle Mode. All other pins are disconnected

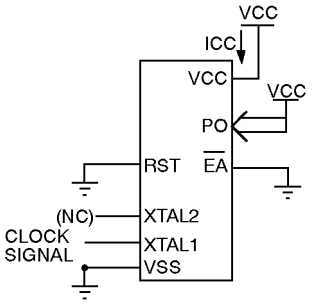


Figure 10. ICC Test Condition, Active Mode. All other pins are disconnected

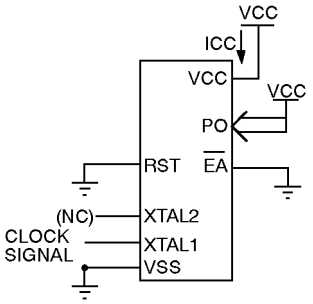
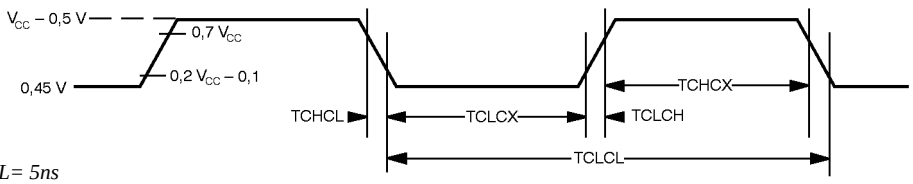


Figure 11. ICC Test Condition, Power Down Mode. All other pins are disconnected



Note:
TCLCH= TCHCL= 5ns

Figure 12. Clock Signal Waveform for ICC Tests in Active and Idle Modes

7.3. Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL= Time for Address Valid to ALE low.

TLLPL= Time for ALE low to $\overline{\text{PSEN}}$ low.

A: Address.	Q: Output data.
C: Clock.	R: READ signal.
D: Input data.	T: Time.
H: Logic level HIGH	V: Valid.
I: Instruction (program memory contents).	W: WRITE signal.
L: Logic level LOW, or ALE.	X: No longer a valid logic level.
P: PSEN.	Z: Float.

7.4. AC Parameters

TA= –55° + 125°C; VSS= 0 V; VCC= 5 V ± 10 %; F= 0 to 36 MHz
(Load Capacitance for PORT 0, ALE and PSEN= 100 pF; Load Capacitance for all other outputs= 80 pF)

Table 4. External Program Memory Characteristics (values in ns)

		16 MHz		30 MHz		36 MHz	
Symbol	**Parameter**	**min**	**max**	**min**	**max**	**min**	**max**
TLHLL	ALE Pulse Width	110		60		50	
TAVLL	Address valid to ALE	40		15		10	
TLLAX	Address Hold After ALE	35		35		35	
TLLIV	ALE to valid instr in		185		100		80
TLLPL	ALE to PSEN	45		25		20	
TPLPH	PSEN pulse Width	165		80		75	
TPLIV	PSEN to valid instr in		125		65		50
TPXIX	Input instr Hold After PSEN	0		0		0	
TPXIZ	Input instr Float After PSEN		50		30		25
TPXAV	PSEN to Address Valid	55		35		30	
TAVIV	Address to Valid instr in		230		130		90
TPLAZ	PSEN low to Address Float		10		6		5

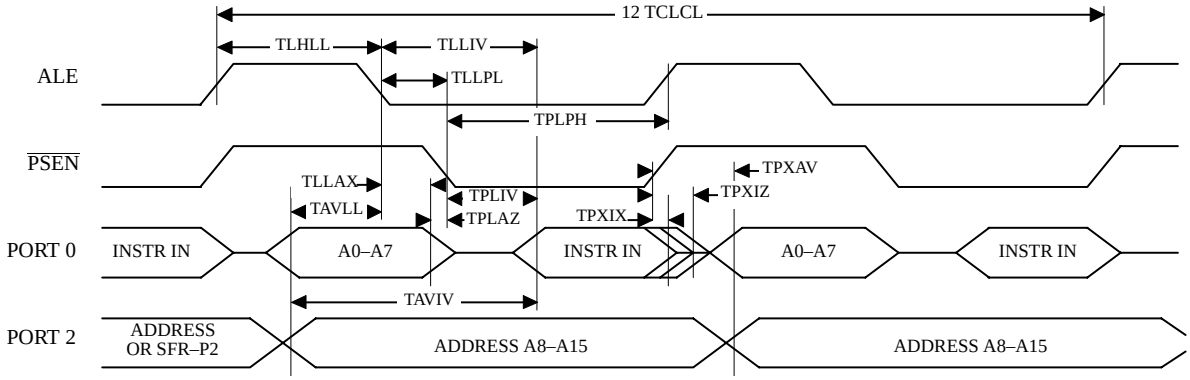


Figure 13. External Program Memory Read Cycle

Table 5. External Data Memory Characteristics (values in ns)

		16 MHz		30 MHz		36 MHz	
Symbol	**Parameter**	**min**	**max**	**min**	**max**	**min**	**max**
TRLRH	RD pulse Width	340		180		120	
TWLWH	WR pulse Width	340		180		120	
TLLAX	Address Hold After ALE	85		55		35	
TRLDV	RD to Valid Data in		240		135		110
TRHDX	Data hold after RD	0		0		0	
TRHDZ	Data float after RD		90		70		50
TLLDV	ALE to Valid Data In		435		235		170
TAVDV	Address to Valid Data IN		480		260		190
TLLWL	ALE to WR or RD	150	250	90	115	70	100
TAVWL	Address to WR or RD	180		115		75	
TQVWX	Data valid to WR transition	35		20		15	
TQVWH	Data Setup to WR transition	380		215		170	
TWHQX	Data Hold after WR	40		20		15	
TRLAZ	RD low to Address Float		0		0		0
TWHLH	RD or WR high to ALE high	35	90	20	40	20	40

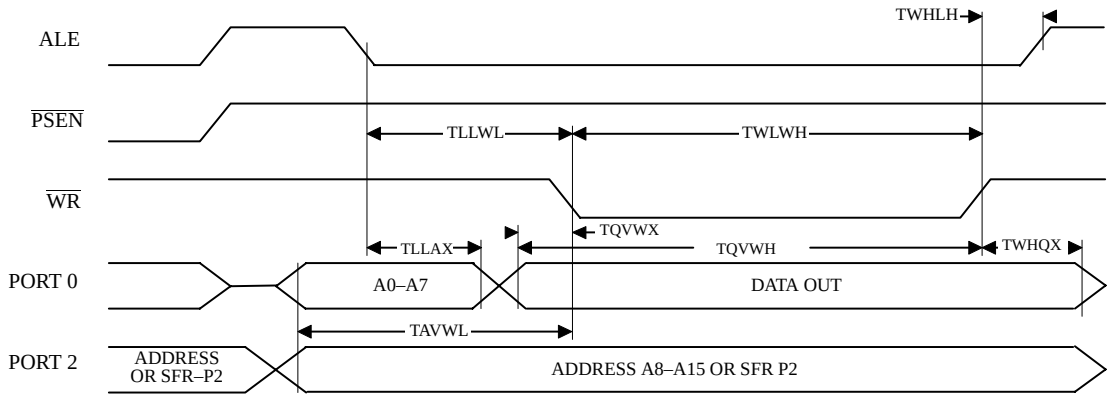


Figure 14. External Data Memory Write Cycle

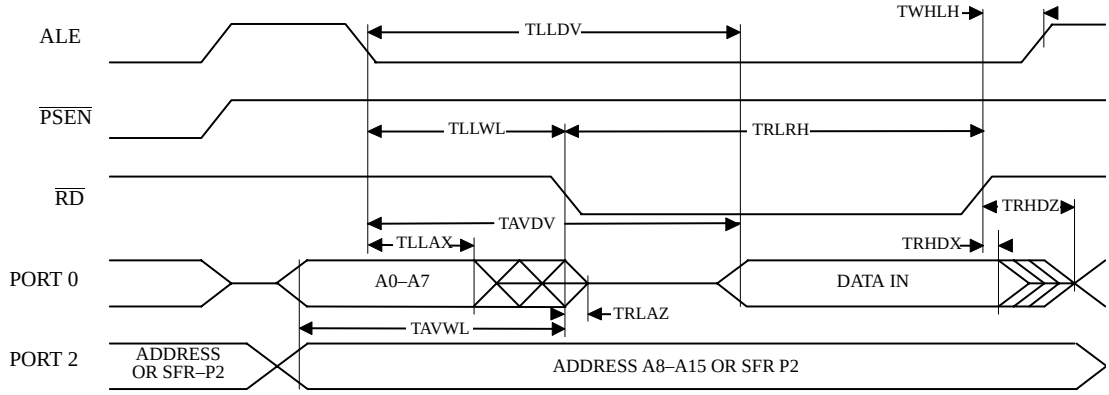


Figure 15. External Data Memory Read Cycle

Table 6. Serial Port Timing – Shift Register Mode (values in ns)

		16 MHz		30 MHz		36 MHz	
Symbol	**Parameter**	**min**	**max**	**min**	**max**	**min**	**max**
TXLXL	Serial Port Clock Cycle Time	750		400		330	
TQVXH	Output Data Setup to Clock Rising Edge	563		300		220	
TXHQX	Output Data Hold after Clock Rising Edge	63		50		45	
TXHDX	Input Data Hold after Clock Rising Edge	0		0		0	
TXHDV	Clock Rising Edge to Input Data Valid		563		300		250

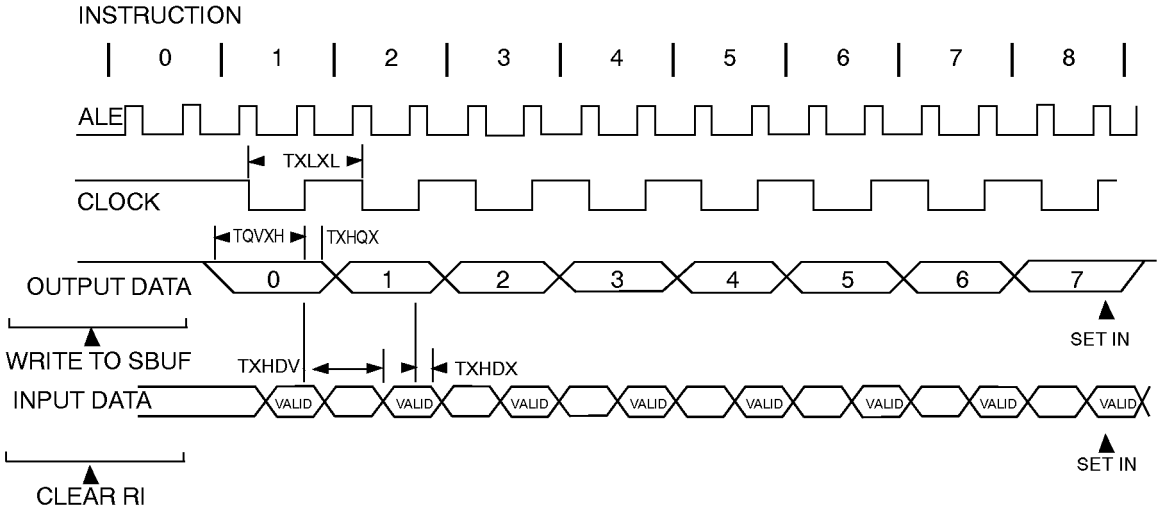


Figure 16. Shift Register Timing Waveforms

Table 7. External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Unit
FCLCL	Oscillator Frequency		44	MHz
TCLCL	Oscillator period	22.7		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

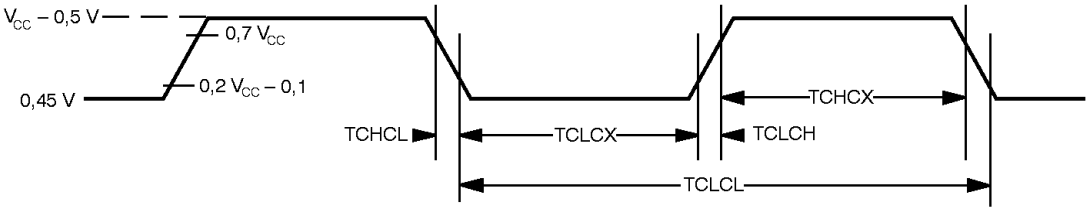


Figure 17. External Clock Drive Waveforms

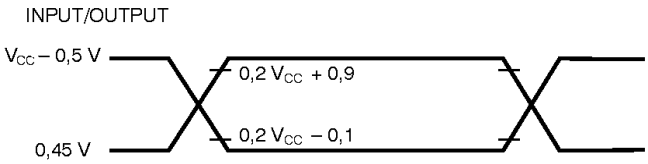


Figure 18. AC Testing Input/Output Waveforms

AC inputs during testing are driven at VCC – 0.5 for a logic “1” and 0.45 V for a logic “0”. Timing measurements are made at VIH min for a logic “1” and VIL max for a logic “0”.

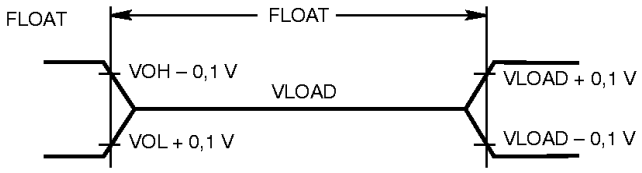


Figure 19. Float Waveforms

For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 mA.

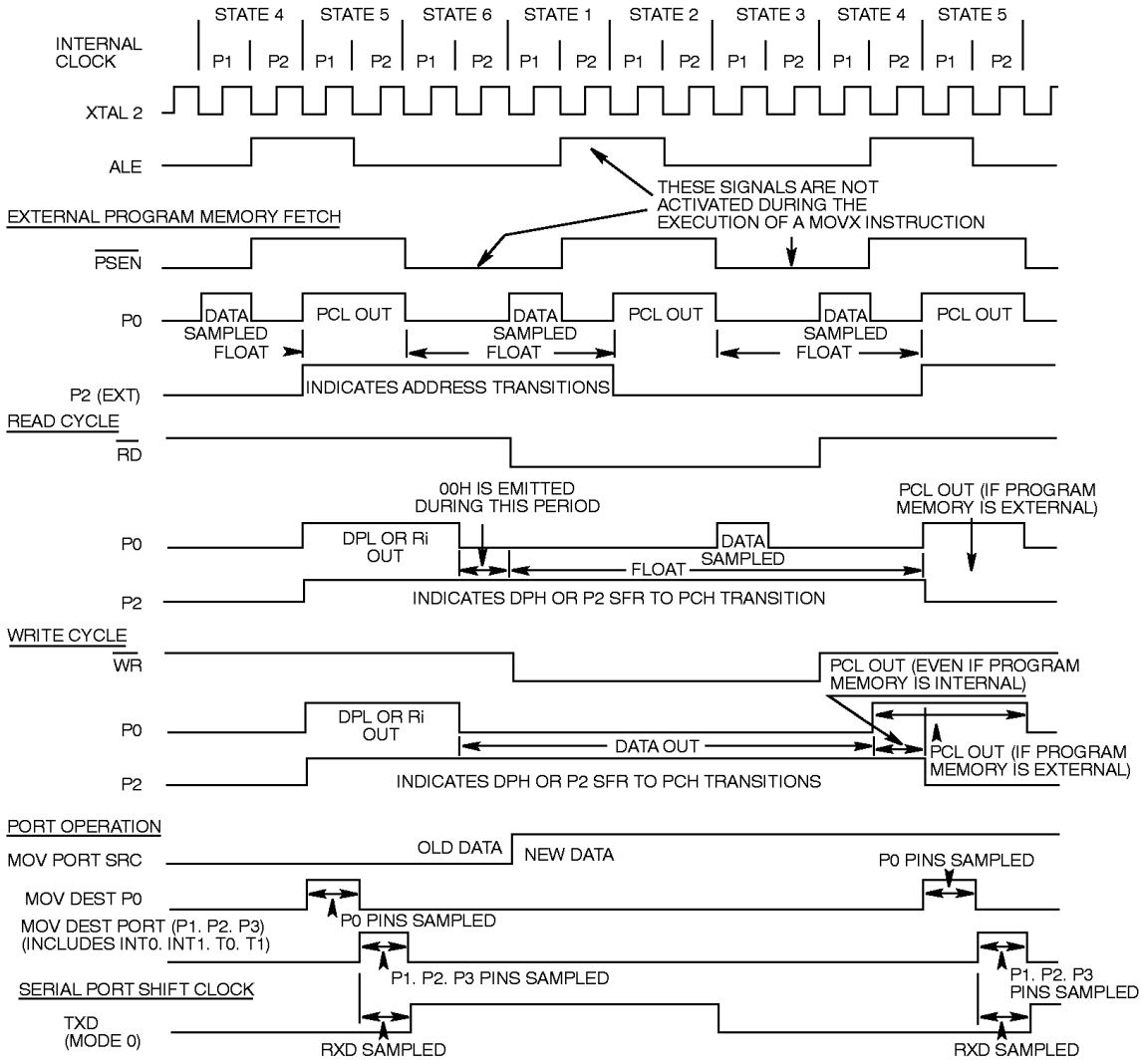
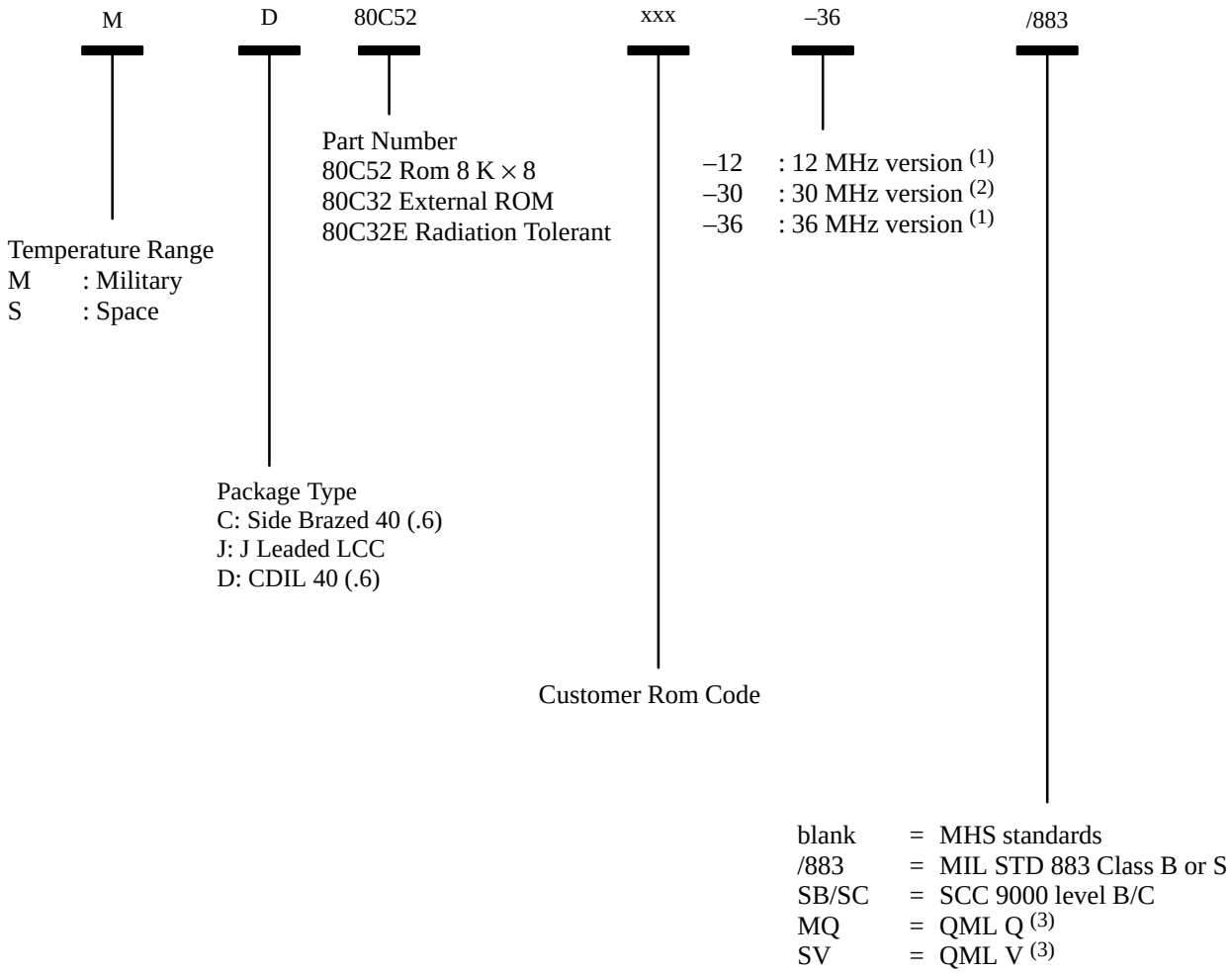


Figure 20. Clock Waveforms

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

8. Ordering Information



1. *Only for C32 and C52.*
2. *Only for C32E*
3. *The Standard Military Drawing 5962–00518 must be taken as the reference for QML–Q and QML–V procurement.*