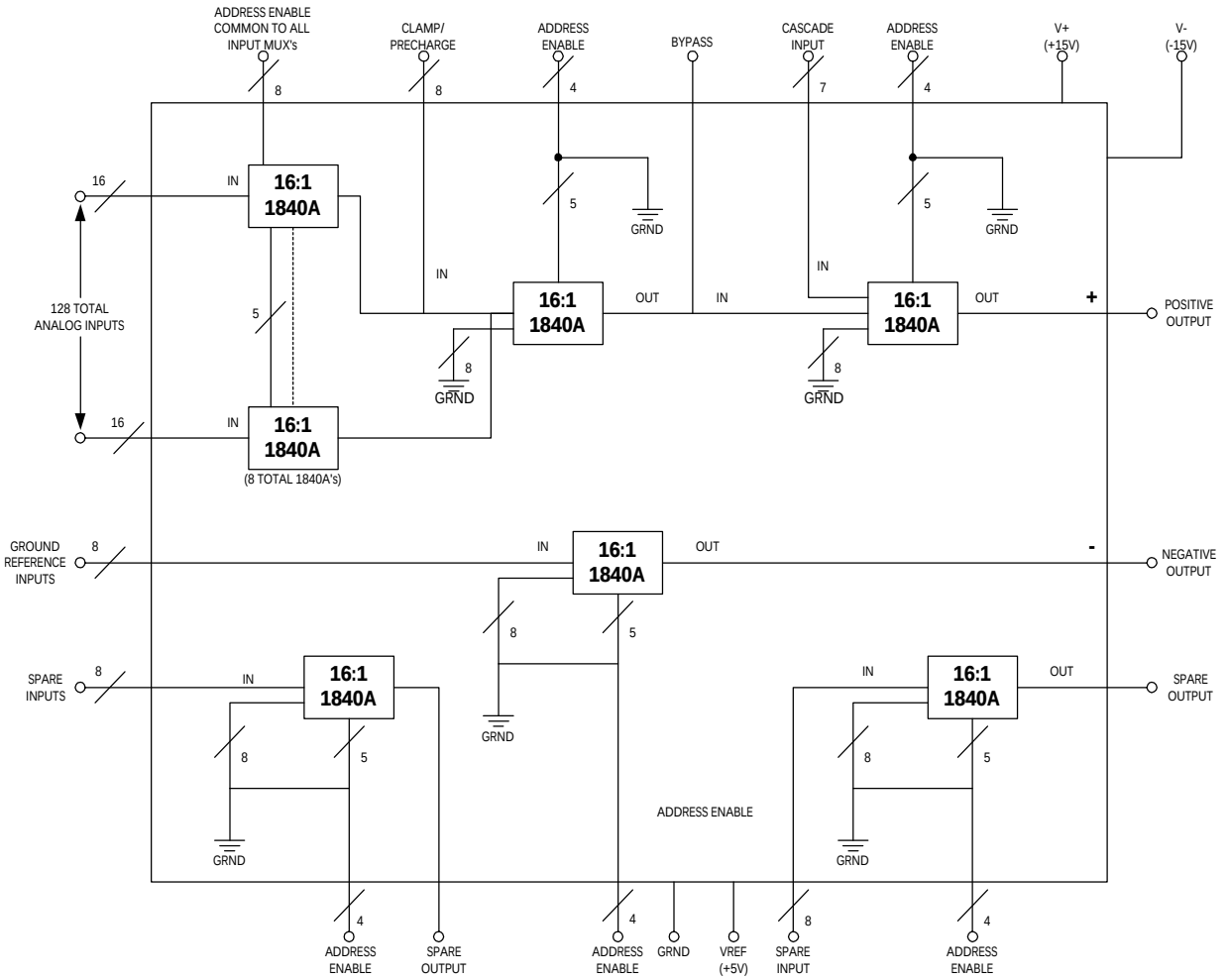
128 CHANNEL MULTIPLEXER
81840RP



81840RP BLOCK DIAGRAM

FEATURES:

- 128 channel multiplexer, MCM
- Package:
  - 256 pin RAD-PAK® quad flat pack

DESCRIPTION:

Space Electronics' 81840RP (RP for RAD-PAK®) high-performance 128-channel multiplexer features a typical 300 krad (Si) total dose tolerance. This datasheet defines the design, performance, and test requirements for a hermetic, telemetry multiplexer, multi-chip-module (MCM), utilizing chip and wire technology to be used in space systems. The 81840RP is intended for use in the environments encountered by high reliability spacecraft applications. The patented radiation-hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. Capable of surviving in-space environment, the 81840RP is ideal for satellite , spacecraft, and space probe missions. It is available up to Class K packaging and screening.

(858) 452-4167 - Fax: (858) 452-5499 - www.spaceelectronics.com

TABLE 1. 81840RP ABSOLUTE MAXIMUM RATINGS[1,2,3,4]

ENVIRONMENT	RANGES
V+ To Ground	20V
V- To Ground	-20V
Input Overvoltage, AIN(1) to AIN(128)	35V to-35V (Power ON or OFF)
Input Overvoltage, Logic Inputs	4V over V_{REF} and -4V below Grd
Power Dissipation	500mW Maximum
Storage Temperature	-65 to 150°C
Operating Temperature	-55 to 125°C

1. The LMUX MCM is designed to operate with power supply voltages ranging from ±5.2V to ±20VDC.
2. The maximum voltage each input AIN(128:1) may see without damage is +35V to -35V with respect to ground.
3. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4. T_A = 25°C unless otherwise specified.

TABLE 2. 81840RP AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	TEST LIMITS						UNITS
		T_A = 25 °C		T_A = 125 °		T_A = -55 °C		
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Input to I/O Channels Prop. Delay	V_{IN} = 5.0V							
$t_{ON(A)}$	R_L = 5kΩ	--	1500	--	1500	--	1500	nsec
$t_{OFF(A)}$	C_L = 50pF	--	1500	--	1500	--	1500	
Enable to I/O	V_{IN} = 5.0V							
$t_{ON(EN)}$	R_L = 5kΩ	--	1500	--	1500	--	1500	nsec
$t_{OFF(EN)}$	C_L = 50 pF	--	1500	--	1500	--	1500	
On Channel Isolation	All enable = 0.8V							
$V_{ISO(ON)}$	V_{IN} = $3V_{RMS}$ @ 500kHz[1]	45	--	45	--	45	--	db
Off Channel Isolation	All enable = 4.0V							
$V_{ISO(OFF)}$	V_{IN} = $3V_{RMS}$ @ 500kHz[1]	45	--	45	--	45	--	db

1. Controlled by design, not directly tested.

TABLE 3. 81840RP ELECTRICAL TEST TABLE

PARAMETER	TEST CONDITIONS	TEST LIMITS						UNITS
		$T_A = 25\ ^oC$		$T_A = 25\ ^oC$		$T_A = 25\ ^oC$		
		MIN	MAX	MIN	MAX	MIN	MAX	
Analog Signal Range, V_0		-15	15	-15	15	-15	15	V
Bypass Output, On-Resistance, 5V, $R_{BP(ON)}$	$V_{IN} = 5V$ $I_{OUT} = -1.0mA$	2.0	6.0	2.0	6.0	2.0	6.0	kΩ
Positive Output, On-Resistance, 5V, $R_{PO(ON)}$	$V_{IN} = 5V$ $I_{OUT} = -1.0mA$	3.0	9.0	3.0	9.0	3.0	9.0	kΩ
Negative or Spare Output, On-Resistance, 5V, $R_{NS(ON)}$	$V_{IN} = 5V$ $I_{OUT} = -1.0mA$	1.0	3.0	1.0	3.0	1.0	3.0	kΩ
Bypass Output, On-Resistance, -5V, $R_{BP(ON)}$	$V_{IN} = -5V$ $I_{OUT} = 1.0mA$	2.0	6.0	2.0	6.0	2.0	6.0	kΩ
Positive Output, On-Resistance, -5V, $R_{PO(ON)}$	$V_{IN} = -5V$ $I_{OUT} = 1.0mA$	3.0	9.0	3.0	9.0	3.0	9.0	kΩ
Negative or Spare Output, On-Resistance, -5V, $R_{NS(ON)}$	$V_{IN} = -5V$ $I_{OUT} = 1.0mA$	1.0	3.0	1.0	4.0	1.0	4.0	kΩ
Input Leakage Current, LA0, LA1, LA2, HA0, LIEN, Address or Enable Pins, I_{AH}, I_{AL}	All unused pins = Ground	-100	100	-200	200	-200	200	nA
Input Leakage Current, All Other Address or Enable Pins $I_{AH,}$ I_{AL}	All unused pins = Ground	-100	100	-200	200	-200	200	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, $+I_{S(OFF)}$	$V_{IN} = 10V$, All enables = 4.0V All unused inputs & outputs = -10V	-20	20	-100	100	-100	100	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, $-I_{S(OFF)}$	$V_{IN} = -10V$ All enables = 4.0V All unused inputs & ouputs = +10V	-20	20	-100	100	-100	100	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, Power off, $+I_{S(OFF)PO}$	VIN = 25V V_S+, V_S-, V_{REF}, V_A, V_{EN} & All unused inputs = Ground	-50	50	-100	100	-100	100	nA
Leakage Current into MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, Positive Overvoltage, $+I_{S(OFF)0V}$[1]	VIN = 35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	-100	100	-200	200	-200	200	nA
Leakage Current inot MUX Input Channels, AINxx, GRINx, SP1INx, SP2INx, CASINx, Negative Overvoltage, $-I_{S(OFF)0V}$[1]	$V_{IN} = -35V$, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	-100	100	-200	200	-200	200	nA

TABLE 3. 81840RP ELECTRICAL TEST TABLE

PARAMETER	TEST CONDITIONS	TEST LIMITS						UNITS
		T_A = 25 °C		T_A = 25 °C		T_A = 25 °C		
		MIN	MAX	MIN	MAX	MIN	MAX	
Leakage Current into MUX Output Channels, SP1OUT, SP2OUT, POSITIVE, NEGATIVE, Positive Overvoltage, $+I_{D(OFF)0V}$[1]	V_{IN} = 35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	-75	75	-200	200	-200	200	nA
Leakage Current into MUX Output Channels, CLPx, BYPASS, $+I_{D(OFF)0V}$[1]	V_{IN} = 35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 0.0V All enables = 4.0V All unused = GND	-100	100	-400	400	-400	400	nA
Leakage Current into MUX Output Channels, SP1OUT, SP2OUT, POSITIVE, NEGATIVE, Negative Overvoltage, $-I_{D(OFF)0V}$[1]	V_{IN} = -35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = -10V All enables = 4.0V All unused = 0.0V	-75	75	-200	200	-200	200	nA
Leakage Current into MUX Output Channels, CLPx, BYPASS, $-I_{D(OFF)0V}$[1]	V_{IN} = -35V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = -10V All enables = 4.0V All unused = 0.0V	-100	100	-400	400	-400	400	nA
Leakage Current into off MUX Output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $+I_{D(OFF)}$	All V_{IN} = 10V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE NEGATIVE = 10V All enables = 0.8V All unused = 0.0V	-20	20	-100	100	-100	100	nA
Leakage Current into off MUX Output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $-I_{D(OFF)}$	All V_{IN} = -10V, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE = 10V All enables = 0.8V All unused = 0.0V	-20	20	-100	100	-100	100	nA
Leakage Current into on MUX Output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $-I_{D(ON)}$ Note: Sequence all inputs for each output.	Output and Input Under Test = 10V All unused V_{IN} = 10V All enables = 0.8V	-20	20	-100	100	-100	100	nA
Leakage Current into on MUX output Channels, CLPx, SP1OUT, SP2OUT, BYPASS, POSITIVE, NEGATIVE, $I_{D(ON)}$ Note: Sequence all inputs for each output	Output and Input Under Test = -10V All unused V_{IN} = -10V All enables = 0.8V	-20	20	-100	100	-100	100	nA
V_{REF}		4.5	7.0	4.5	7.0	4.5	7.0	V

TABLE 3. 81840RP ELECTRICAL TEST TABLE

PARAMETER	TEST CONDITIONS	TEST LIMITS						UNITS
		$T_A = 25\ ^oC$		$T_A = 25\ ^oC$		$T_A = 25\ ^oC$		
		MIN	MAX	MIN	MAX	MIN	MAX	
Input Voltage Low V_{IL}[2]	$V_{IN} = 5.0V$	--	0.3 V_{ref}	--	0.3 V_{ref}	--	0.3 V_{ref}	V
Input Voltage High V_{IH}[2]	$V_{IN} = 5.0V$	0.7 V_{ref}	--	0.7 V_{ref}	--	0.7 V_{ref}	--	V
Supply Current for I_{S+} I_{S-}	All enables = 0.8V	 0.65 -0.65	 6.5 -6.5	 0.65 -0.65	 6.5 -6.5	 0.65 -0.65	 6.5 -6.5	mA
Standby Supply Current for I_{SB+} I_{SB-}	All enables = 0.8V	 0.65 -0.65	 6.5 6.5	 0.65 -0.65	 6.5 -6.5	 0.65 -0.65	 6.5 -6.5	mA

1. Current limit set to 10 µA during test.
2. For V_{IH} and V_{IL} measurements, V_{REF} will equal 4.5V and 5.5V.
3. Unless otherwise specified:
   - V- = -15.0V
   - V+ = 15.0V
   - $V_{REF} = 5.0V$
   - $V_{AH} = 4.0V$
   - $V_{AL} = 0.8V$

FIGURE 1. 81840RP BLOCK DIAGRAM

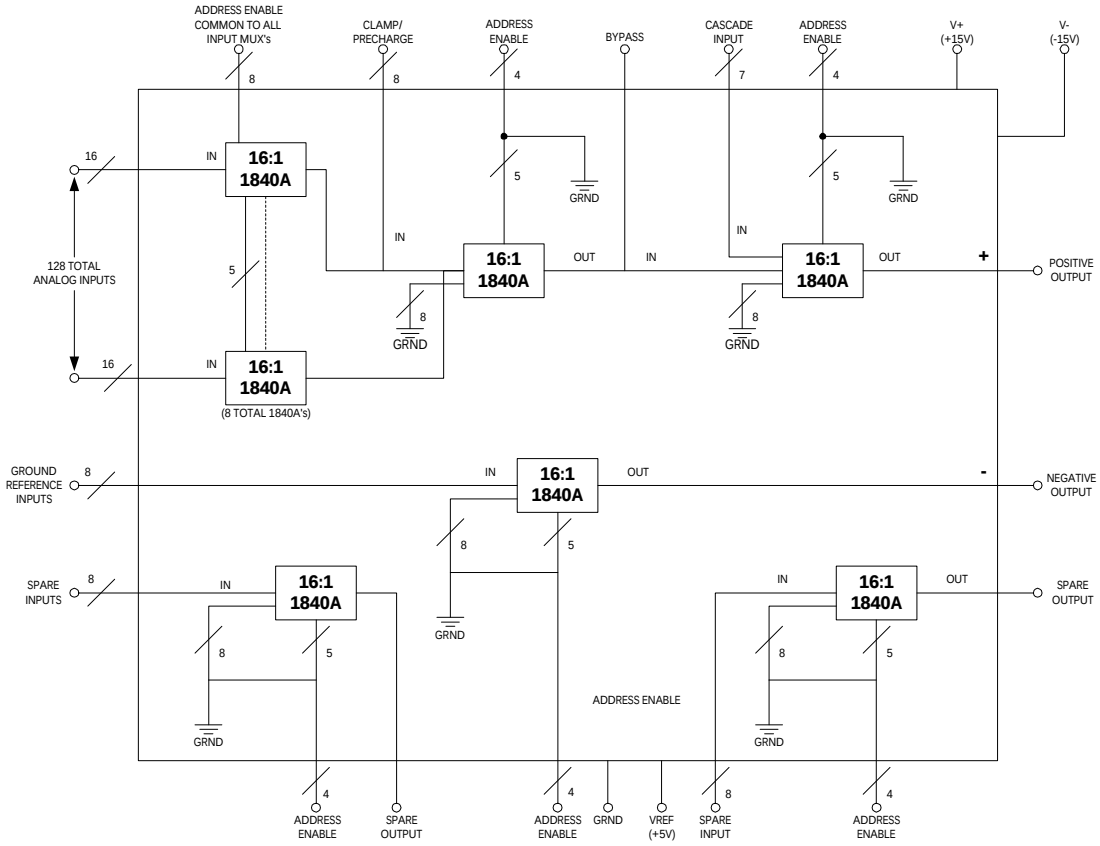


FIGURE 2. 81840RP ADDRESS DECODING SCHEME

ADDRESS INPUTS LA (0,4)	TELEMETRY CHANNEL
0 0 0 0 0 0 0	AIN(1)
0 0 0 0 0 0 1	AIN(2)
0 0 0 0 0 1 0	AIN(3)
0 0 0 0 0 1 1	AIN(4)
0 0 0 0 1 0 0	AIN(5)
0 0 0 0 1 0 1	AIN(6)
0 0 0 0 1 1 0	AIN(7)
0 0 0 0 1 1 1	AIN(8)
0 0 0 1 0 0 0	AIN(9)
"	
"	
"	
1 1 1 0 1 1 1	AIN(121)
1 1 1 1 0 0 1	AIN(122)
1 1 1 1 0 1 0	AIN(123)
1 1 1 1 0 1 1	AIN(124)
1 1 1 1 1 0 0	AIN(125)
1 1 1 1 1 0 1	AIN(126)
1 1 1 1 1 1 0	AIN(127)
1 1 1 1 1 1 1	AIN(128)

FIGURE 3. 81840RP PINOUT

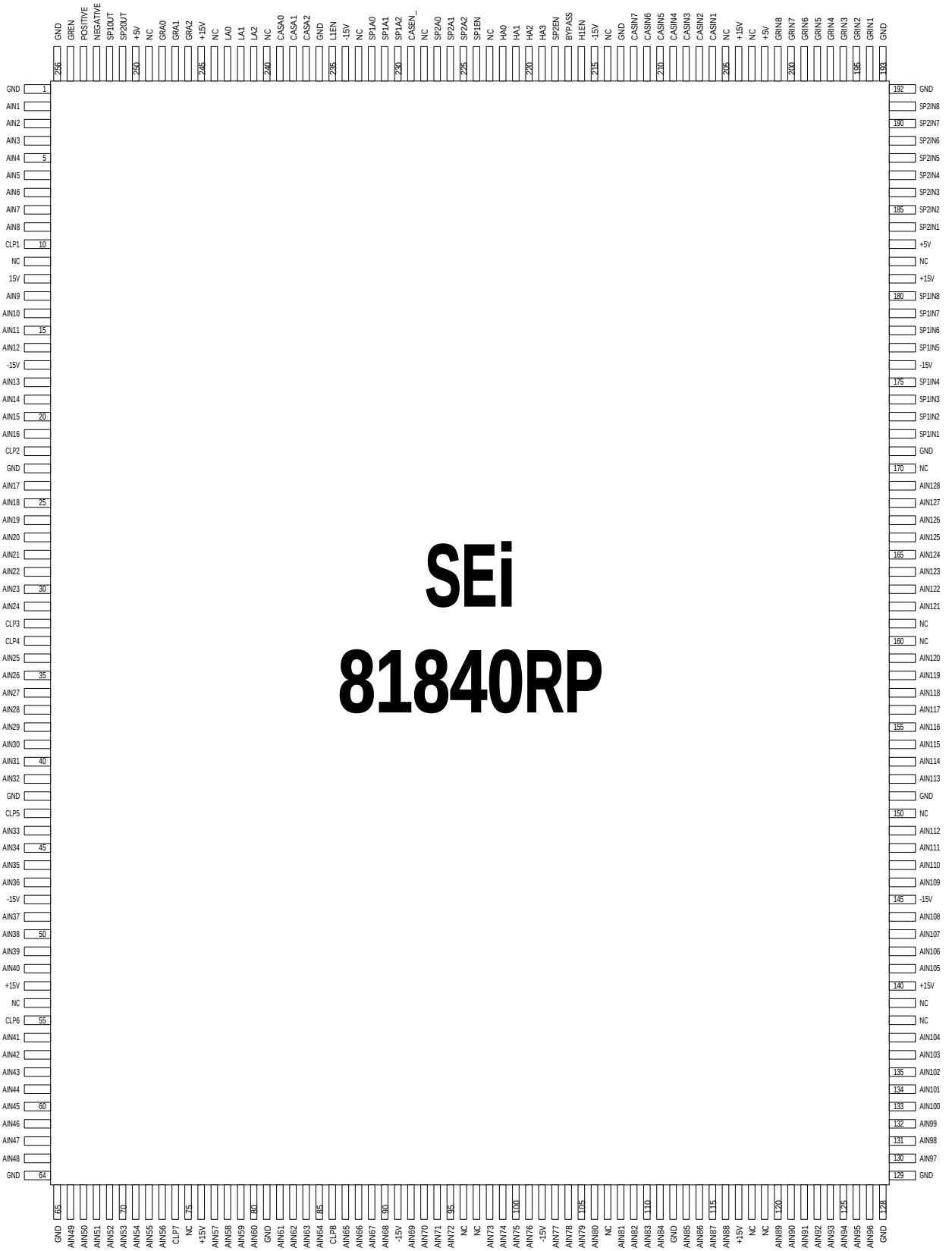
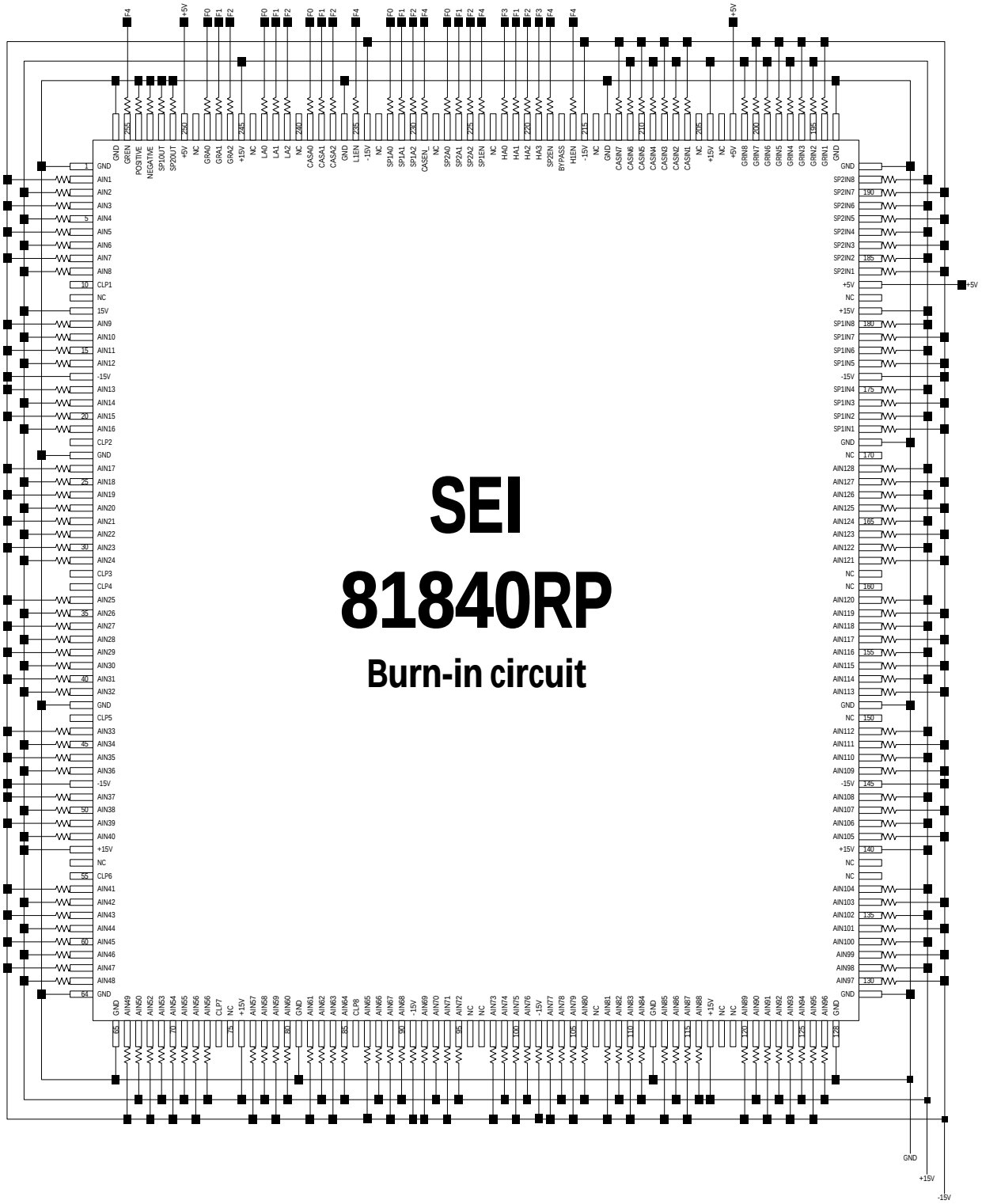
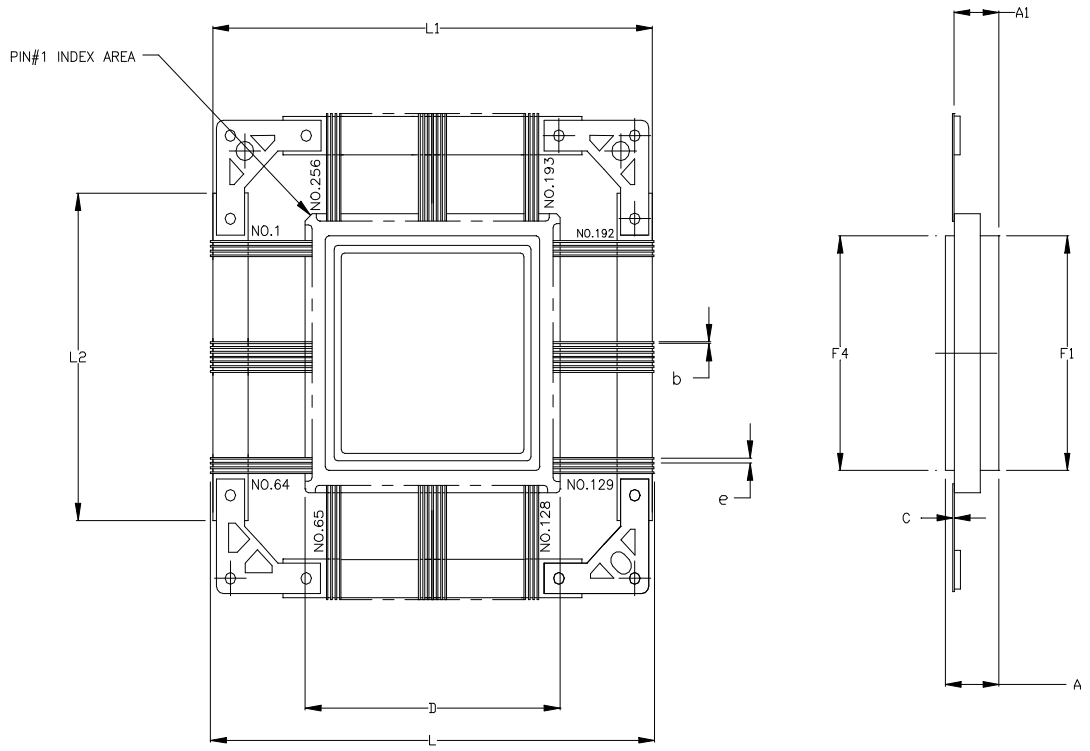


FIGURE 4. 81840RP BURN-IN CIRCUIT



1. V_{CC} = 5VDC +/- 0.25 VDC, CLK = 500 kHz 0 to 5V, 50% duty cycle.
2. F1 = F0/2, F2 = F1/2, etc.
3. Components: all resistors = 1.0k ohm, capacitors = 0.1 micro farad.

FIGURE 5. PACKAGE OUTLINE DIAGRAM



256-PIN QUAD FLAT PACKAGE

SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	.302	.329	.356
b	.005	.007	.009
c	.005	.006	.007
D	1.438	1.450SQ	1.462
D1		1.260BSC	
e		.020BSC	
L	3.010	3.040	3.070
L1	2.970	3.000	3.030
L2	2.178	2.200	2.222
A1	.253	.275	.297
N		256	
F1	1.215	1.220	1.225
F4	1.215	1.220	1.225

Q256-01
All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Space Electronics verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Space Electronics assumes no responsibility for the use of this information.

Space Electronics' products are not authorized for use as critical components in life support devices or systems without express written approval from Space Electronics.

Any claim against Space Electronics Inc. must be made within 90 days from the date of shipment from Space Electronics. Space Electronics' liability shall be limited to replacement of defective parts.

81840RP APPENDIX NOTE

1.0 SCOPE

1.1 THIS DRAWING DEFINES THE DESIGN, PERFORMACE AND TEST REQUIRMENTS FOR A HERMETIC MULTIPLEXER MULTICHIP MODULE, UTILIZING CHIP AND WIRE TECHNOLOGY TO BE USED IN SPACE SYSTEMS.

PART NUMBER	IDENTIFICATION
81840RPQE	ENGINEERING UNIT
81840RPQH	CLASS H
81840RPQK	CLASS K

2. REFERENCE DOCUMENTS

2.1. DOCUMENTS SPECIFIED HEREIN, OF THE ISSUE IN EFFECT ON THE DATE OF INVITATION FOR BID, FORM A PART OF THIS DRAWING TO THE EXTENT SPECIFIED HEREIN. IN CASE OF CONFLICT, THIS DRAWING SHALL TAKE PRECEDENCE.

SPECIFICATIONS

MILITARY

MIL-G-45204	PLATING SPECIFICATION, GOLD
MIL-PRF-38534	HYBRID MICROCIRCUITS, GENERAL SPECIFICATION FOR

STANDARDS

MILITARY

MIL-STD-883	TEST METHODS AND PROCEDURES FOR MICROELECTRONICS

MIL-STD-1285	MARKING OF ELECTRICAL AND ELECTRONIC PARTS

OTHER

ANSI Y14.5M-1982	DIMENSIONING AND TOLERANCING
PI-051-PA	STANDARD REWORK AND REPAIR PROCEDURE (SEi)

3. REQUIREMENTS

3.1. GENERAL: MULTICHIP CIRCUITS (MCM) FURNISHED IN ACCORDANCE WITH THIS DRAWING SHALL MEET THE REQUIREMENTS SPECIFIED IN MIL-PRF-38534, CLASS K AS MODIFIED HEREIN.

3.2. MECHANICAL

3.2.1. DESIGN, CONSTRUCTION AND PHYSICAL DIMENSIONS (CASE OUTLINE) SHALL BE AS SPECIFIED IN MIL-PRF-38534 AND FIGURE 5.0 HEREIN.

3.2.3. LEAD MATERIAL AND FINISH: IN ACCORDANCE WITH MIL-PRF-38534, FINISH LETTER C (GOLD PLATE). WHEN ELECTROLYTIC, ALL GOLD PLATING SHALL BE PER MIL-G-45204.

3.3. ELECTRICAL

3.3.1. ABSOLUTE MAXIMUM RATINGS SHALL BE AS SPECIFIED IN APPLICABLE TABLE.

3.3.2. ELECTRICAL CHARACTERISTICS: ALL MULTI-CHIP MODULES SUPPLIED IN ACCORDANCE WITH THE REQUIREMENTS OF THIS DRAWING SHALL MEET THE APPLICABLE ELECTRICAL TESTS SPECIFIED IN ELECTRICAL CHARACTERISTICS TABLES.

3.3.3. BURN-IN: ALL MULTI-CHIP MODULES SHALL BE SUBJECTED TO BURN-IN IN ACCORDANCE WITH MIL-STD-883, METHOD 1015. THE BURN-IN CIRCUIT USED BY THE MANUFACTURER SHALL BE AS SPECIFIED IN FIGURE 4.0.

3.4. ENVIRONMENTAL

3.4.1. MULTI-CHIP MODULES SUPPLIED IN ACCORDANCE WITH THIS DRAWING SHALL BE CAPABLE OF MEETING THE ENVIRONMENTAL REQUIREMENTS OF MIL-PRF-38534.

3.5. SCREENING TESTS: EACH MULTI-CHIP MODULES SUPPLIED IN ACCORDANCE WITH THIS DRAWING SHALL HAVE BEEN SUBJECTED TO AND PASSED THE SCREENING TESTS PERFORMED BY THE MANUFACTURER.

3.5.1. INTERIM ELECTRICAL PARAMETERS: PERFORM AT 25°C.

3.5.2. FINAL ELECTRICAL TEST CHARACTERISTICS: PERFORM ALL -55°C, AND 125°C TESTS OF ELECTRICAL TEST TABLE 3.

3.5.3. DELTA COMPUTATION:. PER APPLICABLE TABLES.

3.5.4. ELECTRICAL FAILURES: MULTI-CHIP MODULES WHICH FAIL SHALL BE REMOVED FROM TEST AT THE TIME OF OBSERVATION OR IMMEDIATELY FOLLOWING CONCLUSION OF THE TEST IN WHICH THE FAILURE WAS OBSERVED. FAILED MULTI-CHIP MODULES MAY BE REWORKED AS REQUIRED.

3.5.5. SCREENING TEST DATA: ALL ATTRIBUTES AND VARIABLES TEST DATA WHICH RESULTS FROM THE PERFORMANCE OF THE TESTS SPECIFIED IN APPLICABLE TABLE SHALL BE KEPT AT THE SUPPLIERS FACILITY AND BE AVAILABLE FOR REVIEW. THE DATA SHALL BE LEGIBLE AND SHALL BE CORRELATABLE TO THE LOT DATA CODE AND HYBRID MICROCIRCUIT SERIALIZATION.

3.5.6. INSPECTION LOT: INSPECTION LOT SHALL BE AS DEFINED IN MIL-PRF-38534.

3.5.6.1. LOT TRACEABILITY: EACH MULTI-CHIP MODULE SUPPLIED TO THE PROCURING ACTIVITY SHALL CONTAIN DICE WHICH ARE TRACEABLE TO THE WAFER LOT. THE MANUFACTURER SHALL MAINTAIN IN-HOUSE RECORDS (E.G., LOT TRAVELERS) TO DOCUMENT THE COMPLETION OF EACH REQUIRED PROCESSING STEP THROUGH MULTI-CHIP MODULE ASSEMBLY AND SCREENING TESTS.

3.6. MARKING

3.6.1. GENERAL: MARKING SHALL BE IN ACCORDANCE WITH MIL-PRF-38534, AND SHALL INCLUDE, AS A MINIMUM, THE FOLLOWING:

PRIME CONTRACTOR PART NUMBER

DATA CODE (INSPECTION LOT IDENTIFICATION CODE)

MANUFACTURER'S NAME OR TRADEMARK

SERIAL NUMBER AND ESD SYMBOL.

3.7. DESIGN AND PROCESS CONTROL: AT ANY TIME DURING PROCUREMENT OF MULTI-CHIP MODULES, ANY CHANGES TO PROCESSES USED IN THE MANUFACTURE OF THE MULTI-CHIP MODULES THAT IN ANY WAY AFFECT THEIR PHYSICAL OR FUNCTIONAL PERFORMANCE SHALL BE REPORTED TO THE BUYER PRIOR TO MANUFACTURE, OF AFFECTED MICROCIRCUITS. REPRODUCIBLE DOCUMENTATION SHALL BE USED TO DESCRIBE CHANGES.

3.8. SERIALIZATION: EACH MULTI-CHIP MODULE SHALL BE SERIALIZED PRIOR TO THE FIRST RECORDED ELECTRICAL MEASUREMENTS OF THE 100 PERCENT SCREENING TEST. THE SERIAL NUMBER MAY BE NUMERIC OR ALPHA-NUMERIC AT THE MANUFACTURER'S OPTION. HOWEVER, THE SERIAL NUMBER SHALL BE UNIQUE AND TRACEABLE TO THE INDIVIDUAL HYBRID MICROCIRCUIT. SERIAL NUMBERS SHALL NOT BE DUPLICATED WITHIN A LOT DATE CODE.

3.9. LOT DATE CODE: EACH MULTI-CHIP MODULE SHALL BE MARKED WITH A FOUR DIGIT CODE THAT IDENTIFIES THE LAST WEEK OF THE PERIOD (6 WEEKS MAXIMUM) DURING WHICH DEVICES FROM ONE OR MORE INSPECTION LOTS ARE SEALED. INSPECTION LOTS WITHIN A LOT DATE CODE SHALL BE KEPT SEGREGATED UNTIL SERIALIZATION OCCURS.

3.10. DOCUMENTATION AND CHANGE REQUIREMENTS SHALL BE IN ACCORDANCE WITH THE PROCUREMENT DOCUMENT AND HEREIN.

4. QUALITY ASSURANCE PROVISIONS

4.1. GENERAL: THE SUPPLIER SHALL PREPARE, IMPLEMENT, AND MAINTAIN AN EFFECTIVE QUALITY ASSURANCE PROGRAM PLAN THAT DOCUMENTS THE SUPPLIER QUALITY ASSURANCE SYSTEM.

4.2. QUALIFICATION TESTS: MULTICHIP MODULES SUPPLIED IN ACCORDANCE WITH THIS DRAWING SHALL BE CAPABLE OF MEETING THE QUALIFICATION TESTS SPECIFIED IN MIL-STD-883, METHOD 5008. THESE TESTS NEED BE PERFORMED AND DATA FURNISHED ONLY WHEN SPECIFIED. DEVICES UTILIZED SHALL BE RANDOMLY SELECTED FROM THOSE SUCCESSFULLY COMPLETING SCREENING REQUIREMENTS.

4.3 QUALITY CONFORMANCE INSPECTION (QCI): QUALITY CONFORMANCE INSPECTION SHALL BE IN ACCORDANCE WITH MIL-PRF-38534 QUAL-

ITY ASSURANCE REQUIREMENTS AND AS SPECIFIED HEREIN. DEVICES UTILIZED SHALL BE RANDOMLY SELECTED FROM THOSE SUCCESSFULLY COMPLETING SCREENING REQUIREMENTS.

4.3.1. GROUP A INSPECTION: GROUP A INSPECTION SHALL BE IN ACCORDANCE WITH MIL-PRF-38534.

4.3.1.1. TESTS SHALL BE AS SPECIFIED IN MIL-STD-883.

4.3.1.2. SUBGROUPS 7, 8, 9, 10 AND 11 IN TABLE XIa, OF MIL-PRF-38534 SHALL BE OMITTED.

4.3.2. GROUP B INSPECTION: GROUP B INSPECTION SHALL BE IN ACCORDANCE WITH MIL-PRF-38534. SUBGROUP 9 IS NOT TESTED IF OPTED BY SUPPLIER AS ESD CLASS 1, OTHERWISE SAMPLES FROM GROUP A MAY BE UTILIZED.

4.3.2.1. SUBGROUP 2 SHALL BE CONDITION A.

4.3.2.2. SUBGROUP 5 SHALL BE CONDITION D FOR THERMOCOMPRESSION, THERMOSONIC, ULTRASONIC OR WEDGE WIRE BONDING.

4.3.3. GROUP C INSPECTIONS: MULTICHIP MODULES SUPPLIED IN ACCORDANCE WITH THIS DRAWING SHALL BE CAPABLE OF MEETING THE QUALIFICATION TESTS SPECIFIED IN MIL-PRF-38534. GROUP C INSPECTION SHALL BE IN ACCORDANCE WITH MIL-PRF-38534 AND AS FOLLOWS. THE SAMPLE QUANTITY IS FOR LIMITED USAGE ACQUISITION IN ACCORDANCE WITH MIL-STD-883, METHOD 5008.

4.3.3.1. SUBGROUP 1

4.3.3.1.1. CONSTANT ACCELERATION TEST CONDITION SHALL BE 5 Kg.

4.3.3.1.2. RADIOGRAPHIC TESTS ARE NOT REQUIRED. PROCESS CONTROLS ON PARTICLE CONTAMINATION AND CLEANING PROCESSES SHALL BE IN PLACE AT THE SUPPLIER FACILITY.

4.3.3.2. SUBGROUP 2, STEADY-STATE LIFE TEST CONDITIONS, METHOD 1005 OF MIL-STD-883.

4.3.3.2.1. TEST CONDITION D USING THE CIRCUIT IN FIGURE 4.0 HEREIN, T_C = +125°C MINIMUM.

4.3.3.2.2. TEST DURATION: 1,000 HOURS(HRS), PER METHOD 1005 OF MIL-STD-883. READ AND RECORD THE 25°C ELECTRICAL PERFORMANCE TEST CHARACTERISTICS TABLE AT 168 +72/-0, AND 504 +168/-0 HRS. AT 0 AND 1000 +72/-0 HRS, READ AND RECORD THE FINAL ELECTRICAL TESTS TABLE AT -55°C, 25°C, AND 125°C.

4.3.3.3. END POINT ELECTRICAL PARAMETERS SHALL BE AS SPECIFIED IN ELECTRICAL CHARACTERISTICS TABLE HEREIN.

4.3.4. GROUP D INSPECTION: MULTICHIP MODULES SUPPLIED IN ACCORDANCE WITH THIS DRAWING SHALL BE CAPABLE OF MEETING QUALIFICATION TESTS. GROUP D INSPECTION SHALL BE IN ACCORDANCE WITH MIL-PRF-38534. POST BURN-IN ELECTRICAL REJECTS MAY BE UTILIZED. GROUP D INSPECTION CAN BE OMITTED BY SUPPLIER WITH SUBMITTAL OF ACCEPTABLE STATISTICAL DATA TO JUSTIFY OMISSION OF GROUP D TESTS.

4.3.4.1. LEAD INTEGRITY SHALL BE CONDITION B2 (LEAD FATIGUE).

4.3.4.2. SEAL (HERMETICITY) SHALL BE CONDITION C1 FOR GROSS LEAK.

4.4. QCI/QUALIFICATION TEST DATA: ALL ATTRIBUTES AND VARIABLES TEST DATA WHICH RESULTS FROM THE PERFORMANCE OF THE TESTS SPECIFIED. THE DATA SHALL BE LEGIBLE AND SHALL BE CORRELATABLE TO THE LOT DATE CODE AND MULTI-CHIP MODULE.

4.5. QCI/QUALIFICATION TEST SAMPLES: UPON COMPLETION OF QCI/QUALIFICATION TESTS SPECIFIED, ALL QCI/QUALIFICATION TEST SAMPLES SHALL BE IDENTIFIED.

5. PREPARATION FOR DELIVERY

5.1. PACKAGING, PACKING, AND PRESERVATION SHALL BE AS SPECIFIED.

6. NOTES

6.1. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS USED HEREIN ARE DEFINED IN MIL-PRF-38534 AND HEREIN.

6.2. CATASTROPHIC FAILURES: CATASTROPHIC FAILURES ARE DEFINED AS THOSE HYBRID MICROCIRCUITS WHICH EXHIBIT ELECTRICAL OPENS, SHORTS OR ARE NON-FUNCTIONAL.