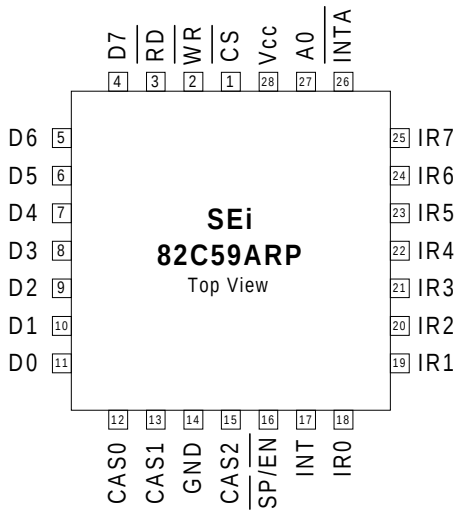
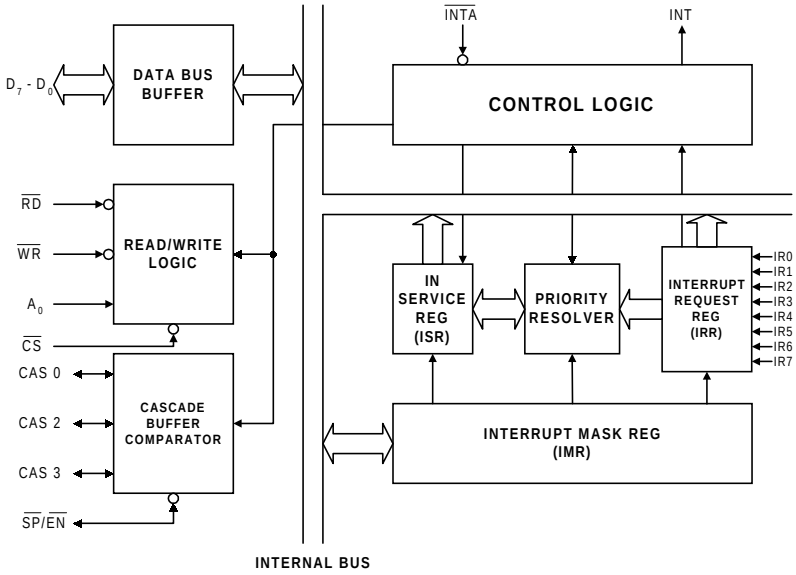
82C59ARP

RADIATION HARDENED CMOS PRIORITY INTERRUPT CONTROLLER





FEATURES:

- **Eight-level Priority Interrupt Controller**
- **RAD-PAK® radiation-hardened against natural space radiation**
- **Total dose hardness: > 100 krad (Si); dependent upon orbit**
- **Single event effect:**
  - **- SEL_{TH} LET: > 80 MeV/mg/cm²**
  - **- SEU_{TH} LET: 11.4 MeV/mg/cm²**
- **Package:**
  - **- 28-pin RAD-PAK® quad flat pack**
- **Low standby power < 10mA**
- **Expandable to 64-level priority controller**
- **Programmable interrupt modes**
- **80C86 compatible operation**
- **Fully static design**
- **Single 5V power supply**

DESCRIPTION:

Space Electronics' 82C59ARP (RP for RAD-PAK®) high-speed microcircuit features a typical 100 kilorad (Si) total dose tolerance; dependent upon orbit. Using SEi's radiation-hardened RAD-PAK® packaging technology, the 82C59ARP is a high-performance Priority Interrupt Controller. The 82C59ARP is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. It can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry. Individual interrupting sources can be masked or prioritized to allow custom system configuration. The fully static circuit design, requiring no clock input, ensures low operating power. Capable of surviving space environments, the 82C59ARP is ideal for satellite, spacecraft, and space probe missions. SEi's RAD-PAK® advanced technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. It is available with packaging and screening up to Class S.

82C59ARP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{SS}		+8.0	V
Input, Output or I/O Voltage		GND-0.5V	V_{CC} +0.5	V
Storage Temperature Range	T_s	-65	+150	◦C
Power Dissipation	P_D		1	W

82C59ARP DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Logical One Input Voltage		V_{IH}	2.0 2.2		V
Logical Zero Input Voltage		V_{IL}		0.8	V
Output HIGH Voltage	I_{OH} = -2.5mA	V_{OH}	3.0		V
	I_{OH} = -100µA		V_{CC} - 0.4		
Output LOW Voltage	I_{OL} = +2.5mA	V_{OL}		0.4	V
Input Leakage Current	V_{IN} = GND or V_{CC}	I_I	-1.0	+1.0	µA
Output Leakage Current	V_{OUT} = GND or V_{CC}	I_O	-10.0	+10.0	µA
IR Input Load Current	V_{IN} = 0V V_{IN} = V_{CC} All temperature ranges	I_{LIR}		-200 10	µA µA
Standby Power Supply Current	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Outputs Open	I_{CCSB}		10	µA
Operating Power Supply Current	V_{CC} = 5.0V V_{IN} = V_{CC} or GND Outputs Open T_A = 25 ◦C	I_{CCOP}		1	mA/MHz

82C59ARP CAPACITANCE
(T_A = 25 °C)

PARAMETER	SYMBOL	TYPICAL	UNITS
Input Capacitance	C_{IN}	15	pF
Output Capacitance	C_{OUT}	15	pF
I/O Capacitance	$C_{I/O}$	15	pF

82C59ARP AC CHARATERISTICS

(V_{CC} = +5.0V ± 10%, GND =0V, T_A = -55°C to +125°C, unless otherwise specified)

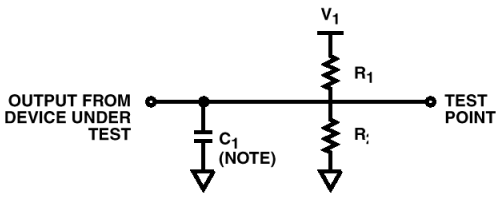
TIMING REQUIREMENTS

PARAMETER	SYMBOL	82C59ARP-5 MIN	82C59ARP-5 MAX	82C59ARP-8 MIN	82C59ARP-8 MAX	UNITS
A0/CS Setup to RD/INTA	(1) T_{AHRL}	10	-	10	-	ns
A0/CS Hold after RD/INTA	(2) T_{RHAX}	5	-	5	-	ns
RD/INTA Pulse Width	(3) T_{RLRH}	235	-	160	-	ns
A0/CS Setup to WR	(4) T_{AHWL}	0	-	0	-	ns
A0/CS Hold after WR	(5) T_{WHAX}	5	-	5	-	ns
WR Pulse Width	(6) T_{WLWH}	165	-	95	-	ns
Data Setup to WR	(7) T_{DVWH}	240	-	160	-	ns
Data Hold after WR	(8) T_{WHDX}	5	-	5	-	ns
Interrupt Request Width Low	(9) T_{JLJH}	100	-	100	-	ns
Cascade Setup to Second or Third INTA (Slave Only)	(10) T_{CVIAL}	55	-	40	-	ns
End of RD to next RD, End of INTA to next INTA (within an INTA sequence only)	(11) T_{RHRL}	160	-	160	-	ns
End of WR to next WR	(12) T_{WHWL}	190	-	190	-	ns
End of Command to next command (not same command type), End of INTA sequence to next INTA sequence	(13) T_{CHCL}	500	-	400	-	ns

TIMING RESPONSES

PARAMETER	SYMBOL	82C59ARP-5 MIN	82C59ARP-5 MAX	82C59ARP-8 MIN	82C59ARP-8 MAX	UNITS
Data Valid from RD/INTA	(14) T_{RLDV}	-	160	-	120	ns
Data Float after RD/INTA	(15) T_{RHDZ}	5	100	5	85	ns
Interrupt Output Delay	(16) T_{JHIH}	-	350	-	300	ns
Cascade Valid from First INTA (Master Only)	(17) T_{IALCV}	-	565	-	360	ns
Enable Active from RD or INTA	(18) T_{RLEL}	-	125	-	100	ns
Enable Inactive from RD or INTA	(19) T_{RHEH}	-	60	-	50	ns
Data Valid from Stable Address	(20) T_{AHDV}	-	210	-	200	ns
Cascade Valid to Valid Data	(21) T_{CVDV}	-	300	-	200	ns

AC Test Circuit

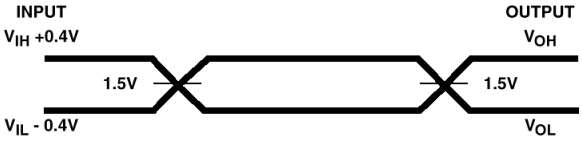


NOTE: Includes stray and jig capacitance.

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V_1	R_1	R_2	C_1
1	1.7V	523Ω	Open	100pF
2	V_{CC}	1.8kΩ	1.8kΩ	50pF

AC Testing Input, Output Waveform



NOTE: AC Testing: All input signals must switch between V_{IL} - 0.4V and V_{IH} + 0.4V. Input rise and fall times are driven at 1ns/V.

Timing Waveforms

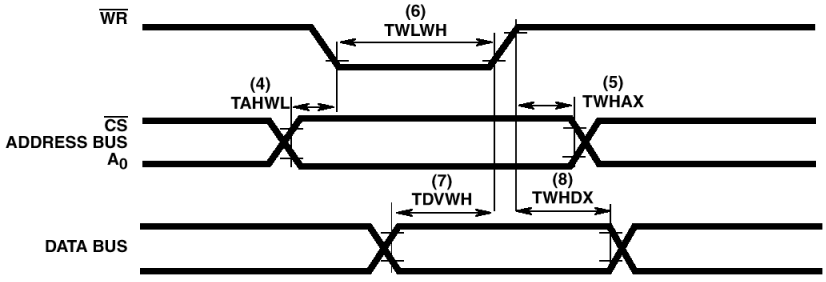


FIGURE 1. WRITE

Timing Waveforms **(Continued)**

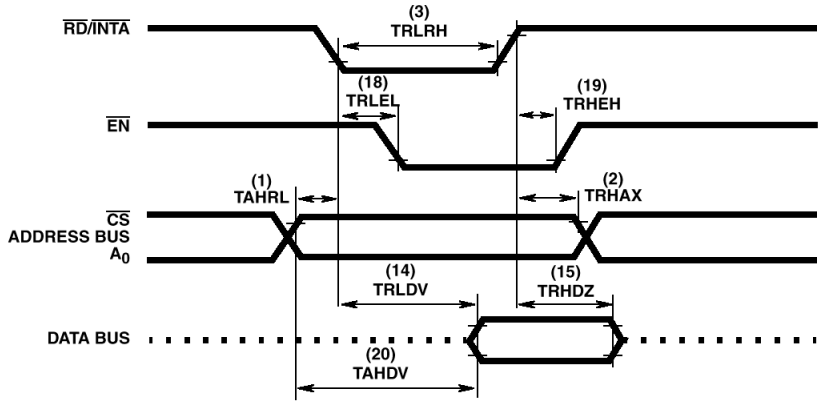


FIGURE 2. $\overline{\text{READ}}/\overline{\text{INTA}}$

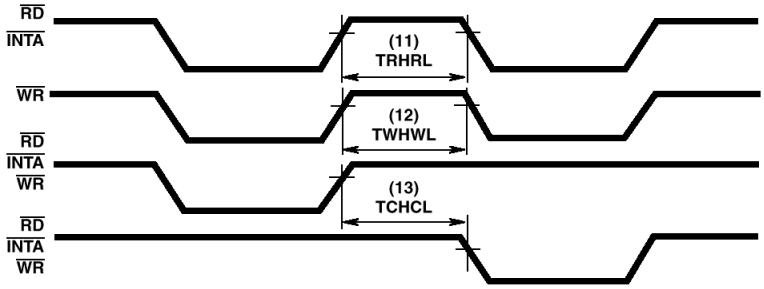
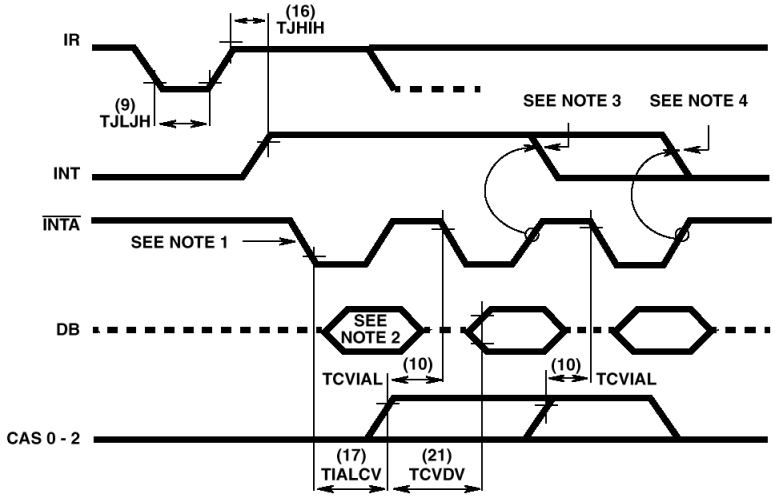


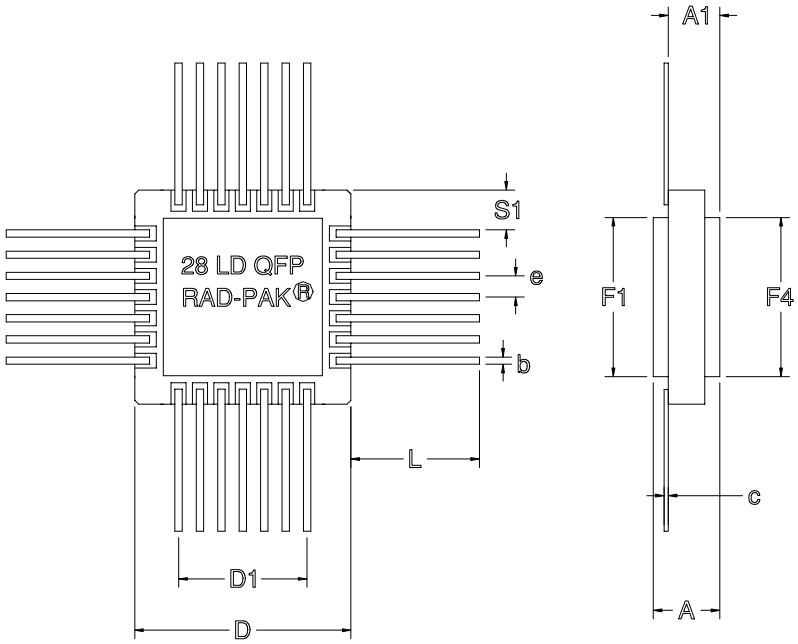
FIGURE 3. OTHER TIMING



NOTES:

1. Interrupt Request (IR) must remain HIGH until leading edge of first $\overline{\text{INTA}}$.
2. During first $\overline{\text{INTA}}$ the Data Bus is not active in 80C86/88/286 mode.
3. 80C86/88/286 mode.
4. 8080/8085 mode.

FIGURE 4. $\overline{\text{INTA}}$ SEQUENCE



28 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.147	0.161	0.175
b	0.016	0.018	0.020
c	0.005	0.006	0.007
D	0.442	0.450	0.460
D1		0.300 BSC	
e		0.050 BSC	
S1	0.013	0.066	--
F1	0.344	0.350	0.356
F4	0.370	0.375	0.380
L	0.265	0.275	0.285
A1	--	0.099	0.108
N		28	

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