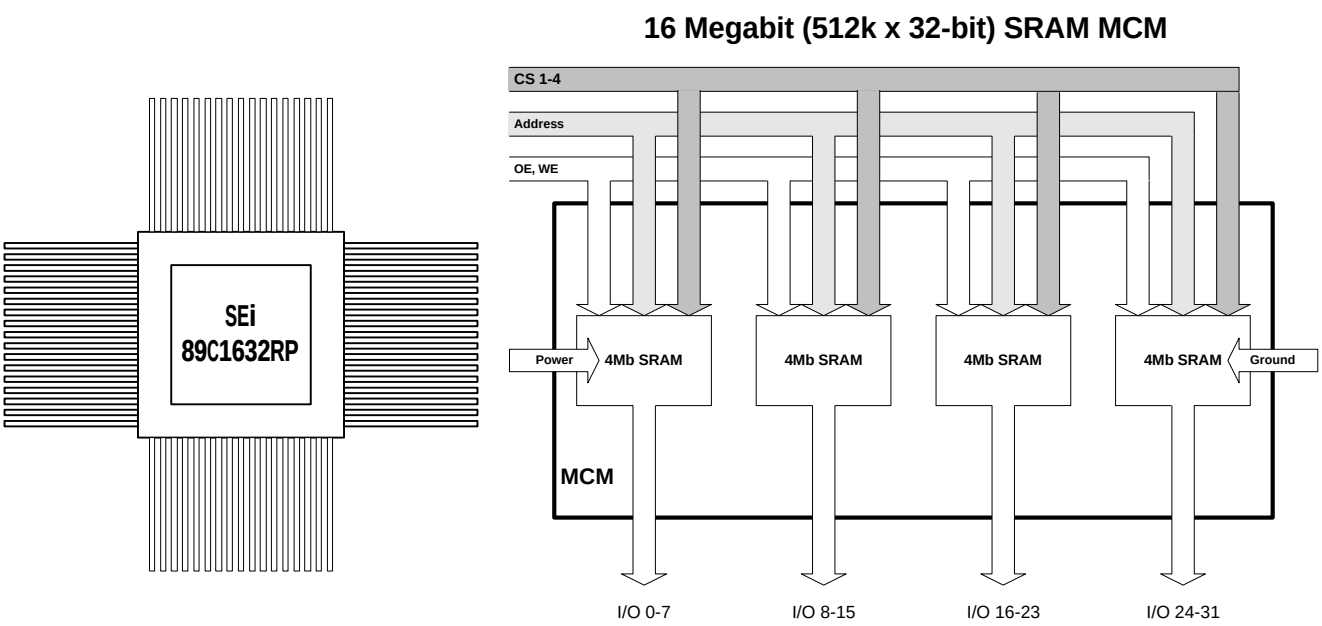
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

16 MEGABIT (512K X 32-BIT) MCM SRAM

89C1632RP



FEATURES:

- Four 512k x 8 SRAM architecture
- RAD-PAK® technology hardens against natural space radiation technology
- Total dose hardness: typical 100 krad (Si); dependent upon orbit
  - No single event latchup > 117 MeV/mg/cm^2
  - SEU threshold = 3 MeV/mg/cm^2
- Package: 68-pin quad flat package
- Fast access time: 25,30 ns
- Completely static memory - no clock or timing strobe required
- Internal bypass capacitor
- High-speed silicon-gate CMOS technology
- 5V or 3V ± 10% power supply
- Equal address and chip enable access times
- Three-state outputs
- All inputs and outputs are TTL compatible

DESCRIPTION:

Space Electronics' 89C1632RP (RP for RAD-PAK®) high-performance 16 Megabit Multi-Chip Module (MCM) Static Random Access Memory features a typical 100 kilorad (Si) total dose tolerance. The four 4-Megabyte SRAM die and bypass capacitors are incorporated into a high-reliable hermetic quad flat-pack ceramic package. With high-performance silicon-gate CMOS technology, the 89C1632RP reduces power consumption and eliminates the need for external clocks or timing strobes. It is equipped with output enable ($\overline{OE}$) and four byte enable ($\overline{CS1}$ - $\overline{CS4}$) inputs to allow greater system flexibility. When $\overline{OE}$ input is high, the output is forced to high impedance. The 89C1632RP has been specifically designed to meet exposure to radiation environments. It has a total-dose survivability of greater than 100 krad (Si), based on a GEO-type orbit (actual TID tolerance depends upon orbit and mission duration). Space Electronics' RAD-PAK® advanced technology incorporates radiation shielding in the microcircuit package that eliminates box shielding. The 89C1632RP is available in Class H or Class K packaging and screening.

(858) 503-3300 - Fax: (858) 503-3301 - www.spaceelectronics.com

TABLE 1. PIN DESCRIPTION

PIN	DESCRIPTION
A0-A18	Address Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Enable
I/O0-I/O31	Data Input/Output
NC	No Connection
V_{CC}	Power Supply
V_{SS}	Ground

89C1632RP PINOUT

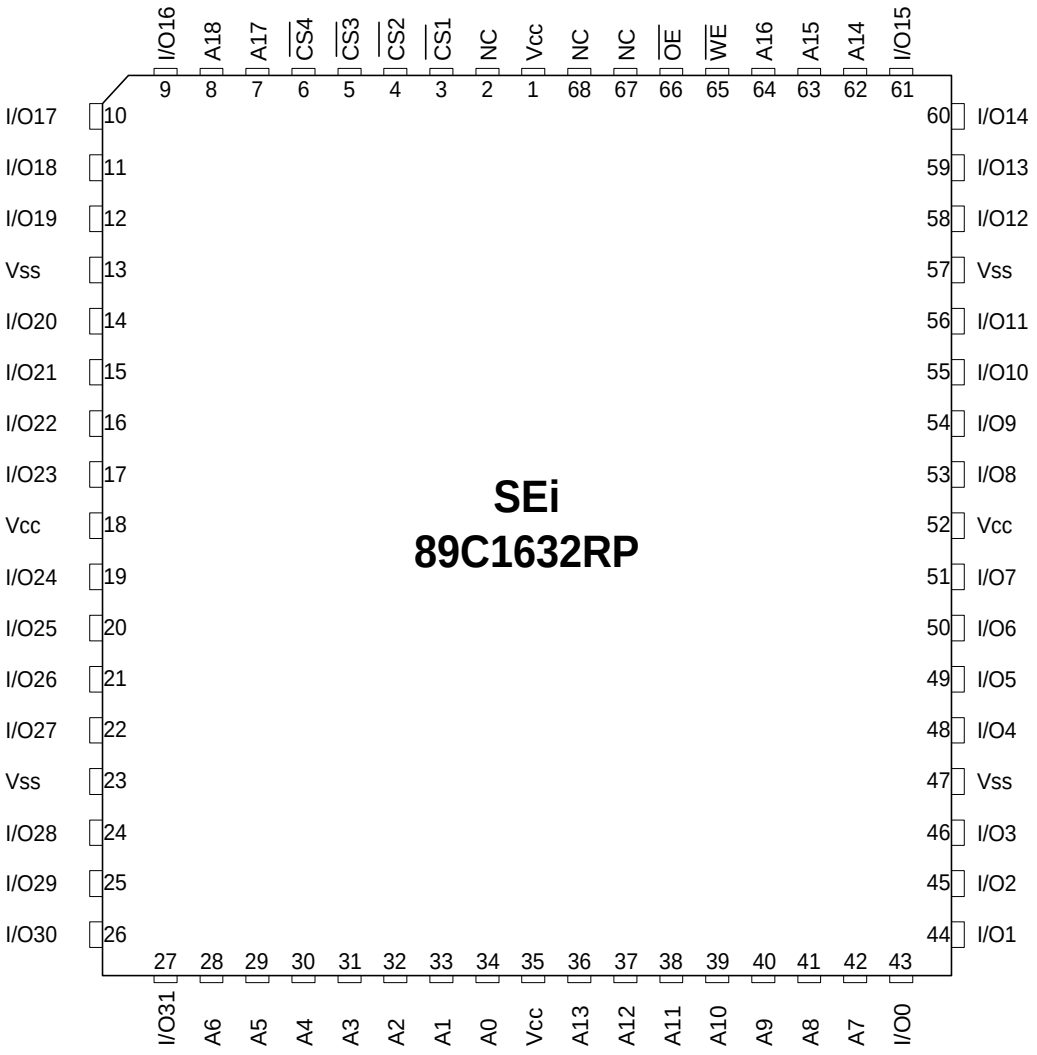


TABLE 2. 89C1632RP ABSOLUTE MAXIMUM RATINGS

(VOLTAGE REFERENCED TO V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage Relative to V_{SS}	V_{CC}	-0.5	+7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	-0.5	+0.5	V
Power Dissipation	P_D	--	4.0	W
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C

TABLE 3. 89C1632RP ABSOLUTE MAXIMUM RATINGS

(V_{CC} 2.7 - 5.5V, T_A = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage, (Operating Voltage Range)	V_{CC}	2.7	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.5 (1)	V
Input Low Voltage	V_{IL}	-0.5 (2)	0.8	V

1. V_{IH} (max) = V_{CC} + 2V ac (pulse width ≤ 10ns) for I ≤ 80 mA.
2. V_{IL} (min) = -2.0V dc; (pulse width ≤ 20 ns) for I ≤ 80 mA.

TABLE 4. 89C1632RP CAPACITANCE

(f = 1.0 MHz, dV = 3.0V, T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Input Capacitance $\overline{CS1}$ - $\overline{CS4}$, $\overline{OE}$, $\overline{WE}$ I/O0-7, I/O8-15, I/O16-23, I/O24-31	C_{IN}	V_{IN} = 0 V	 7 28 7	pF
Input / Output Capacitance	C_{OUT}	$V_{I/O}$ = 0 V	8	pF

TABLE 5. 89C1632RP DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	-8.0	+8.0	uA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	-8.0	+8.0	uA
Average Operating Current Cycle Time: 25 ns 30 ns	I_{CC}	Min. Cycle, 100% Duty, $\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{IN} = V_{IH} or V_{IL}	 -- --	 760 720	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}, cycle time ≥ 25ns	--	240	mA

TABLE 5. 89C1632RP DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
CMOS Standby Power Supply Current	I_{SB1}	$\overline{CS} \geq V_{CC}$ - 0.2V, f = 0 MHz, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} <$ 0.2V	--	60	mA
Output Low Voltage	V_{OL}	I_{OL} = + 8.0 mA	--	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA	2.4	--	V

TABLE 6. AC OPERATING CONDITIONS AND CHARACTERISTICS

PARAMETER	MIN	MAX	UNITS
Input Pulse Level	0.0	3.0	V
Output Timing Measurement Reference Level	--	1.5	V
Input Rise/Fall Time	--	3.0	ns
Input Timing Measurement Reference Level	--	1.5	V

TABLE 7. 89C1632RP READ CYCLE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Read Cycle Time	t_{RC}			ns
89C1632RP-25		25	--	
89C1632RP-30		30	--	
Address Access Time	t_{AA}			ns
89C1632RP-25		--	25	
89C1632RP-30		--	30	
Chip Select to Output	t_{CO}			ns
89C1632RP-25		--	25	
89C1632RP-30		--	30	
Output Enable to Output	t_{OE}			ns
89C1632RP-25		--	7	
89C1632RP-30		--	9	
Output Enable to Low-Z Output	t_{OLZ}			ns
89C1632RP-25		0	--	
89C1632RP-30		0	--	
Chip Enable to Low-Z Output	t_{ILZ}			ns
89C1632RP-25		3	--	
89C1632RP-30		3	--	
Output Disable to High-Z Output	t_{OHZ}			ns
89C1632RP-25		--	7	
89C1632RP-30		--	9	
Chip Disable to High-Z Output	t_{HZ}			ns
89C1632RP-25		--	7	
89C1632RP-30		--	9	

TABLE 7. 89C1632RP READ CYCLE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Output Hold from Address Change	t_{OH}			ns
89C1632RP-25		3	--	
89C1632RP-30		3	--	

TABLE 8. 89C1632RP WRITE CYCLE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Write Cycle Time	t_{WC}			ns
89C1632RP-25		25	--	
89C1632RP-30		30	--	
Chip Select to End of Write	t_{CW}			ns
89C1632RP-25		10	--	
89C1632RP-30		12	--	
Address Set-up Time	t_{AS}			ns
89C1632RP-25		0	--	
89C1632RP-30		0	--	
Address Valid to End of Write	t_{AW}			ns
89C1632RP-25		10	--	
89C1632RP-30		12	--	
Write Pulse Width ($\overline{OE}$ High)	t_{WP}			ns
89C1632RP-25		10	--	
89C1632RP-30		12	--	
Write Pulse Width ($\overline{OE}$ Low)	t_{WP}			ns
89C1632RP-25		12	--	
89C1632RP-30		14	--	
Write Recovery Time	t_{WR}			ns
89C1632RP-25		0	--	
89C1632RP-30		0	--	
Write to Output High-Z	t_{WHZ}			ns
89C1632RP-25		--	7	
89C1632RP-30		--	9	
Data to Write Time Overlap	t_{DW}			ns
89C1632RP-25		7	--	
89C1632RP-30		9	--	
Data Hold from Write Time	t_{DH}			ns
89C1632RP-25		0	--	
89C1632RP-30		0	--	
End Write to Output Low-Z	t_{OW}			ns
89C1632RP-25		3	--	
89C1632RP-30		3	--	

FIGURE 1. AC TEST LOADS

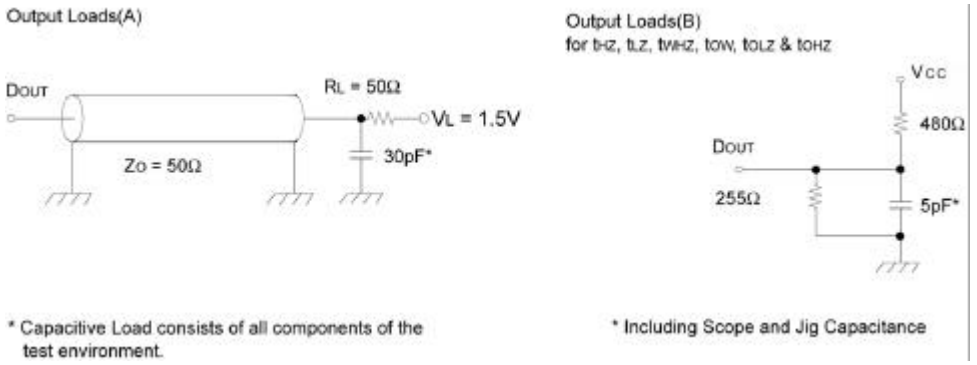


FIGURE 2. TIMING WAVEFORM OF READ CYCLE (1) (ADDRESS CONTROLLED)

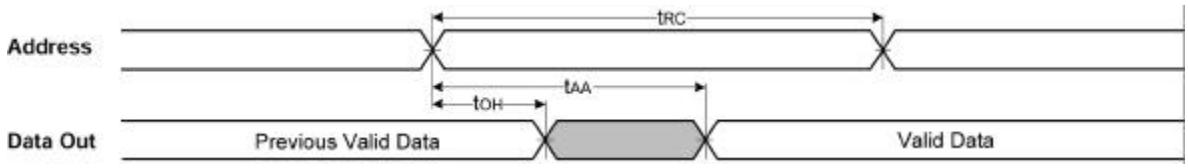
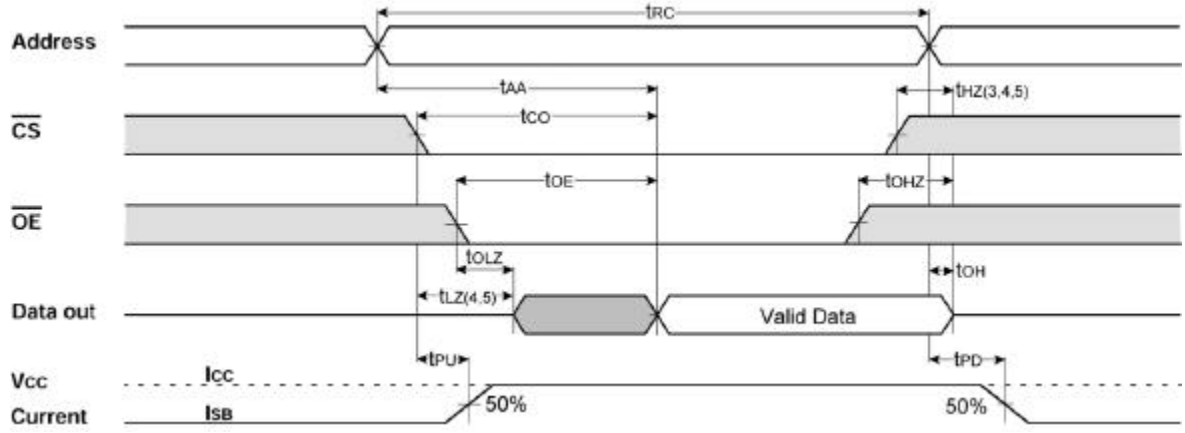


FIGURE 3. TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage conditions, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ = V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

FIGURE 4. TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ CLOCK)

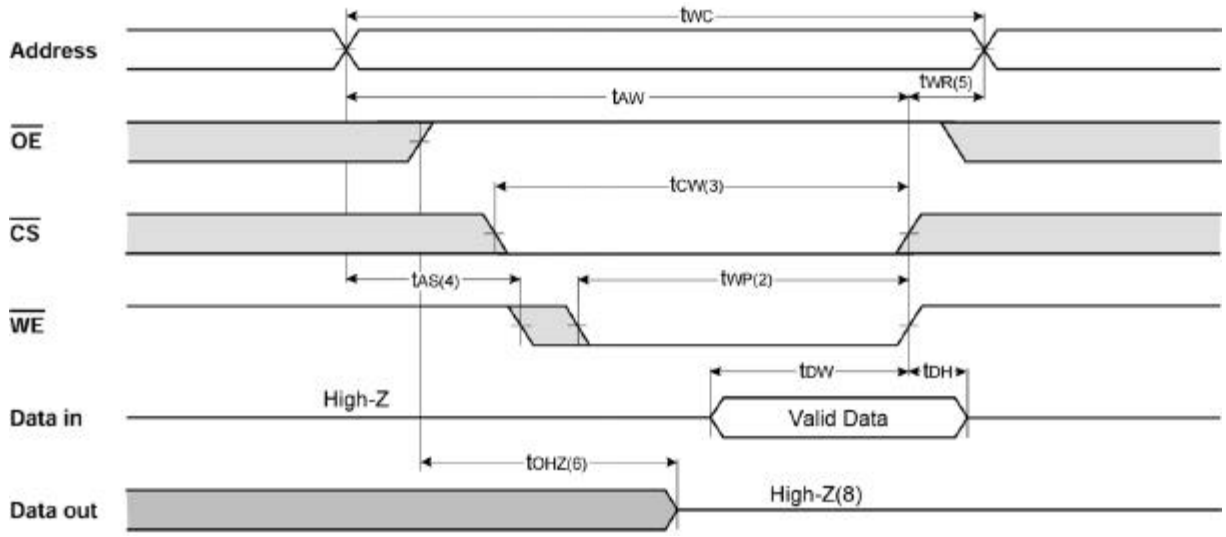


FIGURE 5. TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ LOW FIXED)

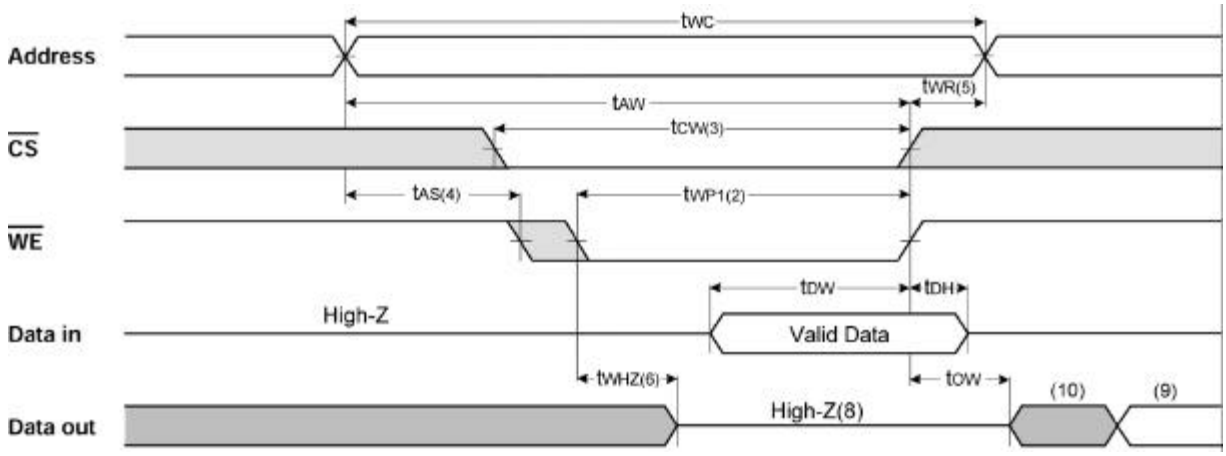
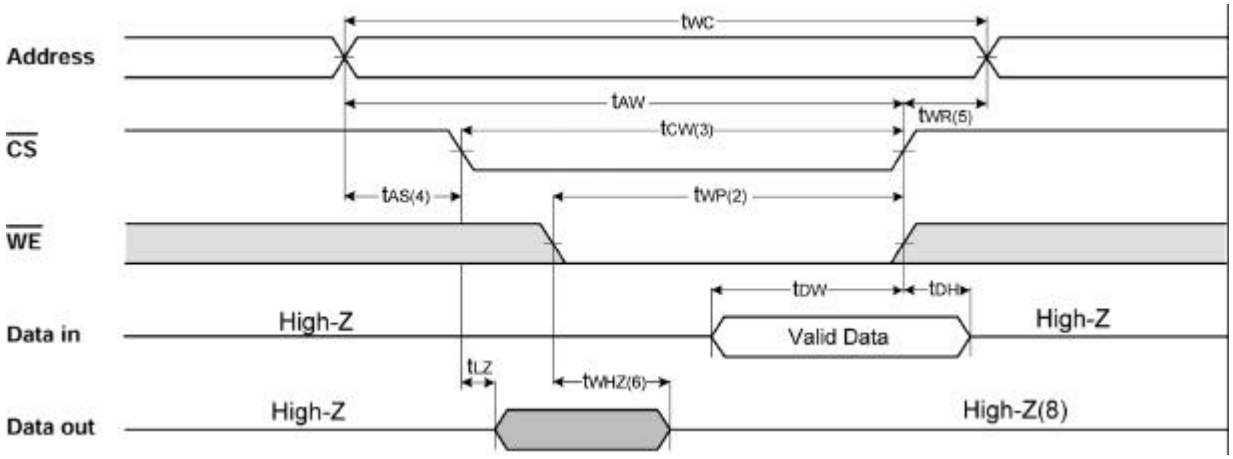
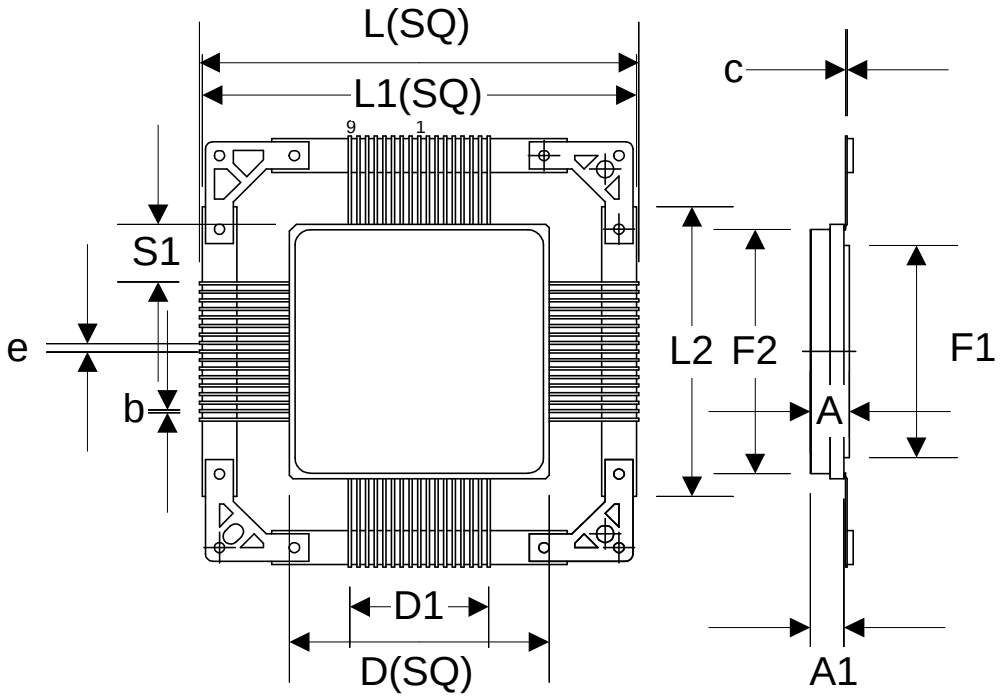


FIGURE 6. TIMING WAVEFORM OF WRITE CYCLE (3) ($\overline{CS}$ CONTROLLED)



1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization of elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ foes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low, I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.



68 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.206	0.225	0.244
b	0.015	0.017	0.018
c	0.008	0.009	0.0012
D	1.479	1.494	1.509
D1	--	0.800	--
L1	2.485	2.500	2.505
L2	1.690	1.700	1.710
A1	0.180	0.195	0.210
e	0.050 BSC		
S1	--	0.339	--
L	2.485	2.510	2.545
F1	1.239	1.244	1.249
F2	1.429	1.434	1.439
N	68		

Q68-04
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Space Electronics verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Space Electronics assumes no responsibility for the use of this information.

Space Electronics' products are not authorized for use as critical components in life support devices or systems without express written approval from Space Electronics.

Any claim against Space Electronics Inc. must be made within 90 days from the date of shipment from Space Electronics. Space Electronics' liability shall be limited to replacement of defective parts.