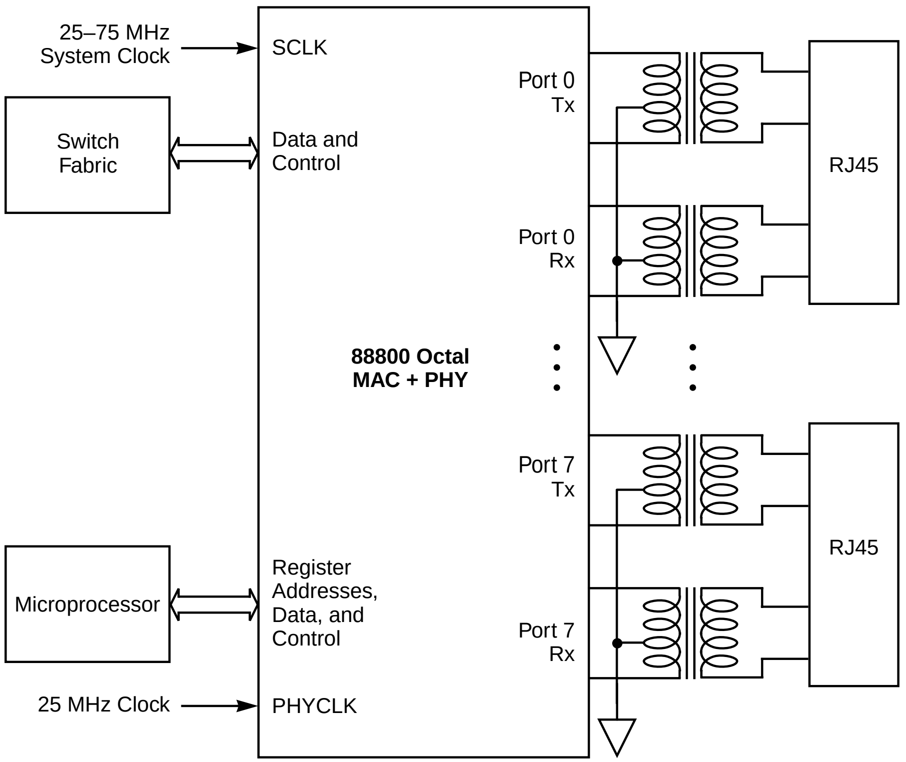
88800 Octal 10/100 Mbits/s Ethernet MAC + PHY Chip

Datasheet

The 88800 is a highly-integrated, octal, MAC + PHY chip for twisted pair and fiber Ethernet applications. The 88800 integrates eight Ethernet Media Access Controllers (MAC) and eight TX/FX/10BASE-T physical layer (PHY) modules.

Figure 1 shows a typical system application of the 88800. It connects eight ports between a switch fabric and RJ45 jacks for physical connection to an Ethernet LAN. A host microprocessor addresses registers in the chip for control and status.

Figure 1 Typical 88800 Application



Functional Description

Figure 2 shows a block diagram of the 88800. For each port, the device has a transmit data path and a receive data path. The transmit data path is from the System Interface to the Transmit FIFO, the MAC, and then out through the PHY to the media. Conversely, the receive data path is from the media, through the PHY and MAC, and out the Receive FIFO to the System Interface.

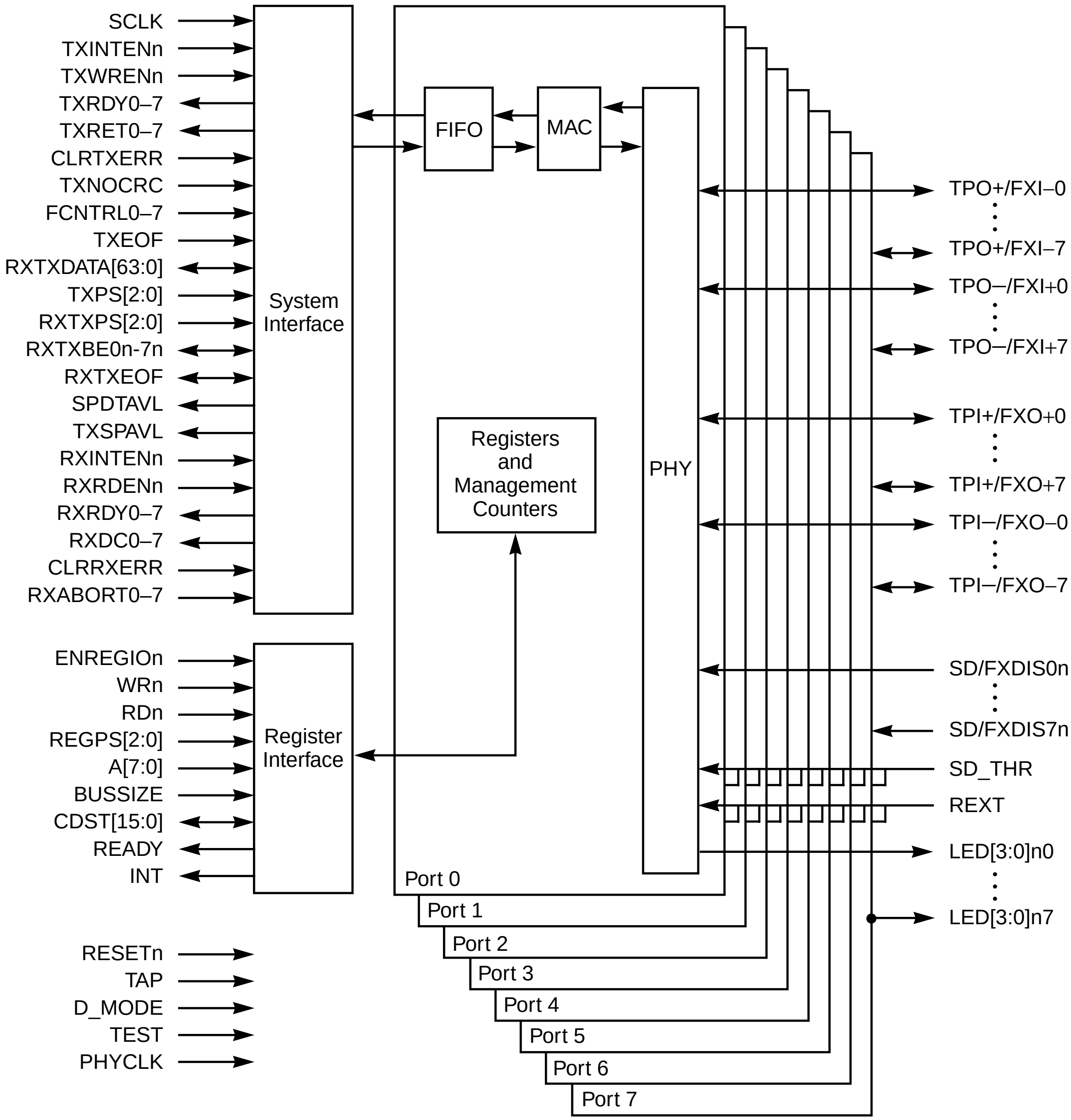
In the transmit data path, data for all eight ports is input into the System Interface from an external bus. One port is selected, and the data is sent to the transmit FIFO of that port. The transmit FIFO provides temporary storage of the data until it is sent to the MAC transmit section for that port. The MAC formats the data into an Ethernet packet per IEEE 802.3 specifications. The PHY transmit section encodes and scrambles the data, creates a waveshaped output waveform, and drives either a twisted pair cable or external fiber optic transceiver. The output waveform conforms to all IEEE 802.3 specifications.

The incoming serial data from either the twisted pair cable or an external fiber optic transceiver is input into the PHY receive section. The PHY receive section equalizes the input signal to compensate for the effects of the twisted pair cable; qualifies and converts the data to internal digital levels; extracts clock and data from the serial data stream; and descrambles and decodes the data into an Ethernet packet. The Ethernet packet is then sent to the MAC receive section for that port.

The MAC receive section decomposes the packet, checks the validity of the packet against certain error criteria and address filters, and checks for MAC Control frames. The MAC then sends valid packets to the receive FIFO for that port. The receive FIFO provides temporary storage of data until it is demanded by the System Interface.

The Register Interface is a separate, bidirectional, 16-bit data bus through which configuration inputs can be written to and status outputs can be read from the internal registers and management counters. There are eight identical register banks, one per port. In addition, port 0 contains a Configuration 6 register, Product ID register, and Interrupt Status register.

Figure 2 88800 Block Diagram



Features

- Single-chip MAC with integrated 100BASE-TX/100BASE-FX/10BASE-T physical layer
- Eight independent channels in one IC
- 3.3 V power supply with 5 V tolerant I/O
- Dual speed – 10/100 Mbits/s
- Full RMON, SNMP, and Ethernet management counter support per port
- 64-bit, 75 MHz system Interface to external bus (5 Gbits/s bandwidth)
- Flexible System Interface: bidirectional or separate RX and TX with 64-, 32-, or 16-bit width
- 16-bit interface to internal registers and management counters
- Independent 256-byte receive and transmit FIFOs per port with programmable watermarks
- Flow control for full- and half-duplex operation
- AutoNegotiation for 10/100 Mbits/s, full/half duplex
- Automatic cyclic redundancy check (CRC) generation and checking
- Retransmission of packet upon collision
- Automatic packet error discarding
- Programmable transmit start threshold
- Programmable backoff interval
- Interrupt capability
- On-chip wave shaping – no external filters required
- Adaptive equalizer and baseline wander correction for 100BASE-TX
- Meets all applicable IEEE 802.3 specifications
- 352-pin ball grid array (BGA) package

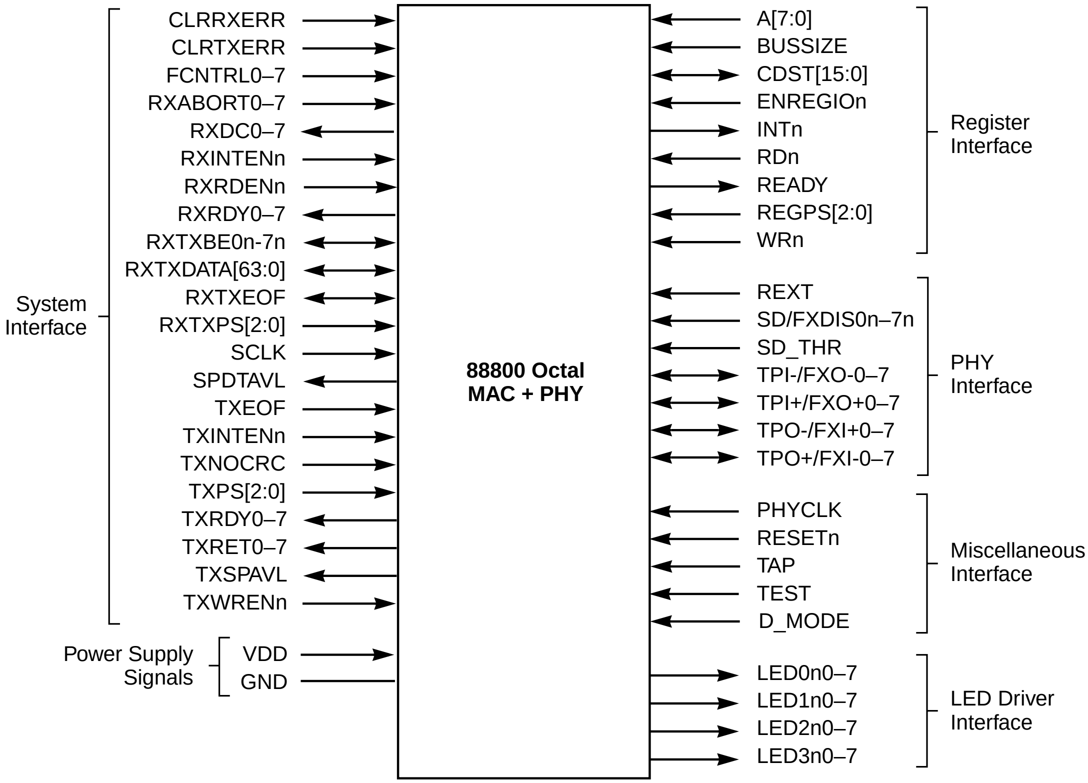
I/O Signal Descriptions

All of the chip's I/O signals are described in this section. As shown in Figure 3, they are organized into:

- System Interface Signals
- PHY Interface Signals
- Register Interface Signals
- LED Driver Signals
- Miscellaneous Signals
- Power Supply Signals

Signals with a lowercase "n" suffixed to their name are active LOW signals. Those signals without the "n" are active HIGH signals. When signals are asserted, they go to their active state. When signals are deasserted, they go to their inactive state.

Figure 3 I/O Signals Organization



System Interface Signals

RXINTENn **Receive Interface Enable** **Input**

When asserted in normal mode, this input enables the System Interface for a receive operation and enables the output drivers on RXDC0–7 and RXRDY0–7. The RXDC and RXRDY outputs are 3-stated when their drivers are disabled.

When asserted in D mode, this input enables the output drivers on RXRDY0–7. The RXDC0–7 output drivers are always enabled in D mode.

This input is latched on the rising edge of SCLK in both modes.

TXINTENn **Transmit Interface Enable** **Input**

When asserted in normal mode, this input enables the System Interface for a transmit operation and enables the output drivers on TXRET0–7 and TXRDY0–7. The TXRET and TXRDY outputs are 3-stated when their drivers are disabled.

When asserted in D mode, this input enables the output drivers on TXRDY0–7. The TXRET0–7 output drivers are always enabled in D mode.

This input is latched on the rising edge of SCLK in both modes.

RXRDENn **Receive Read Enable** **Input**

In normal mode, this input and RXINTENn must be asserted for data in the receive FIFO to be read on RXTXDATA[63:0] for the selected port.

In D mode, only this input needs to be asserted to read the data out of the FIFO.

This input is latched on the rising edge of SCLK in both modes.

TXWRENn **Transmit Write Enable** **Input**

In normal mode, this input and TXINTENn must be asserted for data on RXTXDATA[63:0] to be written into the transmit FIFO for the selected port.

In D mode, only this input needs to be asserted to write data into the FIFO.

This input is latched on the rising edge of SCLK in both modes.

SCLK **System Clock** **Input**

All System Interface inputs and outputs, including RXTXDATA[63:0], are clocked in and out of the device on the rising edges of SCLK. The frequency of SCLK must be between 25 and 75 MHz.

RXTXPS[2:0] **Receive-Transmit Port Select** **Input**

These inputs select which one of the eight ports is accessed over the System Interface. When the device is configured for bidirectional bus operation, these inputs are used for both transmit write and receive read operations. When the device is configured for split bus operation, these inputs are used for receive read operations only. These inputs are latched on the rising edges of SCLK.

RXTXPS[2:0]	Port	RXTXPS[2:0]	Port
0b000	0	0b100	4
0b001	1	0b101	5
0b010	2	0b110	6
0b011	3	0b111	7

TXPS[2:0] **Transmit Port Select** **Input**

These inputs select which one of the eight ports will be accessed over the System Interface. When the device is configured for bidirectional bus operation, these inputs are not used because RXTXPS[2:0] are used instead for both transmit write and receive read operations. When the device is configured for split bus operation, these inputs are used for transmit write operations only. These inputs are latched on the rising edges of SCLK.

TXPS[2:0]	Port	TXPS[2:0]	Port
0b000	0	0b100	4
0b001	1	0b101	5
0b010	2	0b110	6
0b011	3	0b111	7

RXTXBE0n-7n

Receive-Transmit Byte Enable **Input/Output**

These bidirectional, active-LOW signals indicate which bytes of each data word on RXTXDATA[63:0] contain valid data for the selected port. These inputs are latched on the rising edges of SCLK.

When the device is configured for bidirectional bus operation, these pins can carry either inputs or outputs. For transmit write operations, RXTXBE0n–7n are configured as inputs and select the bytes on RXTXDATA[63:0] to be loaded into the TX FIFO for the selected port. For receive read operations, RXTXBE0n–7n are configured as outputs and indicate which bytes being read out of the RX FIFO on RXTXDATA[63:0] contain valid data for the selected port.

When the device is configured for split bus operation, these pins carry either inputs or outputs. For transmit write operations, RXTXBE4n–7n are always configured as inputs and select which bytes on RXTXDATA[63:32] are loaded into the TX FIFO for the selected port. For receive read operations, RXTXBE0n–3n are always configured as outputs and indicate which bytes being read out of the RX FIFO on RXTXDATA[31:0] contain valid data for the selected port.

RXRDY0–7 **Receive FIFO Ready** **Output**

These outputs, one per port, indicate that the RX FIFO data has either exceeded the programmable threshold value, or the end of a packet was loaded into the RX FIFO. These outputs are latched on the rising edge of SCLK and are put in a high-impedance state when RXINTENn is deasserted.

1 = RX FIFO data ≥ RX FIFO threshold or end of frame loaded into RX FIFO

0 = RXFIFO data below threshold

RXRDY0 can be configured to indicate Port 0 or the selected port by appropriately setting the watermark pin map select bit.

TXRDY0–7 **Transmit FIFO Ready** **Output**

These outputs, one per port, indicate that the TX FIFO space exceeds the programmable threshold value. These outputs are latched on the rising edge of SCLK and are put in a high-impedance state when TXINTENn is deasserted.

1 = TX FIFO space ≥ TX FIFO threshold

0 = TXFIFO space below threshold

TXRDY0 can be configured to indicate Port 0 or the selected port by appropriately setting the watermark pin map select bit.

SPDTAVL **FIFO Space/Data Available** **Output**

This output, latched on the rising edge of SCLK, applies to the selected port. It is defined as:

Operation/Mode	SPDTAVL Meaning
RX FIFO Reads/ Bidirectional and Split Bus Modes	HIGH = more than one doubleword of data is in RX FIFO LOW = space not available in RX FIFO
TX FIFO Reads/ Bidirectional Bus Mode Only	HIGH = more than two doublewords of FIFO space are available LOW = space not available in TX FIFO

TXSPAVL **TX FIFO Space Available** **Output**

This output, latched on the rising edges of SCLK, applies to the selected port in split bus mode:

HIGH = More than two doublewords of TX FIFO space

LOW = Space not available in TX FIFO

This pin is not used in bidirectional bus mode.

RXTXEOF **Receive-Transmit End of Frame** **Input/Output**

This bidirectional signal indicates that the current data word is the last word of the packet (end-of-frame indicator) for the selected port. This signal is latched on the rising edge of SCLK.

When the device is configured for bidirectional bus operation, this signal can be either an input or output. During transmit writes, this signal is an input and needs to be asserted when the last word of the packet is being written into the transmit FIFO on RXTXDATA[63:0].

During receive reads, this signal is an output and is asserted when the last word of a receive packet is being read out of the receive FIFO on RXTXDATA[63:0].

When the device is configured for split bus operation, this signal is always an output and is asserted during receive reads when the last word of a receive packet is being read out of the receive FIFO on RXTXDATA[63:32].

TXEOF **Transmit End of Frame** **Input**

In split bus operation, this input signal is asserted during transmit writes to indicate that the current data word is the last word of the packet (end-of-frame indicator) for the selected port. This signal is latched on the rising edge of SCLK.

This signal is ignored when the device is configured for bidirectional bus operation because RXTXEOF contains the necessary end-of-frame information for both transmit write and receive read operations.

TXNOCRC **Transmit No CRC** **Input**

This input, latched on the rising edge of SCLK, applies to the selected port.

1 = CRC is not appended.

0 = CRC is calculated and appended to the current transmit packet being input on the System Interface.

RXTXDATA[63:0]

Receive-Transmit Data **Input/Output**

This bidirectional bus carries data read to or written from the FIFO for the selected port. The data is latched on the rising edge of SCLK.

When the device is configured for bidirectional bus operation, these lines can be either inputs or outputs. For transmit write operations, RXTXDATA[63:0] are inputs and carry data to be written to the transmit FIFO. For receive read operations, RXTXDATA[63:0] are outputs and carry data read from the receive FIFO.

When the device is configured for split bus operation, these lines are either inputs or outputs. For transmit write operations, RXTXDATA[63:32] are inputs and carry data to be written to the transmit FIFO. For receive read operations, RXTXDATA[31:0] are outputs and carry data read from the receive FIFO.

RXABORT0–7 Receive Abort **Input**

These inputs, one per port, are latched on the rising edge of SCLK.

1 = Abort packet, discard RX FIFO data, and block RX FIFO input until start of next packet

0 = No discard

RXDC0–7 Receive Discard **Output**

1 = RX FIFO data discarded due to receive error

0 = No discard

These outputs, one per port, are enabled when RXINTENn is asserted and latched on the rising edge of SCLK. They are placed in a high-impedance state when RXINTENn is deasserted. RXDC0–7 are latched HIGH until cleared with the CLRRXERR signal. As long as RXDC0–7 are latched HIGH, no new packets are loaded into the receive FIFO. Setting the discard pin map select bit (DISMAP) to the appropriate state configures the RXDC[0] pin to indicate Port 0 or the selected port.

In D mode, the output drivers on RXDC0–7 are always enabled.

TXRET0–7 Transmit Retry **Output**

1 = TX FIFO data discarded due to transmit error

0 = No discard

These outputs, one per port, are enabled when TXINTENn is asserted and latched on the rising edge of SCLK. They are placed in a high-impedance state when TXINTENn is deasserted. TXRET0–7 are latched HIGH until cleared with the CLRTXERR signal. As long as TXRET0–7 are latched HIGH, no new packets can be transmitted out of the transmit FIFO. TXRET0 can be configured to indicate Port 0 or the selected port by appropriately setting the discard pin map select bit.

In D mode, the output drivers on TXRET0–7 are always enabled.

CLRRXERR Clear Receive Error **Input**

This input is latched on the rising edge of SCLK.

1 = RXDC0–7 lines are cleared for the selected port.

0 = Not cleared.

CLRTXERR **Clear Transmit Error** **Input**

This input is latched on the rising edge of SCLK.

1 = TXRET0–7 lines are cleared for the selected port.

0 = Not cleared

FCNTRL0–7 **Flow Control** **Input**

These inputs, one per port, are latched on the rising edge of SCLK.

In Half-Duplex mode:

1 = JAM packet transmitted when receive data detected

0 = Normal operation

In Full-Duplex mode:

1 = MAC control pause frames transmitted when receive data detected.

0 = Normal operation

PHY Interface Signals

TPO+/FXI–0–7

Twisted Pair Transmit, Positive
FX Receive, Negative **Output/Input**

The SD/FXDIS0n–7n signals control the operation of the TPO+/FXI–0–7 pins. The TPO+/FXI–0–7 pins function as twisted-pair outputs or fiber optic inputs, based on the states of the corresponding SD/FXDIS0n–7n signals. For more details, see the SD/FXDIS0n–7n signal description on page 14.

TPO–/FXI+0–7

Twisted Pair Transmit, Negative
FX Receive, Positive **Output/Input**

The SD/FXDISn0–7 signals control the operation of the TPO–/FXI+0–7 pins. The TPO–/FXI+0–7 pins function as twisted-pair outputs or fiber-optic inputs, based on the states of the corresponding SD/FXDIS0n–7n signals. For more details, see the SD/FXDIS0n–7n signal description on page 14.

TPI+/FXO+0–7

Twisted Pair Receive, Positive
FX Transmit, Positive **Input/Output**

The SD/FXDIS0n–7n signals control the operation of the TPI+/FXO+0–7 pins. The TPI+/FXO+0–7 pins function as twisted-pair (TP) inputs or fiber-optic outputs, based on the states of the corresponding SD/FXDIS0n–7n signals. For more details, see the SD/FXDIS0n–7n signal description on page 14.

TPI–/FXO–0–7 **Twisted Pair Receive, Negative**
FX Transmit, Negative **Input/Output**

The SD/FXDIS0n–7n signals control the operation of the TPI–/FXO–0–7 pins. The TPI–/FXO–[7:0] pins function as twisted-pair inputs or fiber optic outputs, based on the states of the corresponding SD/FXDIS0n–7n signals. For more details, see the SD/FXDIS0n–7n FX signal description on page 14.

SD/FXDIS0n–7n

FX Signal Detect/FX Interface Disable **Input**

When these pins are not tied to ground, the FX interface for the corresponding port is enabled and the pins carry signal detect emitter-coupled logic (ECL) inputs. The trip point for the ECL inputs is determined by the voltage on SD_THR.

When these pins are tied to ground, the FX interface is disabled and the TP interface is enabled.

SD_THR **Signal Detect Input Threshold Level Set** **Input**

The voltage on this pin determines the ECL threshold level (trip point) for the SD input signals so that the device can directly interface to both 3.3 V and 5 V fiber optic transceivers. Typically, this pin is either tied to ground (for 3.3 V) or to an external voltage divider (for 5 V).

REXT **Transmit Current Set** **Input**

An external resistor connected between this pin and ground sets the output current for the TP and FX transmit outputs.

Register Interface Signals

ENREGIOn — **Enable Register I/O Operation** — **Input**

This input must be asserted to enable reading and writing of data on the Register Interface input and output signals. This input is clocked in on the falling edge of WRn or RDn.

WRn — **Write Strobe** — **Input**

This input is a write enable signal that must be asserted for data to be written into the addressed register for a given port.

RDn — **Read Strobe** — **Input**

This input is a read enable signal that must be asserted for data to be read from the addressed register for a given port. This input must remain asserted until data is placed on CDST[15:0] or until the READY output is asserted.

REGPS[2:0] — **Register Port Select** — **Input**

These inputs determine which ports' registers are being accessed over the Register Interface. These inputs are clocked on the falling edge of WRn or RDn.

REGPS[2:0]	Port	REGPS[2:0]	Port
0b000	0	0b100	4
0b001	1	0b101	5
0b010	2	0b110	6
0b011	3	0b111	7

A[7:0] — **Register Select Address** — **Input**

These inputs provide the address for the specific internal register to be accessed for a selected port. These inputs are clocked on the falling edge of WRn or RDn.

BUSSIZE — **Register Interface Bus Size Select** — **Input**

This bit selects the width of the register interface bus as follows:

1 = Register Interface bus is 16 bits wide on CDST[15:0].

0 = Register Interface bus is 8 bits wide on CDST[7:0].

CDST[15:0] **Register Data** **Input/Output**

This bidirectional bus is the 16-bit data path to and from the internal registers for a selected port. Data is read/written from/to the internal registers on the falling edge of WRn or RDn. These lines are high impedance until their output drivers are enabled by asserting RDn and ENREGIOn.

READY **Register Ready Indication** **Output**

This output is asserted to indicate that data being read out on CDST[15:0] is valid. READY is asserted only after RDn has been asserted and stays asserted until after RDn is deasserted.

INTn **Interrupt Output** **O.D. with Pull-Up**

This open drain output with resistor pullup is asserted when there is an interrupt on any port.

LED Driver Signals

LED3n0–7 **LED 3** **Output**

These output signals, one per port, can be programmed through an internal register to indicate any one of 16 events. The default value for these outputs is Link Detect. These signals can drive an LED tied to VDD or ground.

When programmed as Link Detect output (default):

1 = No detect

0 = Link detected

LED2n0–7 **LED 2** **Output**

These output signals, one per port, can be programmed though an internal register to indicate any one of 16 events. The default value for these outputs is Activity. These signals can drive an LED tied to VDD or ground.

When programmed as Activity output (default):

1 = No activity

0 = Transmit or receive packet occurred (held LOW for 100 ms)

LED1n0–7 **LED 1** **Output**

These output signals, one per port, can be programmed though an internal register to indicate any one of 16 events. The default value for these outputs is Full-Half-duplex Detect. These signals can drive an LED tied to VDD or ground.

When programmed as Full-Half-duplex Detect output (default):

1 = Half duplex

0 = Full duplex

LED0n0–7 **LED 0** **Output**

These output signals, one per port, can be programmed though an internal register to indicate any one of 16 events. The default value for these outputs is 10/100 Speed Detect. These signals can drive an LED tied to VDD or ground.

When programmed as 10/100 Speed Detect output (default):

1 = 10 Mbits/s

0 = 100 Mbits/s

Miscellaneous Signals

RESETn **Reset** **Input**

1 = Normal

0 = Device reset (FIFOs cleared, counters cleared, register bits set to defaults)

TAP **3-State All Output Pins** **Input**

This pin is used for testing purposes only.

1 = All output and bidirectional pins placed in high impedance state

0 = Normal operation

D_MODE **D Mode Enable** **Input**

1 = D mode

0 = Normal mode

TEST **Test Mode Enable** **Input**
This pin, reserved for factory use, must be tied LOW for proper device operation.

PHYCLK **PHY Clock** **Input**
This input is used to generate internal clocks for the PHY section. There must be a 25 MHz clock signal applied to this pin.

Power Supply Signals

VDD **Positive Supply** **Input**
+3.3 V (+ 5%) Volts

GND **Ground** **–**
0 Volts

Specifications

The specifications included are the Absolute Maximum Ratings, DC Characteristics, Pin Layout and Signal Assignments, and the Package Drawing. Refer to the technical manual for AC timing.

Absolute Maximum Ratings

Absolute maximum ratings are limits which, if exceeded, may cause permanent damage to the device or affect device reliability. All voltages listed in Table 1 are with respect to GND unless otherwise specified.

Table 1 Absolute Maximum Ratings

Parameter	Rating
VDD Supply Voltage	–0.3 V to +4.0 V
All Inputs	–0.3 V to +5.5 V
All Outputs	+0.3 V to +5.5 V
Input Latchup Current	±100 mA
Package Power Dissipation	7.5 Watt @ 70 ˚C
Storage Temperature	–65 to +150 ˚C
Temperature Under Bias	–10 to +80 ˚C
Lead Temperature (Soldering, 10 s)	260 ˚C
Body Temperature (Soldering, 10 s)	220 ˚C

DC Characteristics

The DC characteristics of the chip are listed in Table 2. Unless otherwise noted, all test conditions are as follows:

T_A = 0 to +70 ˚C
V_{DD} = + 3.3 V ± 5%
SCLK = 75 MHz + 0.01%
REXT = 10 kΩ + 1%, No Load

Table 2 DC Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage			0.8	V	All inputs except SCLK
				0.6	V	SCLK
V_{IH}	Input High Voltage	2.0			V	All inputs except SCLK
		2.4			V	SCLK
I_{IL}	Input Low Current			1	µA	V_{IN} = GND
I_{IH}	Input High Current			1	µA	$V_{IN} = V_{DD,}$ all signals except INTn
		12		50	µA	INTn
I_{OZ}	Output Hi-Z Current			10	µA	V_{OUT} = GND – V_{DD}, output in high-impedance state
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = –2 mA All except RXTXDATA[63:0], RXTXEOF, TXRDY0–7, RXRDY0–7, TXRET0–7, RXDC0–7, LEDn[3:0]0–7
				0.4	V	I_{OL} = –8 mA RXRXDATA[63:0], RXTXEOF, TXRDY0–7, RXRDY0–7, TXRET0–7, RXDC0–7
				0.4	V	I_{OL} = –20 mA LEDn[3:0]0–7
V_{OH}	Output High Voltage	2.4			V	I_{OL} = 2 mA All except RXRXDATA[63:0], RXTXEOF, TXRDY0–7, RXRDY0–7, TXRET0–7, RXDC0–7, LEDn[3:0]0–7
		2.4			V	I_{OL} = 8 mA RXRXDATA[63:0], RXTXEOF, TXRDY0–7, RXRDY0–7, TXRET0–7, RXDC0–7
		2.4			V	I_{OL} = 20 mA LEDn[3:0]0–7

Table 2 DC Characteristics (Cont.)

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
C_{IN}	Input Capacitance		5		pF	
C_{IO}	I/O Capacitance		5		pF	
I_{VDD}	V_{DD} Supply Current			1300	mA	Transmitting 100%, 100 Mbits/s
				1300	mA	Transmitting 100%, 10 Mbits/s
I_{GND}	GND Supply Current			1800	mA	Transmitting 100%, 100 Mbits/s[1]
				1800	mA	Transmitting 100%, 10 Mbits/s[1]

1. I_{GND} includes current flowing into GND from the external resistors and transformer on TPO+/–.

Pin Layout and Signal Assignments

Figure 4 shows the ball grid layout and signal assignments for the 88800 package.

Figure 4 88800 352-Pin BGA Special Assignments

A1 GND	A2 GND	A3 GND	A4 TPI–/ FXO–_7	A5 TPO–/ FXI+_7	A6 TPO–/ FXI+_6	A7 TPi–/ FXO–_6	A8 REXT	A9 TPI–/ FXO–_5	A10 TPO–/ FXI+_5	A11 TPO–/ FXI+_4	A12 TPI–/ FXO–_4	A13 GND
B1 GND	B2 VDD	B3 GND	B4 TPI+/ FXO+_7	B5 TPO+/ FXI–_7	B6 TPO+/ FXI–_6	B7 TPI+/ FXO+_6	B8 GND	B9 TPI+/ FXO+_5	B10 TPO+/ FXI–_5	B11 TPO+/ FXI–_4	B12 TPI+/ FXO+_4	B13 VDD
C1 FCNTRL_6	C2 GND	C3 VDD	C4 SD/ FXDISn_7	C5 GND	C6 VDD	C7 SD/ FXDISn_6	C8 VDD	C9 SD/ FXDISn_5	C10 GND	C11 VDD	C12 SD/ FXDISn_4	C13 GND
D1 LED3_4n	D2 FCNTRL_7	D3 FCNTRL_4	D4 VDD	D5 VDD	D6 GND	D7 GND	D8 VDD	D9 GND	D10 VDD	D11 VDD	D12 GND	D13 VDD
E1 LED3_5n	E2 LED2_4n	E3 TEST0	E4 FCNTRL_5									
F1 LED3_6n	F2 LED2_5n	F3 LED1_4n	F4 TEST1									
G1 LED1_6n	G2 LED2_6n	G3 LED1_5n	G4 LED0_4n									
H1 LED1_7n	H2 LED0_6n	H3 VDD	H4 LED0_5n									
J1 RXRDY_6	J2 LED0_7n	J3 LED3_7n	J4 VDD									
K1 TXRDY_7	K2 RXRDY_5	K3 RXRDY_7	K4 LED2_7n									
L1 TXRDY_5	L2 TXRDY_6	L3 RXRDY_4	L4 VDD									
M1 RXABORT_6	M2 RXABORT_ 7	M3 TXRDY_4	M4 VDD									
N1 GND	N2 RXDC_7	N3 RXABORT_4	N4 RXABORT_ 5									
P1 GND	P2 RXDC_6	P3 VDD	P4 RXDC_5									
R1 RXDC_4	R2 TXRET_7	R3 TXRET_6	R4 TXRET_4									
T1 TXRET_5	T2 RXTXBE3n	T3 RXTXBE1n	T4 RXTXBE7n									
U1 RXTXBE2n	U2 RXTXBE0n	U3 RXTXBE6n	U4 RXINTENn									
V1 VDD	V2 RXTXBE5n	V3 TXINTENn	V4 VDD									
W1 RXTXBE4n	W2 RXRDENn	W3 VDD	W4 RXTXPS1									
Y1 TXWRENn	Y2 SCLK	Y3 RXTXPS0	Y4 TXPS0									
AA1 RXTXPS2	AA2 TXPS2	AA3 SPDTAVL	AA4 TXEOF									
AB1 TXPS1	AB2 TXSPAVL	AB3 VDD	AB4 CLRTXERR									
AC1 RXTXEOF	AC2 TXNOCRC	AC3 RXTXDATA 32	AC4 VDD	AC5 RXTXDATA 34	AC6 RXTXDATA 38	AC7 RXTXDATA 41	AC8 RXTXDATA 45	AC9 VDD	AC10 RXTXDATA 52	AC11 RXTXDATA 56	AC12 RXTXDATA 61	AC13 RXTSDATA 1
AD1 CLRRXERR	AD2 GND	AD3 VDD	AD4 RXTXDATA 33	AD5 RXTXDATA 37	AD6 VDD	AD7 RXTXDATA 44	AD8 RXTXDATA 48	AD9 RXTXDATA 51	AD10 RXTXDATA 54	AD11 RXTXDATA 58	AD12 RXTXDATA 62	AD13 RXTXDATA 2
AE1 GND	AE2 VDD	AE3 GND	AE4 RXTXDATA 36	AE5 RXTXDATA 40	AE6 RXTXDATA 43	AE7 RXTXDATA 47	AE8 RXTXDATA 50	AE9 RXTXDATA 53	AE10 RXTXDATA 57	AE11 RXTXDATA 60	AE12 RXTXDATA 63	AE13 RXTXDATA 3
AF1 GND	AF2 GND	AF3 RXTXDATA 35	AF4 RXTXDATA 39	AF5 RXTXDATA 42	AF6 RXTXDATA 46	AF7 RXTXDATA 49	AF8 VDD	AF9 RXTXDATA 55	AF10 RXTXDATA 59	AF11 VDD	AF12 RXTXDATA 0	AF13 GND

Figure 4 88800 352-Pin BGA Package Drawing (Cont.)

A14 GND	A15 TPI–/ FXO–_3	A16 TPO–/ FXI+_3	A17 TPO–/ FXI+_2	A18 TPI–/ FXO–_2	A19 SD_THR	A20 TPI–/ FXO–_1	A21 TPO–/ FXI+_1	A22 TPO–/ FXI+_0	A23 TPI–/ FXO–_0	A24 GND	A25 GND	A26 GND
B14 VDD	B15 TPI+/ FXO+_3	B16 TPO+/ FXI–_3	B17 TPO+/ FXI–_2	B18 TPI+/ FXO+_2	B19 GND	B20 TPI+/ FXO+_1	B21 TPO+/ FXI–_1	B22 TPO+/ FXI–_0	B23 TPI+/ FXO+_0	B24 GND	B25 VDD	B26 GND
C14 GND	C15 SD/ FXDISn_3	C16 VDD	C17 GND	C18 SD/ FXDISn_2	C19 VDD	C20 SD/ FXDISn_1	C21 VDD	C22 GND	C23 SD/ FXDISn_0	C24 VDD	C25 GND	C26 FCNTRL_1
D14 VDD	D15 GND	D16 VDD	D17 VDD	D18 GND	D19 VDD	D20 GND	D21 GND	D22 VDD	D23 VDD	D24 FCNTRL_3	D25 FCNTRL_0	D26 LED3_3n
									E23 FCNTRL_2	E24 RESETn	E25 LED2_3n	E26 LED3_2n
									F23 TAP	F24 LED1_3n	F25 LED2_2n	F26 LED3_1n
									G23 LED0_3n	G24 LED1_2n	G25 LED2_1n	G26 LED1_1n
									H23 LED0_2n	H24 VDD	H25 LED0_1n	H26 LED1_0n
									J23 VDD	J24 LED3_0n	J25 LED0_0n	J26 A7
									K23 LED2_0n	K24 PHYCLK	K25 A6	K26 A4
									L23 VDD	L24 A5	L25 A3	L26 A1
									M23 A2	M24 A0	M25 CDST0	M26 VDD
									N23 CDST1	N24 CDST2	N25 CDST3	N26 GND
									P23 CDST6	P24 CDST5	P25 CDST4	P26 GND
									R23 VDD	R24 CDST9	R25 CDST8	R26 CDST7
									T23 CDST15	T24 CDST13	T25 CDST11	T26 CDST10
									U23 WRn	U24 INTn	U25 CDST14	U26 CDST12
									V23 VDD	V24 RDn	V25 ENREGIOn	V26 READY
									W23 RXRDY_2	W24 REGPS1	W25 BUSSIZE	W26 VDD
									Y23 TXRDY_3	Y24 RXRDY_1	Y25 REGPS0	Y26 REGPS2
									AA23 RXABORT_3	AA24 TXRDY_2	AA25 VDD	AA26 RXRDY_3
									AB23 RXDC_3	AB24 RXABORT_2	AB25 TXRDY_1	AB26 RXRDY_0
AC14 RXTXDATA 6	AC15 RXTXDATA 10	AC16 RXTXDATA 15	AC17 RXTXDATA 19	AC18 VDD	AC19 RXTXDATA 26	AC20 RXTXDATA 29	AC21 TXRET_1	AC22 RXDC_0	AC23 VDD	AC24 RXDC_2	AC25 RXABORT_1	AC26 TXRDY_0
AD14 RXTXDATA 5	AD15 RXTXDATA 8	AD16 RXTXDATA 13	AD17 VDD	AD18 RXTXDATA 20	AD19 RXTXDATA 23	AD20 RXTXDATA 27	AD21 RXTXDATA 30	AD22 TXRET_2	AD23 RXDC_1	AD24 VDD	AD25 GND	AD26 RXABORT_0
AE14 RXTXDATA 4	AE15 VDD	AE16 RXTXDATA 11	AE17 RXTXDATA 14	AE18 RXTXDATA 17	AE19 RXTXDATA 21	AE20 RXTXDATA 24	AE21 VDD	AE22 RXTXDATA 31	AE23 TXRET_3	AE24 GND	AE25 VDD	AE26 GND
AF14 GND	AF15 RXTXDATA 7	AF16 RXTXDATA 9	AF17 RXTXDATA 12	AF18 RXTXDATA 16	AF19 RXTXDATA 18	AF20 RXTXDATA 22	AF21 RXTXDATA 25	AF22 RXTXDATA 28	AF23 TXRET_0	AF24 VDD	AF25 GND	AF26 GND

Packaging

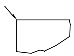
Figure 5 is a drawing of the package used for the 88800.

Figure 5 88800 Package Drawing

REV.	DESCRIPTION	DATE	CHECKED	ORIGINATED BY
00	INTIAL RELEASE PER DCN #C01435	12/18/96	T.Y.L.	M.E.
01	CHANGES PER DCN #C02060	07/31/97	Y.M.K.	R.L.S.
02	CHANGES PER DCN #C02112	08/19/97	Y.M.K.	M.W.
03	DIM CHANGES PER DCN C03992	07/28/98	DPARK	KMN

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.
2. DIMENSION "d" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM $\boxed{C}$.
3. PRIMARY DATUM $\boxed{C}$ AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. PIN A1 I.D. MARK.
5. SHAPE AT CORNER.



SINGLE FORM

6. NUMBER OF ROWS IN FROM EDGE TO CENTER.
7. SEATING PLANE CLEARANCE: MINIMUM HEIGHT OF ENCAPSULANT ABOVE SEATING PLANE.
8. "S" IS MEASURED WITH RESPECT TO $\boxed{A}$ AND $\boxed{B}$ AND DEFINES THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, THE VALUE IS "S"=e/2.

AMKOR/ANAM CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

DECIMAL	ANGULAR
X.X ±0.10	±1°
X.XX ±0.05	
X.XXX ±0.03	

MATERIAL: SEE NOTES

FINISH: SEE NOTES

DO NOT SCALE DRAWING

PROJECTION

APPROVALS		DATE
DRAWN	M. EMMETTE	11/08/96
CHECKED	B. ADKINS	11/20/96
ENG'R	P. MESCHER	11/25/96
RELEASED	T.Y. LLORENTE	12/18/96

Anam Semiconductor, Inc. Sungdong-Ku, Seoul, Korea

Amkor Technology, Inc. Chandler, Arizona, USA

amkor anam

TITLE: PACKAGE OUTLINE – SBGA, 35.0mm X 35.0mm, 2 LAYER, 1.27mm PITCH, LAMINATE PACKAGE, AAWW

SIZE	SID NUMBER	DWG. NUMBER	REV
B	N/A	71868	03

STRIP DWG. NUMBER/REV	CUST. CODE	SCALE	SHEET
N/A	N/A	SCALE: NONE	SHEET 1 OF 3

Figure 5 88800 Package Drawing (cont.)

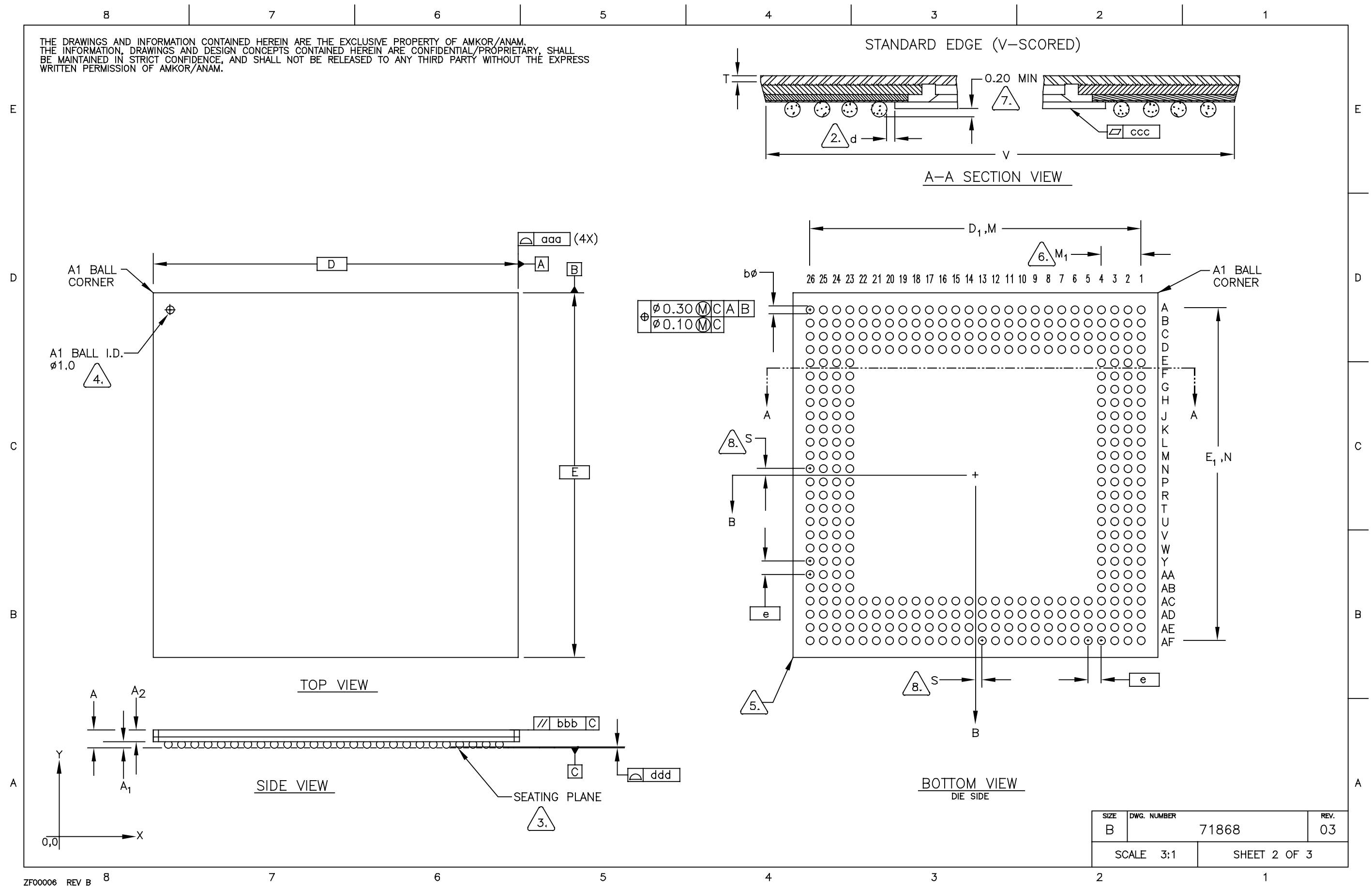
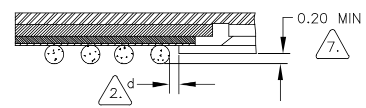


Figure 5 88800 Package Drawing (cont.)

BODY SIZE	35.0mm X 35.0mm PACKAGE			BODY SIZE
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	——	——	1.70	OVERALL THICKNESS
A1	0.50	0.60	0.70	BALL HEIGHT
A2	0.80	0.91	1.00	BODY THICKNESS
D	——	35.00	——	BODY SIZE
D1	31.65	31.75	31.85	BALL FOOTPRINT
E	——	35.00	——	BODY SIZE
E1	31.65	31.75	31.85	BALL FOOTPRINT
M,N	26 x 26			BALL MATRIX
M1 6	2–4			NUMBER OF ROWS DEEP
b	0.60	0.75	0.90	BALL DIAMETER
d	0.50			MIN DISTANCE ENCAP TO BALLS
e	1.27			BALL PITCH
aaa	——	——	0.20	PACKAGE BODY PROFILE
bbb	——	——	0.25	PARALLEL
ccc	——	——	0.20	ENCAP FLATNESS OVER DIE
ddd	——	——	0.20	COPLANARITY
S	——	0.635	——	SOLDER BALL PLACEMENT
T	0.050	0.125	0.175	V–SCORE WEB THICKNESS
V	34.20	——	34.90	V–SCORE BOTTOM SIZE

STANDARD BODY SIZE DIMENSION TABLE

OPTIONAL EDGE (ROUTED)



B–B SECTION VIEW

SIZE	DWG. NUMBER	REV.
B	71868	03
SCALE NONE	SHEET 3 OF 3	

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