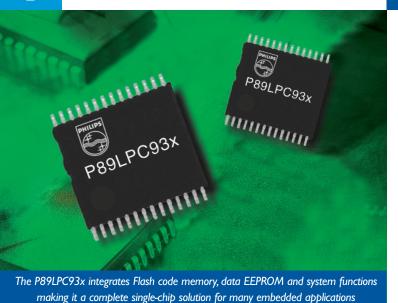
Philips 89LPC93x

8 KB Flash with 512 Byte Data EEPROM and 768 Byte SRAM



Description

The LPC900 family is based on a high performance 80C51 core that executes most instructions in two clock cycles, six times the rate of standard 80C51 devices. Many system level functions such as on-chip RC-oscillator, brown-out detect and separate watch dog oscillator have been incorporated into the LPC900 family in order to reduce component count, board space, and system cost.

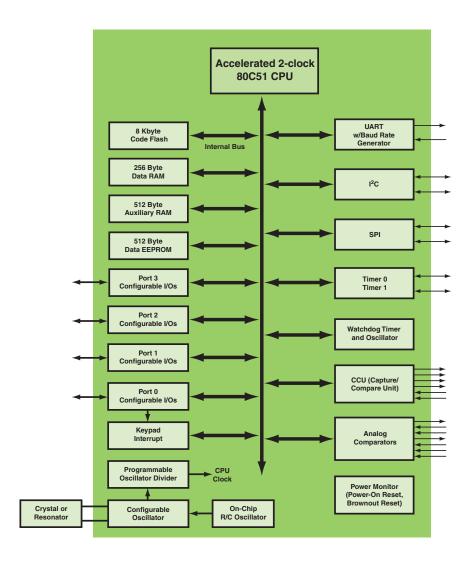
The P89LPC93x series integrates Flash program memory, data EEPROM memory and SRAM along with a variety of communications ports and system supervisory functions all in a small 28-pin package. The P89LPC93x series is designed for applications that demand high performance and high integration together with low voltage, low EMI and low cost.

Features

- High performance 2-clock 80C51 CPU providing 6 times the performance of the standard 80C51—most instructions execute in 167 ns at 12 MHz
- High Performance at reduced clock frequency results in both power saving and reduced EMI
- 2.4 V to 3.6 V V_{DD} operating range with 5 V tolerant I/O pins
- 8 Kbyte Flash code memory with 64-byte sectors and 2 ms block write/erase cycle
- 512 Byte data EEPROM memory allows device serialization, parameter storage etc.
- · 256 Byte RAM data memory
- 512 Byte auxiliary on-chip RAM
- Two 16-bit counter/timers with I/O port toggle and 8-bit PWM functions
- Real time clock/system timer
- 16-bit Capture/Compare Unit (CCU) with 32x PLL providing input capture, output compare and PWM
- Two analog comparators with selectable inputs and reference source
- Enhanced UART with framing error detection, automatic address detection
- 400 Kbit/s I²C communication port
- 3 Mbit/s SPI communication port
- · Eight keyboard interrupt inputs
- Two additional external interrupt inputs
- · Four interrupt priority levels
- Available in 28-pin TSSOP package



P89LPC93x Block Diagram



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