82C403/403A

CRT Clock Synthesizer

Data Sheet

October 1991

CHIPS®

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Title: CRT Clock Synthesizer
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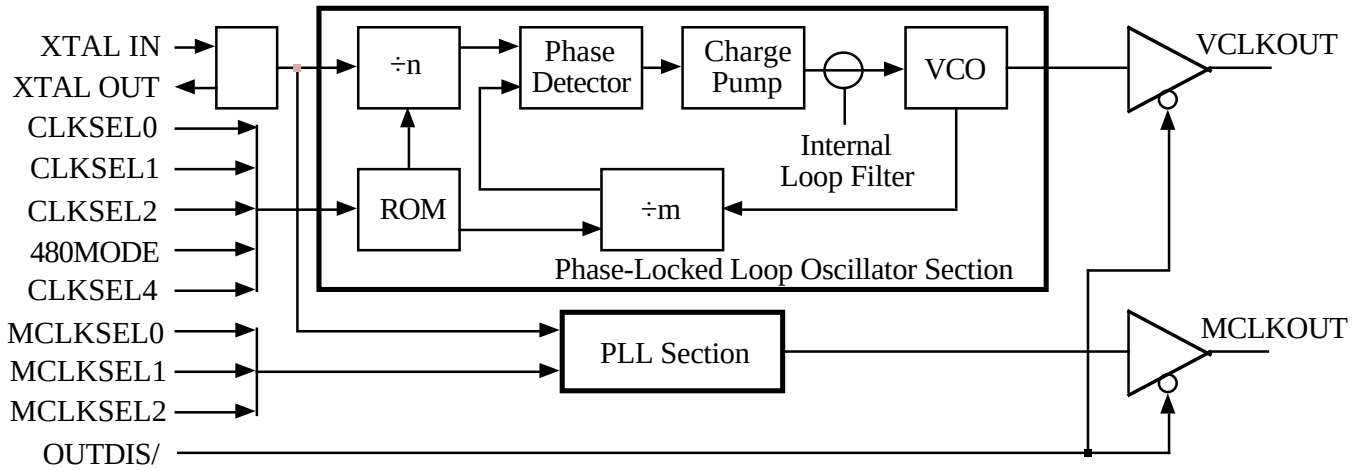
82C403/403A
CRT Clock Synthesizer

- 2 Independent Clock Outputs
- Supports all 82C453 and 82C480 Frequency Requirements
- Frequencies Supported up to 108 MHz
- Low Power Consumption
- Reduced Board Space Requirements
- 3-State Output Control Disables Outputs for Test Purposes
- 5-Volt Operation
- Replaces up to Nine TTL Oscillators
- Internal Loop Filter Requires no External Components
- Frequency Selection Scheme Compatible with Chips BIOS and Extended Mode Drivers
- 16-pin DIP or SOIC Package
- Reference Frequency uses Standard 14.31818 MHz Crystal
- Low-Power, High Speed 1.25µ CMOS Technology



82C403/403A Functional Block Diagram

Revision History

Revision	Date	By	Comment
0.1	7/90	DR	Draft Copy
0.1	7/90	DR	Review Copy before formatting
0.2	8/90	DR	Added Table of Contents and List of Figures
0.3	1/91	DR	Pin Descriptions - added vertical lines to define Type and Active columns. DC Characteristics - changed formula under Notes column 2nd and 3rd places.
0.4	5/91	DR/ST	Added 403A frequency table, 40x Clock Chip Layout, and Pin List.

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Introduction

In applications requiring two or more TTL oscillators, board space, power consumption, and cost may be reduced by using a clock synthesis chip.

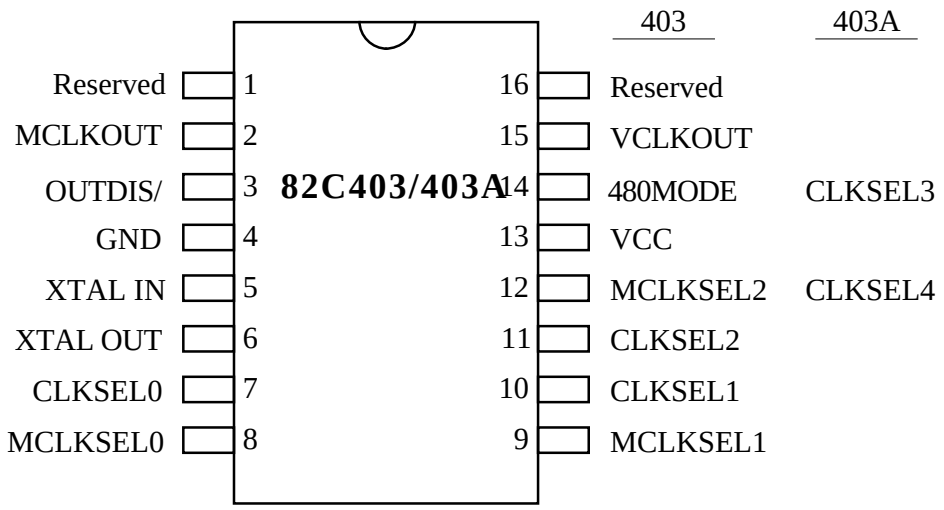
The 82C403 and 82C403A clock synthesizer chips are designed specifically for interfacing to the 82C453 and 82C480/B484 CRT Controllers. The 82C403/403A feature two independent clock outputs, impedance matched for direct connection to the 82C453 and 82C480/B484. This reduces the over/undershoot problems which are encountered when designing with fast TTL oscillators and eliminates the resistors required to fix them. This also reduces high frequency noise within the circuit which should facilitate meeting FCC requirements.

In high-resolution 82C480 applications, the 82C403/403A replaces up to nine TTL oscillators. The 82C403/403A replaces all six TTL oscillators required for complete 82C453 resolution support. Since only two high frequency clocks are running at a time, this reduces the noise generated by the board even further.

Note: The 82403A is a second generation version of the 82C403 clock synthesizer. It provides more flexibility for video frequencies when using the 82C453 Ultra VGA. In particular, the 82C403A provides a 50.350MHz selection which is required for a high refresh 800x600 VESA standard mode. The 82C403A also supports 32 video frequency selects whereas the 82C403 only supported 16. The 82C403A however only supports 4 memory clock frequencies as compared to 8 in the 82C403.

For many customers, both the 82C403 and the 82C403A will satisfy their requirements.

82C403/403A Pinouts



82C403/403A Pin List

Pin Name	Pin #
CLKSEL0	7
CLKSEL1	10
CLKSEL2	11
GND	4
MCLKOUT	2
MCLKSEL0	8

Pin Name	Pin #
MCLKSEL1	9
MCLKSEL2/CLKSEL4	12
OUTDIS/	3
Reserved	1
Reserved	16

Pin Name	Pin #
VCC	13
VCLKOUT	15
XTAL IN	5
XTAL OUT	6
480MODE/CLKSEL3	14

82C403/403A PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
5	XTAL IN	In	Both	Reference frequency input (if using an external oscillator) or 14.31818 MHz crystal input.
6	XTAL OUT	Out	Both	Optional Oscillator output to a 14.31818 MHz (Series Resonant) crystal. All passive components required for series resonant operation are implemented internally to the 82C403/403A.
7 10 11 14 12	CLKSEL0 CLKSEL1 CLKSEL2 480MODE/CLKSEL3 MCLKSEL2/CLKSEL4	In In In In In	Both Both Both Both Both	The CLKSEL inputs are connected directly to the CLKSEL outputs of the 82C480/82B484/82C453. They are used to decode the requested output frequency. The CLKSEL4 input exists only in the 82C403A. In the 82C403, 480MODE determines the CRT controller mode in which the 82C403 is to operate: 0: 82C453 1: 82C480
12 9 8	MCLKSEL2/CLKSEL4 MCLKSEL1 MCLKSEL0	In In In	Both Both Both	The MCLKSEL inputs determine the MCLKOUT frequency generated. The MCLKSEL2 input exists only in the 82C403.
3	OUTDIS/	In	Low	Output Disable. This disables both of the clock outputs and puts those pins into a high-impedance mode. This is useful for automated board test or for multiplexing additional clocks into the CRT controller. This pin has an internal pull-up and may be left unconnected if not used. 0: Clock outputs disabled (3-state) 1: Clock outputs enabled
15	VCLKOUT	Out	Both	Video Clock Output. This should be connected directly to the CLKIN input on the 82C453 or 82B484. The output impedance has been matched for a standard layout and the characteristic input impedance of an 82C453 or 82B484.

82C403/403A PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
2	MCLKOUT	Out	Both	Memory Clock Output. This should be connected directly to the MCLK input on the 82C453 or 82C480 CRT controller. The output impedance has been matched for a standard layout and the characteristic input impedance of an 82C453 and 82C480 CRT controller.
1 16	RESERVED RESERVED	NC NC		Reserved pins (do not connect).
13	VCC	Power		+5V Power Supply.
4	GND	Ground		Ground Pin.

82C403/403A Functional Description

Clock Oscillator Selection

The output frequency values of VCLKOUT are selected by the 480MODE, CLKSEL4:0 and OUTDIS/ pins as shown on the following pages.

The output frequency values for MCLKOUT are selected by MCLKSEL2:0:

MCLKSEL2	MCLKSEL1	MCLKSEL0	MCLKOUT (MHz)
0	0	0	32.5
0	0	1	36.0
0	1	0	40.0
0	1	1	45.0
1	0	0	32.5
1	0	1	50.0
1	1	0	40.0
1	1	1	45.0

82C403 MCLKSEL

MCLKSEL1	MCLKSEL0	MCLKOUT (MHz)
0	0	32.5
0	1	50.0
1	0	40.0
1	1	45.0

82C403A MCLKSEL

At any time during operation, the selection lines can be changed to choose a different frequency. The internal phase-lock loop will immediately begin to seek the newly selected frequency. During the transition period, the clock output will not glitch. The intermediate frequency will not exceed the higher of the two transition frequencies.

Tri-State Output Operation

The OUTDIS/ signal, when pulled low, will 3-state both of the clock output lines. This supports "wired-or" connections between external clock lines (e.g. the Feature Connector external clock) and allows for procedures such as automated testing, where the clock must be disabled. The OUTDIS/ signal contains an internal pull-up and may be left unconnected if it is not required.

Optional External Crystal

Normal operation requires a nominal 14.31818 MHz reference signal which is standard in all PC systems. If the 82C403 is to be used in a motherboard application then it can be used to generate the 14.31818 MHz clock (XTAL OUT) required for the system. If the 14.31818 MHz clock is generated elsewhere on the motherboard, it may be connected directly to the 82C403/403A (XTAL IN). In motherboard applications, control over the quality of the reference clock is guaranteed by the layout and design. When

OUTDIS/	480MODE	CLKSEL2	CLKSEL1	CLKSEL0	VCLKOUT (MHz)
0	X	X	X	X	HIGH-Z
1	0	0	0	0	25.175
1	0	0	0	1	28.322
1	0	0	1	0	36.0
1	0	0	1	1	44.9
1	0	1	0	0	31.2
1	0	1	0	1	28.322
1	0	1	1	0	40.0
1	0	1	1	1	65.0
1	1	0	0	0	25.175
1	1	0	0	1	44.9
1	1	0	1	0	65.0
1	1	0	1	1	80.0
1	1	1	0	0	31.2
1	1	1	0	1	40.0
1	1	1	1	0	75.0
1	1	1	1	1	108.0

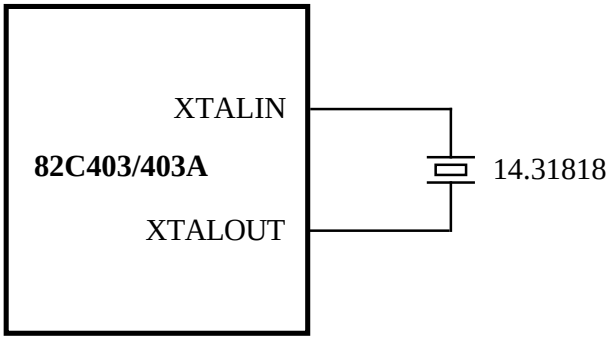
82C403 VCLKOUT Frequency Select

OUTDIS/	CLKSEL4	CLKSEL3	CLKSEL2	CLKSEL1	CLKSEL0	VCLKOUT (MHz)
0	0	X	X	X	X	HIGH-Z
1	0	0	0	0	0	25.175
1	0	0	0	0	1	28.322
1	0	0	0	1	0	31.2
1	0	0	0	1	1	44.9
1	0	0	1	0	0	50.35
1	0	0	1	0	1	75.0
1	0	0	1	1	0	40.0
1	0	0	1	1	1	65.0
1	0	1	0	0	0	25.175
1	0	1	0	0	1	28.322
1	0	1	0	1	0	36.0
1	0	1	0	1	1	44.9
1	0	1	1	0	0	50.35
1	0	1	1	0	1	75.0
1	0	1	1	1	0	40.0
1	0	1	1	1	1	65.0
1	1	0	0	0	0	25.175
1	1	0	0	0	1	28.322
1	1	0	0	1	0	36.0
1	1	0	0	1	1	44.9
1	1	0	1	0	0	31.2
1	1	0	1	0	1	28.322
1	1	0	1	1	0	40.0
1	1	0	1	1	1	65.0
1	1	1	0	0	0	25.175
1	1	1	0	0	1	44.9
1	1	1	0	1	0	65.0
1	1	1	0	1	1	80.0
1	1	1	1	0	0	31.2
1	1	1	1	0	1	40.0
1	1	1	1	1	0	75.0
1	1	1	1	1	1	108.0

82C403A VCLKOUT Frequency Select

placing the 82C403/403A on a daughter card the stability of the system bus 14.31818 MHz reference frequency is not assured. In most modern PC designs, this signal is stable enough for use with the 82C403/403A. There will however always be exceptions.

For those cases where a stable noise-free system clock cannot be guaranteed, the 82C403/403A includes a built-in oscillator which can serve as the reference source. If this mode is desired, an external series-resonant 14.31818 MHz crystal should be connected between the XTAL1 and XTAL2 pins. No additional resistors or capacitors are required. All components necessary to achieve resonance are fabricated internal to the 82C403/403A.



82C403/403A Crystal Interface

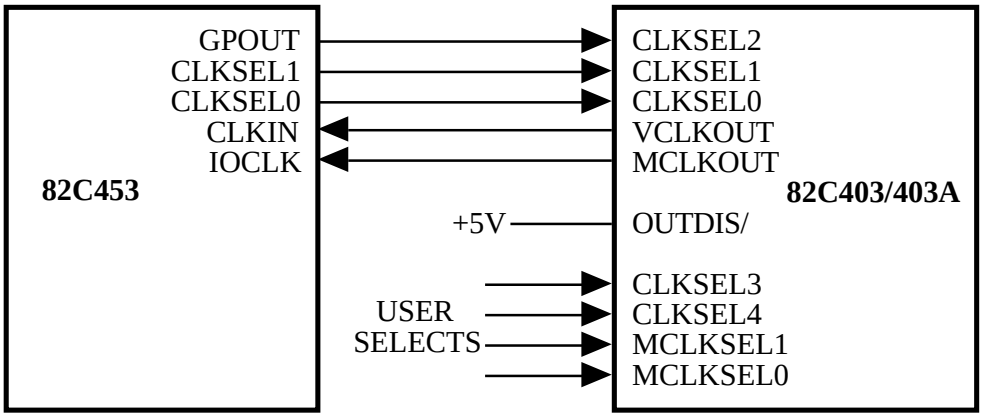
No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the 82C403/403A. The phase-lock loops are fabricated internally and require no external capacitors.

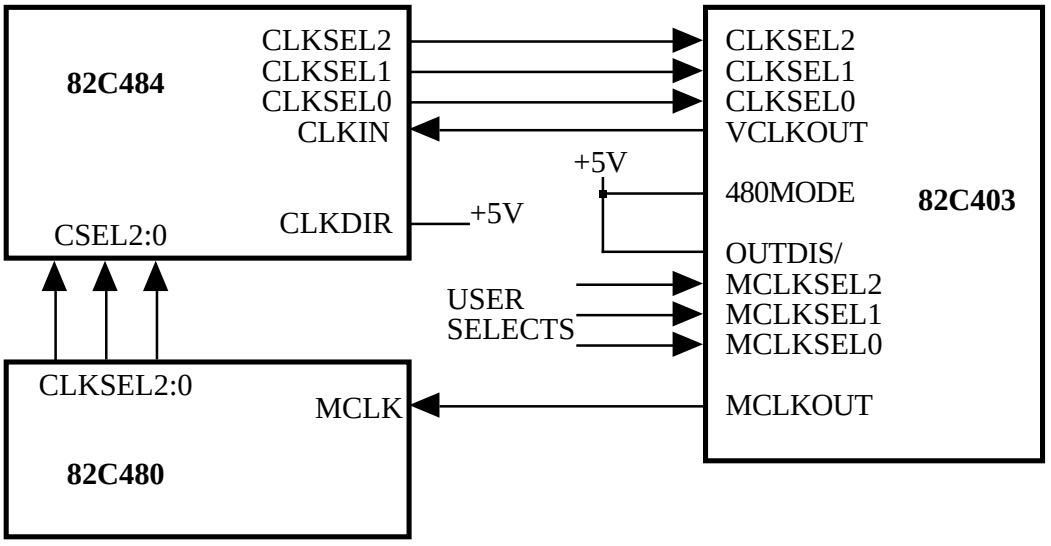
Clock Synthesizer Description

Both of the oscillator blocks are classic phase-locked loops connected as shown in the block diagram on the front page. The external input frequency (XTAL IN) is 14.31818 Mhz and goes into a "divided-by-n" block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is essentially a feedback system which attempts to get two signals (the divided reference signal and the divided variable 'synthesized' signal) to arrive in phase. The system attempts to achieve zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower depending on what is required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately 'lock-on' to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal 'loop filter' provides stability and damping.



82C403/403A Interface to an



82C403 Interface to an 82C480

Output Frequency Accuracy

The accuracy of the output frequency depends upon the target output frequency. The tables within this document contain target frequencies which are different than the actual frequencies produced by the clock synthesizer. The output frequency of the 82C403/A clock synthesizer is an integral fraction of the input (reference) frequency:

$$f_{Out} = \frac{2 f_{Ref} m}{n} \quad m,n \text{ integer}$$

Only certain output frequencies are possible for a particular reference input. The 82C403/A always produces an output frequency within 1% of the target. This is more than sufficient to meet standard display requirements.

Minimized Parasitic Problems

All of the 82C40x family of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins isolated as much as possible. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used internally. This eliminates the need to provide separate analog and digital VCC and GND to the chip.

The parts use center pins to deliver power and ground to the die instead of the more conventional corner pins. The package leadframes are optimized to have especially 'fat' power and ground leads. This gives the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce and output crosstalk.

Stability and "Bit-Jitter"

The long-term frequency stability of the 82C40x phase-locked loop frequency synthesis components are good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices are affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The 82C40x frequency synthesis parts have been designed with an emphasis on reduction of "bit-jitter". The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize this "bit-jitter". The 82C40x families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

Temperature and Process Sensitivity

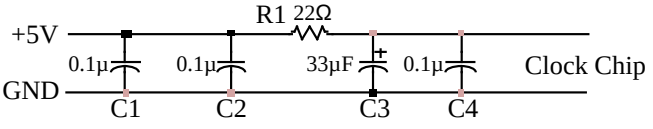
Because of its feedback circuitry, the 82C403/A is inherently stable over temperature and manufacturing process variations. An advantage of incorporating the loop filter internal to the chip is that now the loop filter will track the same process variations as does the VCO. This means there are no manufacturing "tweaks" required to filter components as is commonly required for external "de-coupled" filters.

82C40x Clock Chip Layout

Clock synthesis chips are extremely sensitive to voltage supply noise. This is due in part to their use of VCO's to lock onto the desired frequency. The 82C40x family of clock chips all currently contain multiple Phase Lock Loops (PLLs). Each Phase Lock Loop employs a Voltage Controlled Oscillator (VCO). These VCO's have a very high df/dv so small changes in supply voltage can cause large shifts in output frequency. The stability of the VCO's in graphics applications is critical in order to avoid frequency fluctuations. Temporary phase shifts are seen on the display as jitter. To minimize supply line ripple, CHIPS has developed the following layout suggestions for filtering the power supply to the 82C40x clock chips.

When using the 82C403/A, a full power and ground plane layout should be employed both under and around the IC package.

For two layer boards, bring a separate V_{CC} trace from the bus connector up to the clock chip. This is also desirable but not absolutely necessary for multi-layer layouts. Filter this trace at its source with a 0.1µF capacitor (C1) and again adjacent to the 22Ω resistor (C2) as shown. Multi layer boards tapping an inner power plane may omit the first 0.1µF capacitor (C1) but should include the second (C2). All designs must include R1, C3, and C4.



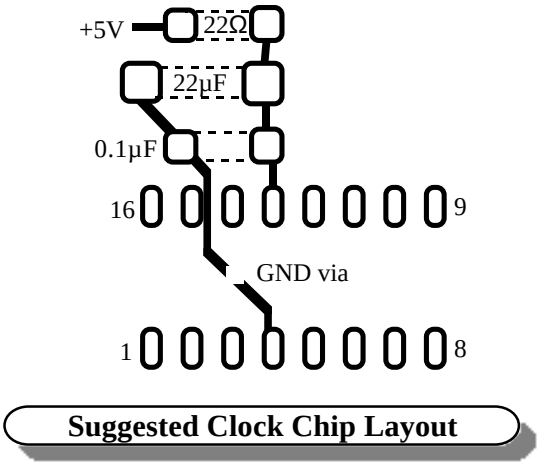
Clock Chip Power Supply Isolation

The 22Ω resistor acts to filter small fluctuations but also drops the supply voltage to the 82C40x chip by approximately 500mV. This value may be increased to as much as 33Ω in very noisy situations with careful attention given to the supply voltage level at the clock chip. If the supply (V_{CC}) drops below 4.25V at the clock chip then the phase lock loop may lose lock. The 82C40x family of clock chips have been tuned to operate with a 22Ω resistor in series with the V_{CC} input.

The isolated supply should be filtered by a bulk tantalum 22µF-47µF capacitor and immediately adjacent to the clock chip by another 0.1µF cap. Both capacitors should be placed within 0.15" of the power pin.It is extremely important that the power supply trace to the clock chip pass from the 22Ω resistor, connecting the bulk capacitor, then connecting the 0.1µF capacitor before reaching the power pin on the clock chip. There will be high frequency noise on the isolated supply trace between the bulk capacitor and the 0.1µF. It is important that the clock chip power pin not see any of this noise so do not route the trace from the bulk cap to the 0.1µF via the power pin. The 0.1µF cap will filter this high frequency noise which may otherwise cause visible jitter on the display. For through-hole designs, use ceramic disk capacitors rather than axial leaded capacitors. Minimizing inductance between the V_{CC} and GND pins on the clock chip is very important. For two layer designs, a GND plane should be placed under the 82C40x and its immediate bypass components.

The designer should also avoid routing the clock output traces of the 82C403/403A in close parallel proximity for any great distance. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs and the duty cycle. The 82C403/A has been optimized to have its clock output pins connected directly to the VGA controller.

When designing with this device, the best rule to follow is to locate the 82C403/403A as close to the 82C45x VGA controller as is possible. Do not route high frequency signals such as DRAM control lines near to the 82C403/403A or its clock outputs. A suggested layout is shown below for the isolated section of the supply.



Suggested Clock Chip Layout

82C403/403A Electrical Specifications

82C403/403A ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	175	mW
V_{CC}	Supply Voltage	-0.5	–	7.0	V
V_I	Input Voltage	-0.5	–	V_{CC}+0.5	V
T_{SOL}	Maximum Soldering Temperature (10 sec.)	–	–	260	°C
T_{OP}	Operating Temperature (Ambient)	-25	–	85	°C
T_{STG}	Storage Temperature	-40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C403/403A NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Ambient Temperature	0	–	55	°C

82C403/403A DC CHARACTERISTICS

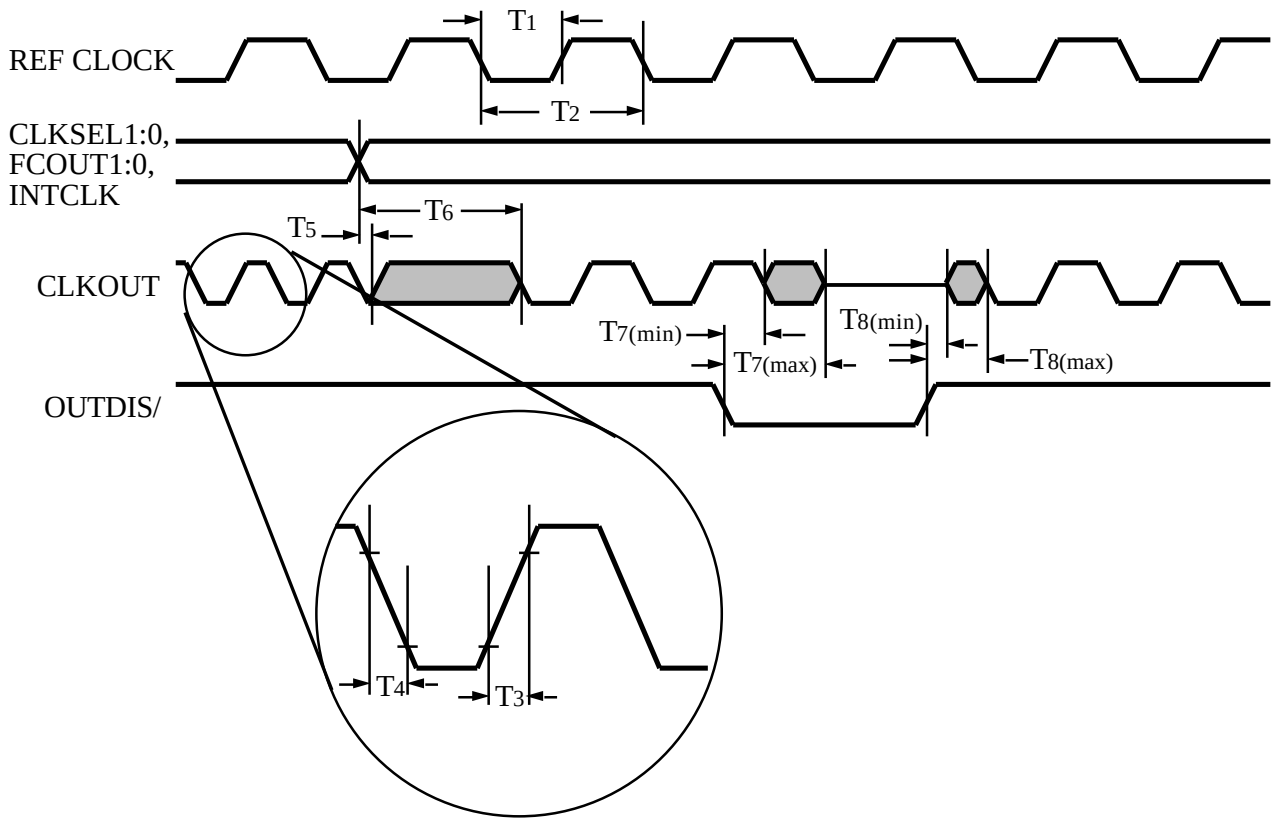
(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	@ 0°C	–	35	mA
I_{IL}	Input Low Leakage Current	V_I = 0.4 v	–	-500	µA
I_{IH}	Input High Current	V_I = 4.6 v	–	2.5	µA
I_{OZ}	Output Leakage Current	High Impedance	–	10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.5	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	2.8	–	V
C_{IN}	Input Capacitance		–	10	pF
	Bit Jitter	(1σ)	–	±350	ps
	Bit Jitter	Absolute	–	500	ps

Electrical specifications contained herein are preliminary and subject to change without notice.

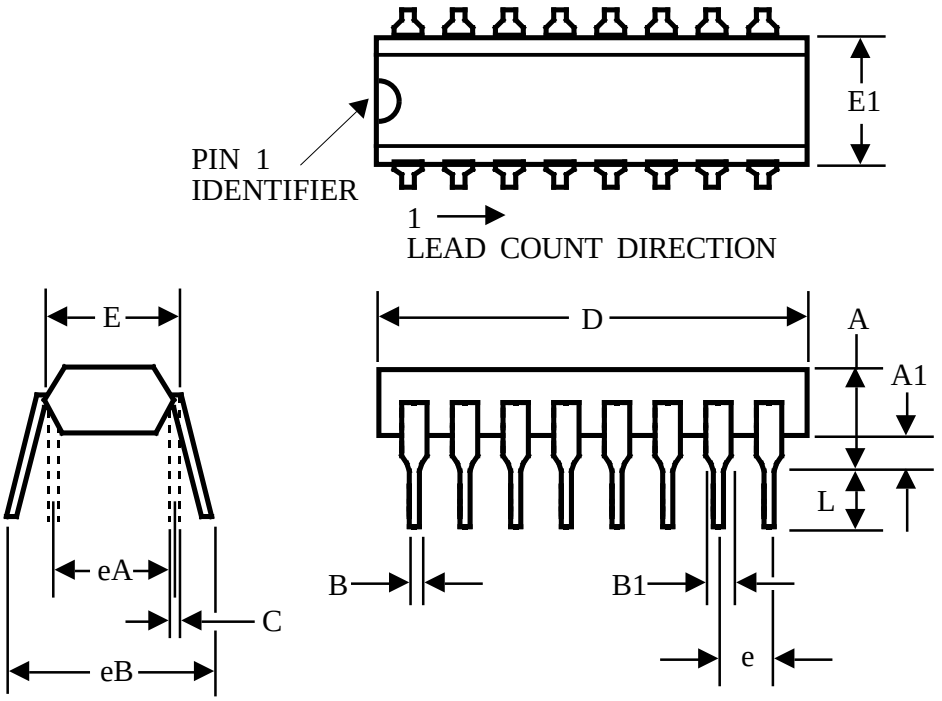
82C403/403A AC CHARACTERISTICS - Clock Timing

Symbol	Parameter	Notes	Min	Typ	Max	Units
f_{REF}	Reference Frequency	(± 10 ppm)	–	14.31818	–	MHz
T_2	Reference Clock Period		–	69.84128	–	ns
T_1/T_2	Reference Clock Duty Cycle		45	–	55	%
T_3	Output Clock Rise Time		–	–	3	ns
T_4	Output Clock Fall Time		–	–	3	ns
T_5	Frequency Select to Output Unstable		0	–	–	ns
T_6	Frequency Select to Output Stable		–	–	10	ms
T_7	OUTDIS/ Active to Output 3-state		–	–	12	ns
T_8	OUTDIS/ Inactive to Valid Clock Out		–	–	12	ns



82C403/403A Clock Timing

N82C403/403A Mechanical Specifications

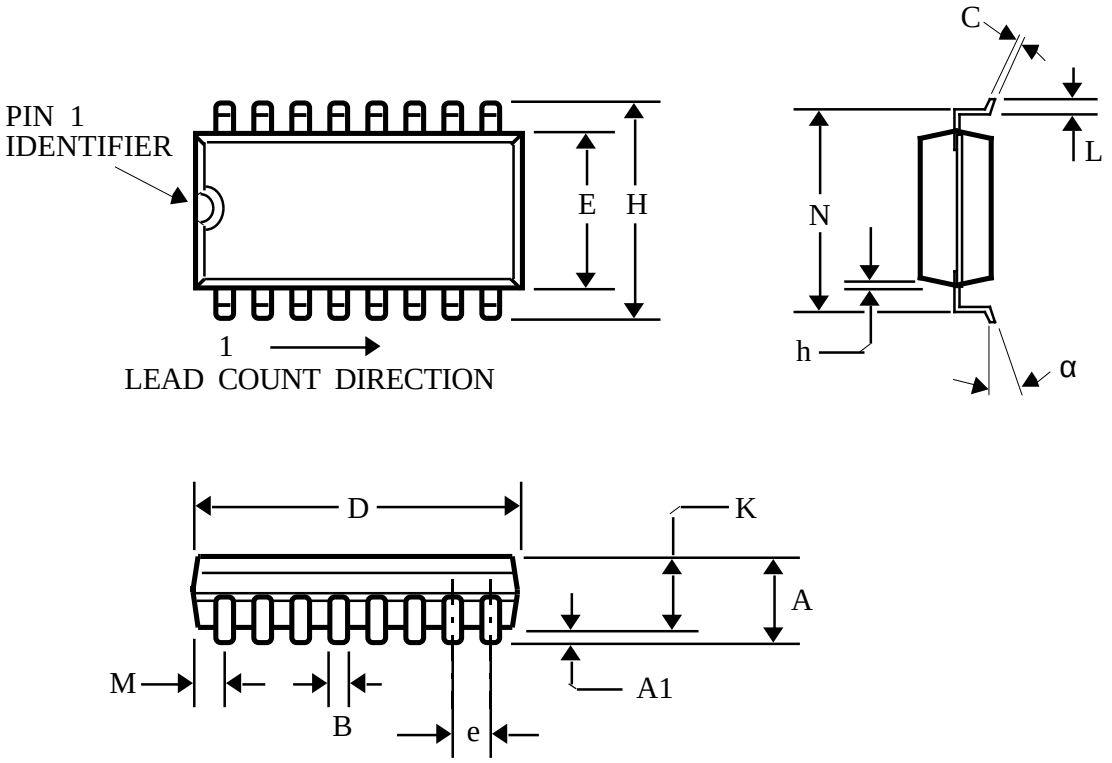


Plastic Dip Package (PDIP)

SYMBOL	LEAD COUNT = 16		
	MIN	TYP	MAX
A	0.195	–	0.200
A1	0.015	–	–
B	0.015	–	0.020
B1	0.050	–	0.070
C	0.008	–	0.012
D	0.745	–	0.790
E	0.290	–	0.310
E1	0.220	–	0.280
e	–	0.100	–
eA	0.290	–	–
eB	–	–	0.310
L	0.100	–	–

(Dimensions in Inches)

F82C403/403A Mechanical Specifications



Small Outline IC Package (SOIC)

SYMBOL	LEAD COUNT = 16 MIN	TYP	MAX
A	0.099	–	0.104
A1	0.004	–	0.009
B	0.014	–	0.019
C	0.009	0.010	0.013
D	0.405	–	0.410
E	0.294	–	0.299
e	–	0.050	–
H	0.402	–	0.419
h	–	0.025 x 45°	–
L	0.030	–	0.040
α	0 °	–	8 °
K	0.088	–	0.098
M	0.020	–	0.030
N	0.335	–	0.351

(Dimensions in Inches)