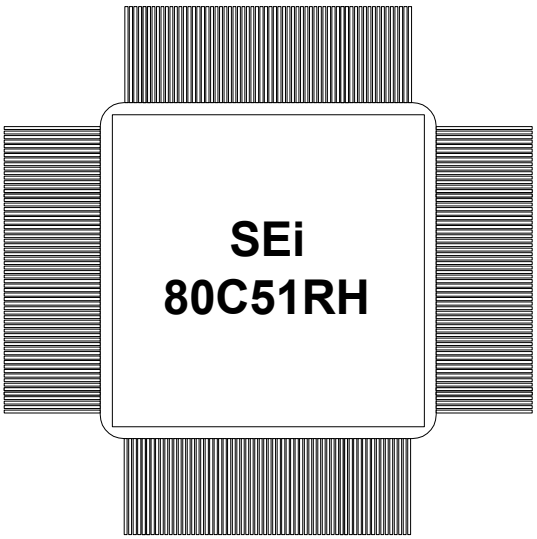
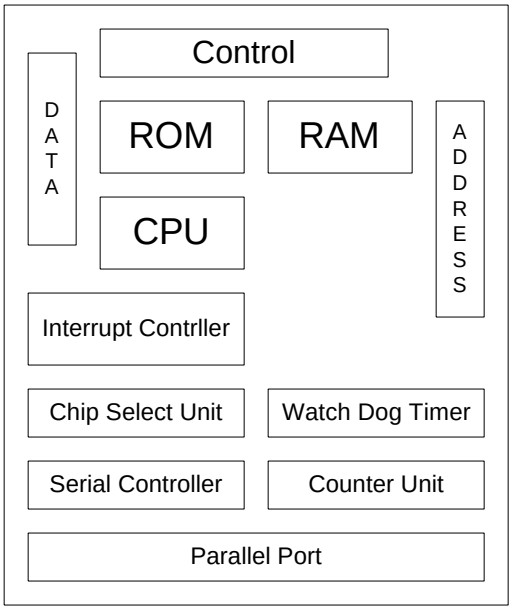
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

8-BIT MICROCONTROLLER
80C51RH





FEATURES:

- 128 bytes of on-chip data RAM
- Four 16-bit timer/counter
- 80 programmable I/O lines (ten 8-bit ports)
- 2 programmable full duplex serial channels
- Single +5 V power supply
- Military temperature range: -55 to 125 ^{o}C
- Radiation-hardened:
  - Total dose: 1 x 10^{7} rads (Si)
  - SEU: 1 x 10^{-8} (upsets/bit-day)
  - SEL: immune

DESCRIPTION:

Space Electronics' 80C51RH is an INTEL compatible single chip microcontroller and is fabricated using radiation-hardened SOI technology. The 80C51RH 8-bit microcontroller features a typical 10 MRads (Si) total dose tolerance (dependent upon orbit and mission duration) and is latchup immune.

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TABLE 1.

FUNCTION	DESCRIPTION
Core CPU	
Instruction Set	Full software compatible with INTEL 8051 (8-bit CPU)
Clock Frequency	12.5 MHz maximum
Internal ROM	3.5 Kbytes mask ROM
Internal Data RAM	128 bytes
Interrupt Circuit	2 Channel (external interrupt)
	3 Channel (internal interrupt for CPU)
Digital Interface Circuit Serial I/O Port	
Number of Channels	1 Channel (Core CPU)
	1 Channel (Using M8251 macro-based)
Digital Transmission	Full duplex
Transfer Rate	300-19200 bps (programmable)
Transfer Method	Asynchronous communications
Parallel I/O Port	
Number of I/O Ports	1 Port (Core CPU)
	9 Ports (3 x M8255 macro-based)
Number of I/O Bits	80 bit (8-bits x 10 ports)
I/O Setup	Programmable per 8-bit unit

TABLE 2.

FUNCTION	DESCRIPTION
Boot Loader/Debugger Programs [1]	
	Built-in test (register check, calculator check, memory check)
	Down load of a user program (conform to INTEL HEX file)
	Dump of external data memory
	Display and modify data of external data memory
	Display and modify data of internal data memory
	Dispaly and modify data of register
	Execute and interrupt a user program

1. Internal mask ROM has the boot loader/debugger programs which enable user program to be loaded through serial lines from external host computer and to be executed. The external host computer sends the command through serial lines to download the program.

TABLE 3.

FUNCTION	DESCRIPTION
Counter/Timer Circuit (CTC)	
Number of Channels	2 channel (core CPU)
	3 channel (using M8254 macro-based)
Number of Count bit	16-bit length
Setup of Clock Input	2 channel (core CPU) Programmable select external/internal input
	3 channel (M8254 macro-based) external input only
Supplement	One of 2 channel (core CPU) and one of 3 channel used for the baud rate generator

TABLE 4.

FUNCTION	DESCRIPTION
Watch-dog-timer Circuit (WDT)	
Time of WDT	11, 22, 44 , 87, 175, 350, 699, 1398 ms (at 12 MHz) clock) programmable
The output of WDT	The error signal of WDT to outside of RH8M51

TABLE 5.

FUNCTION	DESCRIPTION
Function of Extend Circuit [1]	
Signal of external interface bus	
Address Bus	16-bit
Data Bus	8-bit
Control Bus	Program memory read (PSEN*)
	Data memory read (RD*)
	Data memory write (WR*)
	Memory read (MEM_RD*)
	I/O request (IORQ*)
Signal of external memory select	2-bit (32 Kbyte per unit)
Signal of bank select	7-bit (32 Kbyte per unit)

1. This device has some select signals to extend I/O lines and memories outside of 80C51RH.

TABLE 6.

FUNCTION	DESCRIPTION
Bus Line of External ROM [1]	
Address bus	12-bit
Data bus	8-bit

1. The 80C51RH is able to have an external ROM without using internal mask ROM.

FIGURE 1. 80C51RH BLOCK DIAGRAM

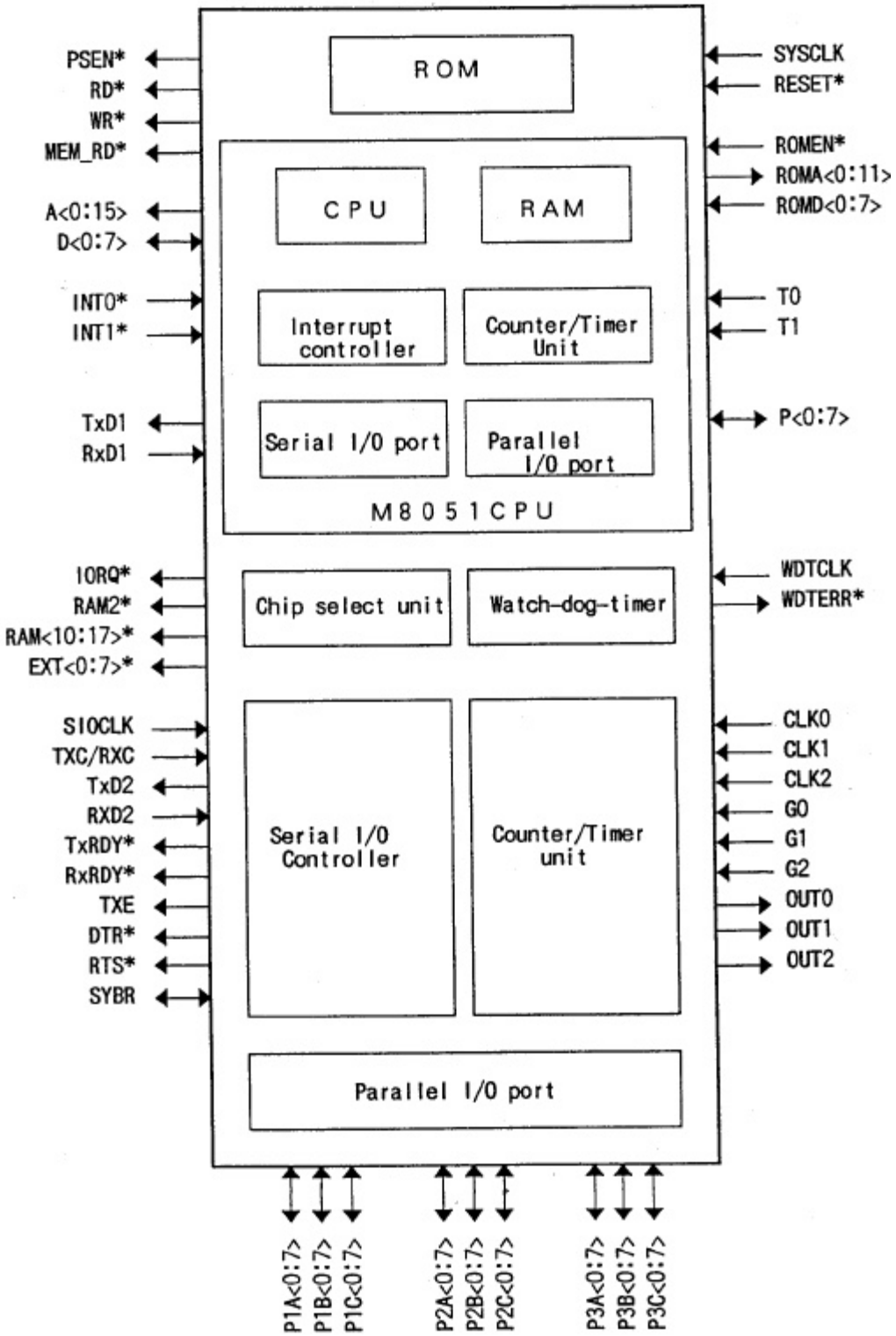

FIGURE 2. PIN CONNECTIONS