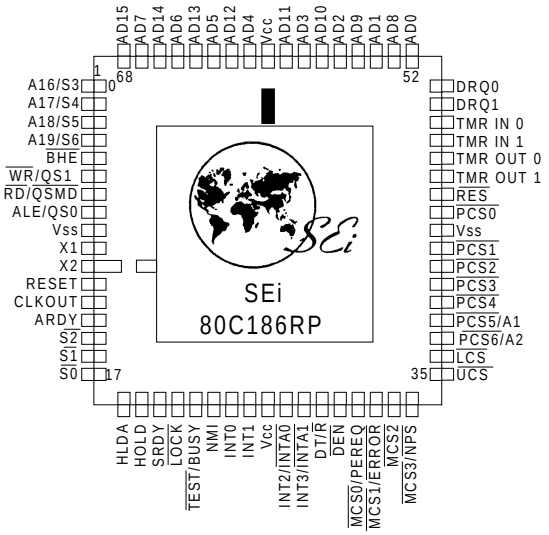
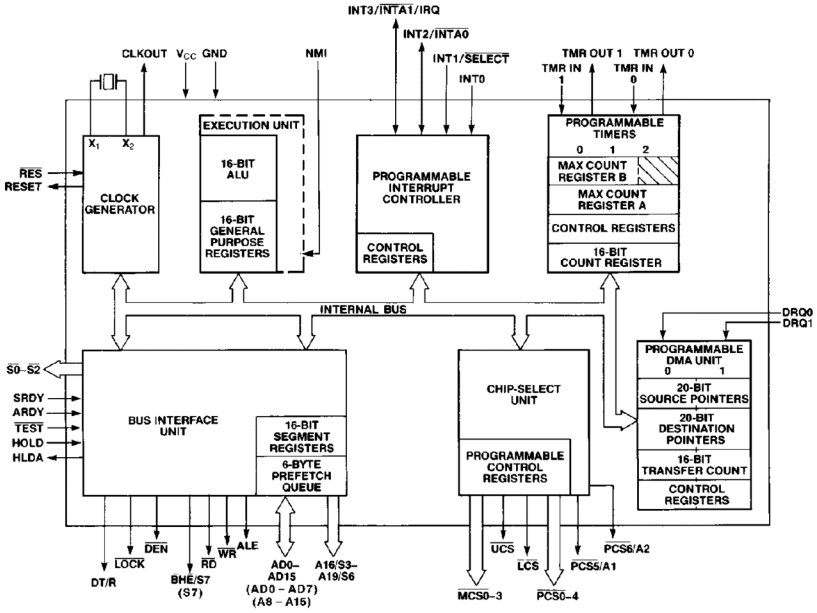
80C186RP

RADIATION HARDENED 16-BIT MICROPROCESSOR





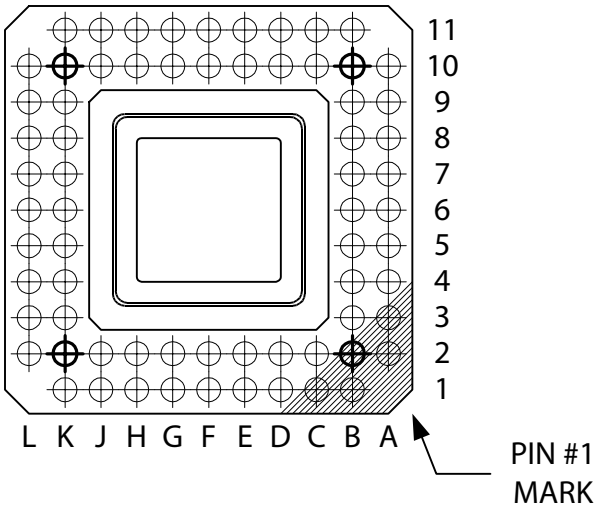
FEATURES:

- **16-bit microprocessor**
- **Total dose hardness typical 100 Krad (Si); dependent upon orbit**
- **Single event effect:**
  - **SEL_{TH}: 61 MeV/mg/cm²**
  - **SEU_{TH}: 9 MeV/mg/cm²**
- **Package:**
  - **-68 pin RAD-PAK® quad flat pack**
  - **-68 pin RAD-PAK® PGA**
- **DRAM refresh with control unit**
- **Power-save logic**
- **Clock generator**
- **2 independent DMA channels**
- **Programmable interrupt controller**
- **3 programmable 16-bit timers**
- **Programmable memory and peripheral chip select logic**
- **System-level testing support**
- **Local bus controller**
- **Available in 10MHz and 12.5MHz**
- **Direct addressing capability to 1Mbyte and 64 Kbyte I/O**
- **Complete system development support**

DESCRIPTION:

Space Electronics' 80C186RP (RP for RAD-PAK®) high integration 16-bit microprocessor features a typical 100krad(Si) total dose tolerance;dependent upon orbit. The 80C186RP has two major modes of operation:enhanced and compatible. The enhanced mode adds three new features to the system design - Dynamic RAM refresh, power-save control and an asynchronous numerics co-processor interface. The compatible mode allows 100% pin-for-pin compatibility with commercial 80C186. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. Capable of surviving in space environment, the 80C186RP is ideal for satellite, spacecraft, and space probe missions. It is available in with packaging and screening up to Class S.

PINS FACING UP



FUNCTION	PIN	WIREBOND PAD	DIE PAD
VCC	F1	1	43
AD4	E2	2	45
AD12	E1	3	46
AD5	D2	4	47
AD13	D1	5	48
AD6	C2	6	49
AD14	C1	7	50
AD7	B2	8	51
AD15	B1	9	52
A16/S3	A2	10	53
A17/S4	B3	11	54
A18/S5	A3	12	55
A19/S6	B4	13	56
$\overline{BHE}$	A4	14	57
$\overline{WR}$/QS1	B5	15	58
$\overline{RD}$/$\overline{QSMD}$	A5	16	59
ALE/QS0	B6	17	60
VSS	A6	18	61
X1	B7	19	62
X2	A7	20	63

FUNCTION	PIN	WIREBOND PAD	DIE PAD
RESET	B8	21	64
CLKOUT	A8	22	65
ARDY	B9	23	66
$\overline{S2}$	A9	24	67
$\overline{S1}$	B10	25	68
$\overline{S0}$	A10	26	69
HLDA	B11	27	1
HOLD	C10	28	2
SRDY	C11	29	3
$\overline{LOCK}$	D10	30	4
$\overline{TEST}$/BUSY	D11	31	5
NMI	E10	32	6
INT0	E11	33	7
INT1	F10	34	8
VCC	F11	35	9
INT2/$\overline{INTA0}$	G10	36	10
INT3/INTA1	G11	37	11
DT/$\overline{R}$	H10	38	12
$\overline{DEN}$	H11	39	13
$\overline{MCS0}$/PEREQ	J10	40	14

FUNCTION	PIN	WIREBOND PAD	DIE PAD
$\overline{MCS1}$/$\overline{ERROR}$	J11	41	15
$\overline{MCS2}$	K10	42	16
$\overline{MCS3}$/NPS	K11	43	17
$\overline{UCS}$	L10	44	28
$\overline{LCS}$	K9	45	19
$\overline{PCS6}$/A2	L9	46	20
$\overline{PCS5}$/A1	K8	47	21
$\overline{PCS4}$	L8	48	22
$\overline{PCS3}$	K7	49	23
$\overline{PCS2}$	L7	50	24
$\overline{PCS1}$	K6	51	25
VSS	L6	52	26
$\overline{PCS0}$	K5	53	27
$\overline{RES}$	L5	54	28
TMR OUT1	K4	55	29
TMR OUT0	L4	56	30
TMR IN 1	K3	57	31
TMR IN 0	L3	58	32
DRQ 1	K2	59	33
DRQ 0	L2	60	34

FUNCTION	PIN	WIREBOND PAD	DIE PAD
AD0	K1	61	35
AD8	J2	62	36
AD1	J1	63	37
AD9	H2	64	38
AD2	H1	65	39
AD10	G2	66	40
AD3	G1	67	41
AD11	F2	68	42

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80C186RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage On Any Pin with Respect to Ground		-1.0	+7.0	V
Operating Temperature Range	T_{OPR}	-55	+125	^{O}C
Storage Temperature Range	T_{STG}	-65	+150	^{O}C

80C186RP OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Digital Supply Voltage	V_{CC}	4.75	5.25	V
Temperature Range	T_A	-55	+125	^{O}C

80C186RP DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC}=5V ± 5%, T_A = -55 to +125°C, unless otherwise Specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Input Leakage Current	0.45V < V_{IN} < V_{cc}	I_{LI}	-10	+10	uA
Output Leakage Current	0.45V < V_{OUT} < V_{cc} 1/	I_{LO}	-10	+10	uA
Input Low Voltage		V_{IL}	-0.5	+0.8	V
Input High Voltage	All except X1 and RES\	V_{IH}	2.0	V_{CC} +0.5	V
Input High Voltage	RES\	V_{IH1}	3.0	V_{CC} +0.5	V
Input High Voltage	ARDY/SRDY	V_{IH2}	2.3	V_{CC} +0.5	V
Output Low Voltage	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)	V_{OL}		0.45	V
Output High Voltage	I_{OH} = -2.4 mA @ 2.4V 4/ I_{OH} = -200µA @ 0.8 V_{CC} 4/	V_{OH}	2.4 4.0	-- --	V
Power Supply Current	12.5 MHz 3/ 10 MHz 3/	I_{CC}		160 140	mA
Power Save Current	Typical @ 25°C, V_{CC} = 5.0V	I_{PS}	10 mA per MHz + 20		mA
Clock Output Low	I_{CLO} = 4.0 mA	V_{CLO}		0.6	V
Clock Output High	I_{CHO} = -500 µA	V_{CHO}	4.0		V
Clock Input Low Voltage(X1)		VCLI	-0.5	0.6	V
Clock Input High Voltage(X1)		VCHI	3.9	V_{CC} +1.0	V
Input Capacitance	@ 1MHz 2/	C_{IN}		10	pF
I/O Capacitance	@ 1MHz 2/	C_{IO}		20	pF

Note:

1/ Pins being floated during HOLD or by invoking the ONCE Mode.

2/ Guaranteed by design.

3/ Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.

4/ RD\/QSMD\, UCS\, MCS0\/PEREQ, MCSL\/ERROR\, and TEST\/BUSY pins have internal pull-up devices that are active at RESET. Excessive loading on these pins can cause the 80C186 to go into undesired modes of operation upon RESET.

80C186RP AC ELECTRICAL CHARACTERISTICS - TIMING REQUIREMENTS 1/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Data in Setup (A/D)		T_{DVCL}			
80C186RP-10				15	ns
80C186RP-12				15	
Data in Hold (A/D)		T_{CLDX}			
80C186RP-10			5		
80C186RP-12			5		ns
ARDY Resolution Transition Setup Time 2/		T_{ARYCH}			
80C186RP-10				15	ns
80C186RP-12				15	
Asynchronous Ready (ARDY) Setup Time		T_{ARYLCL}			
80C186RP-10			30		ns
80C186RP-12			30		
ARDY Active Hold Time		T_{CLARX}			
80C186RP-10				15	ns
80C186RP-12				15	
ARDY Inactive Hold Time		T_{ARYCHL}			
80C186RP-10				15	ns
80C186RP-12				15	
Synchronous Ready (SRDY) Transition Setup Time		T_{SRYCL}			
80C186RP-10				15	ns
80C186RP-12				15	
SARDY Transition Hold Time		T_{CLSRY}			
80C186RP-10				15	ns
80C186RP-12				15	
HOLD Setup		T_{HVCL}			
80C186RP-10			20		ns
80C186RP-12			20		
INTR, NMI, TEST, TMR IN Setup Time		T_{INVCH}			
80C186RP-10			20		ns
80C186RP-12			20		
DRQ0, DRQ1, Setup Time		T_{INVCL}			
80C186RP-10			20		ns
80C186RP-12			20		

80C186RP AC ELECTRICAL CHARACTERISTICS - MASTER INTERFACE TIMING RESPONSES 1/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Address Valid Delay 80C186RP-10 80C186RP-12	C_L = 50 pF - 200 pF all outputs (except T_{CLTMV}) @10MHz C_L = 50 pF - 100 pF all outputs @12.5MHz	T_{CLAV}	 5 5	 50 36	ns
Address Hold 80C186RP-10 80C186RP-12		T_{CLAX}	 0 0		ns
Address Float Delay 80C186RP-10 80C186RP-12		T_{CLAZ}		 30 25	ns
Command Lines Float Delay 80C186RP-10 80C186RP-12		T_{CHCZ}		 40 33	ns
Command Lines Valid Delay (after Float) 80C186RP-10 80C186RP-12		T_{CHCV}		 45 37	ns
ALE Width (min) 80C186RP-10 80C186RP-12		T_{LHLL}	 T_{CLCL} - 30 T_{CLCL} - 30		ns
ALE Active Delay 80C186RP-10 80C186RP-12		T_{CHLH}		 30 25	ns
ALE Inactive Delay 80C186RP-10 80C186RP-12		T_{CHLL}		 30 25	ns
Address Hold to ALE Inactive (min) 80C186RP-10 80C186RP-12		T_{LLAX}	 T_{CHCL} - 20 T_{CHCL} - 15		ns
Data Valid Delay 80C186RP-10 80C186RP-12		T_{CLDV}	 5 5	 40 36	ns
Data Hold time 80C186RP-10 80C186RP-12		T_{CLDOX}	 3 3		ns
Data Hold After WR\ (min) 80C186RP-10 80C186RP-12		T_{WHDX}	 T_{CLCL} - 34 T_{CLCL} - 20		ns
Control Active Delay 1/ 80C186RP-10 80C186RP-12		T_{CVCTV}	 3 3	 56 47	ns
Control Active Delay 2/ 80C186RP-10 80C186RP-12		T_{CHCTV}	 5 5	 44 37	ns
Control Inactive Delay 80C186RP-10 80C186RP-12		T_{CVCTX}	 4 5	 44 37	ns

80C186RP AC ELECTRICAL CHARACTERISTICS - MASTER INTERFACE TIMING RESPONSES (continued) 1/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
DEN\ Inactive Delay (Non-Write Cycle)	C_L = 50 pF - 200 pF all outputs (except T_{CLTMV}) @10MHz	T_{CVDEX}			
80C186RP-10			5	56	ns
80C186RP-12			5	47	
Address Float to RD\ Active		T_{AZRL}			
80C186RP-10			0		ns
80C186RP-12			0		
RD\ Active Delay	C_L = 50 pF - 100 pF all outputs @12.5MHz	T_{CLRL}			
80C186RP-10			5	44	ns
80C186RP-12			5	37	
RD\ Inactive Delay		T_{CLRH}			
80C186RP-10			5	44	ns
80C186RP-12			5	37	
RD\ Inactive to Address Active (min)		T_{RHAV}			
80C186RP-10			T_{CLCL} - 40		ns
80C186RP-12			T_{CLCL} - 20		
HLDA Valid Delay		T_{CLHAV}			
80C186RP-10			5	40	ns
80C186RP-12			4	33	
RD\ Pulse Width (min)		T_{RLRH}			
80C186RP-10			$2T_{CLCL}$ - 46		ns
80C186RP-12			$2T_{CLCL}$ - 40		
WR\ Pulse Width (min)		T_{WLWH}			
80C186RP-10			$2T_{CLCL}$ - 34		ns
80C186RP-12			$2T_{CLCL}$ - 30		
Address Valid to ALE Low (min)		T_{AVLL}			
80C186RP-10			T_{CLCL} - 19		ns
80C186RP-12			T_{CLCL} - 15		
Status Active Delay		T_{CHSV}			
80C186RP-10			5	45	ns
80C186RP-12			5	35	
Status Inactive Delay		T_{CLSH}			
80C186RP-10			5	50	ns
80C186RP-12			5	35	
Timer Output Delay	100 pF max @ 10MHz	T_{CLTMV}			
80C186RP-10				48	ns
80C186RP-12				40	
Reset Delay	C_L = 50 pF - 200 pF all outputs (except T_{CLTMV}) @10MHz	T_{CLRO}			
80C186RP-10				48	ns
80C186RP-12				40	
Queue Status Delay		T_{CHQSV}			
80C186RP-10				28	ns
80C186RP-12				28	
Status Hold Time	C_L = 50 pF - 100 pF all outputs @12.5MHz	T_{CHDX}			
80C186RP-10			5		ns
80C186RP-12			5		

80C186RP AC ELECTRICAL CHARACTERISTICS - MASTER INTERFACE TIMING RESPONSES (continued) 1/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Address Valid to Clock High 80C186RP-10 80C186RP-12	C_L = 50 pF - 200 pF all outputs (except T_{CLTMV}) @10MHz C_L = 50 pF - 100 pF all outputs @12.5MHz	T_{AVCH}	 0 0		ns
LOCK\ Valid /Invalid Delay 80C186RP-10 80C186RP-12		T_{CLLV}	 5 5	 45 40	ns
DEN\ Inactive to DT/R\ Low 80C186RP-10 80C186RP-12		T_{DXDL}	 0 0		ns

80C186RP AC ELECTRICAL CHARACTERISTICS - CHIP SELECT TIMING RESPONSES 1/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
Chip-Select Active Delay 80C186RP-10 80C186RP-12		T_{CLCSV}	 	 45 33	ns
Chip-Select Hold from Command Inactive 80C186RP-10 80C186RP-12		T_{CXCSX}	 T_{CLCL} - 10 T_{CLCL} - 10		ns
Chip-Select Inactive Delay 80C186RP-10 80C186RP-12		T_{CHCSX}	 5 5	 40 36	ns

80C186RP AC ELECTRICAL CHARACTERISTICS - CLKIN REQUIREMENTS 1/ 4/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
CLKIN Period 6/ 80C186RP-10 80C186RP-12		T_{CKIN}	 50 40	 1000 1000	ns
CLKIN Fall Time 80C186RP-10 80C186RP-12	3.5 to1.0 V 2/	T_{CKHL}	 	 5 5	ns
CLKIN Rise Time 80C186RP-10 80C186RP-12	1.0 to 3.5 V 2/	T_{CKLH}	 	 5 5	ns
CLKIN Low Time 80C186RP-10 80C186RP-12	1.5V 3/	T_{CLCK}	 23 18	 	ns
CLKIN High Time 80C186RP-10 80C186RP-12	1.5 V 3/	T_{CHCK}	 23 18	 	ns

80C186RP AC ELECTRICAL CHARACTERISTICS - CLKOUT TIMING 1/ 5/

(V_{CC}=5V ± 10%, V_{PP} = V_{SS}, T_A = -55 to +125°C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	MAX	UNIT
CLKIN to CLKOUT Skew		T_{CICO}			
80C186RP-10				25	ns
80C186RP-12				21	
CLKOUT Period 6/		T_{CLCL}			
80C186RP-10			100	2000	ns
80C186RP-12			80	2000	
CLKOUT Low Time	1.5 V	T_{CLCH}			
80C186RP-10			0.5 T_{CLCL} - 8		ns
80C186RP-12			0.5 T_{CLCL} - 7		
CLKOUT High Time	1.5 V	T_{CHCL}			
80C186RP-10			0.5 T_{CLCL} - 8		
80C186RP-12			0.5 T_{CLCL} - 7		
CLKOUT Rise Time 2/	1.0 to 3.5 V	T_{CH1CH2}			
80C186RP-10				10	ns
80C186RP-12				10	
CLKOUT Fall Time 2/	3.5 to 1.0V	T_{CL2CL1}			
80C186RP-10				10	ns
80C186RP-12				10	

Note:

1/ All timings are measured at 1.5V and 100pF loading on CLKOUT unless otherwise noted. All output test conditions are with C_L = 50 - 200pF (10MHz) and C_L = 50 - 100pF (12.5MHz). For A.C. tests, input V_{IL} = 0.45V and V_{IN} = 2.4V except at X1 where V_{IH} = V_{CC} - 0.5V.

2/ These values are supplied for design purposes.

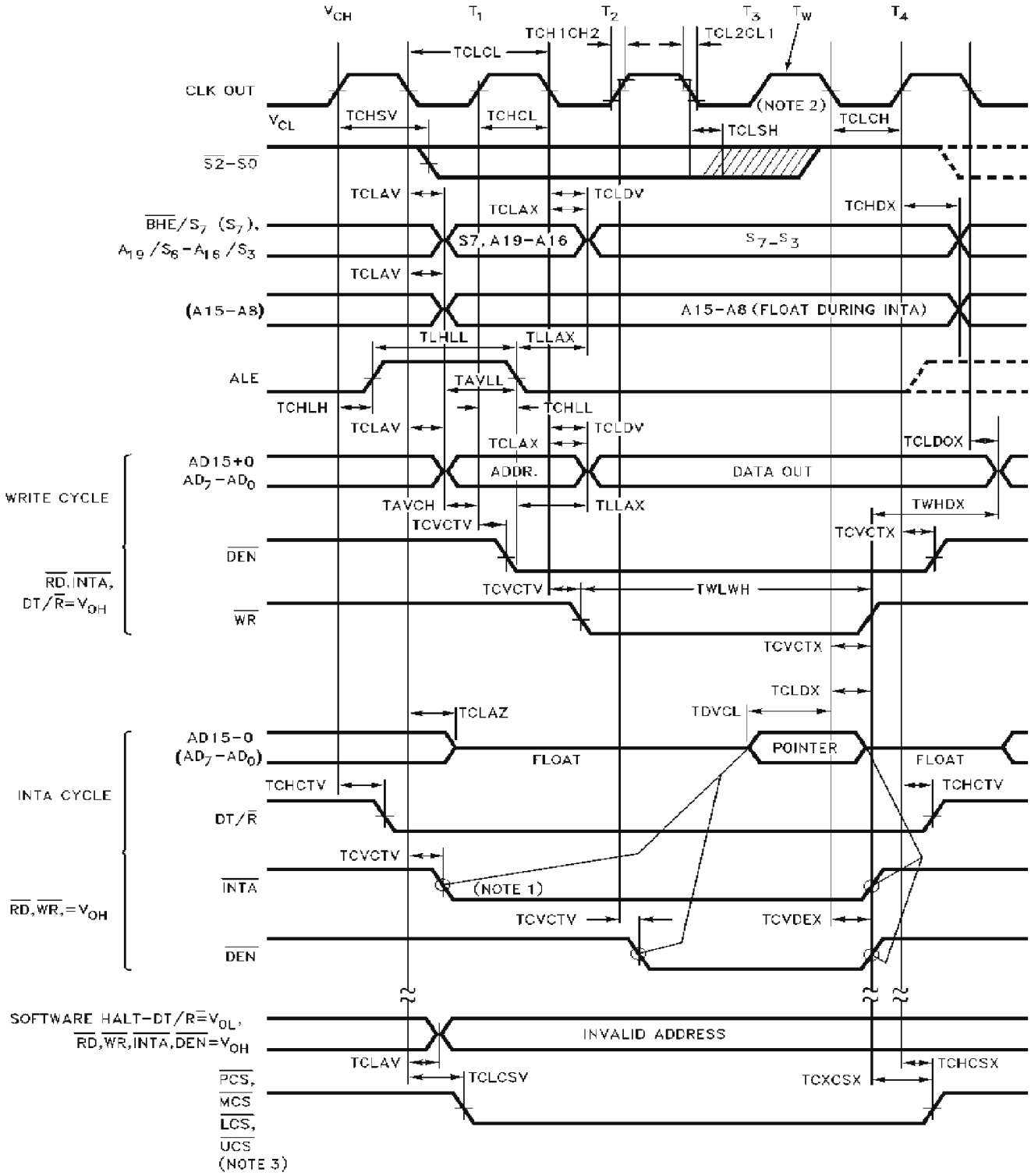
3/ T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 45% of T_{CKIN}.

4/ Measurements taken with external clock input to X1 and X2 not connected.

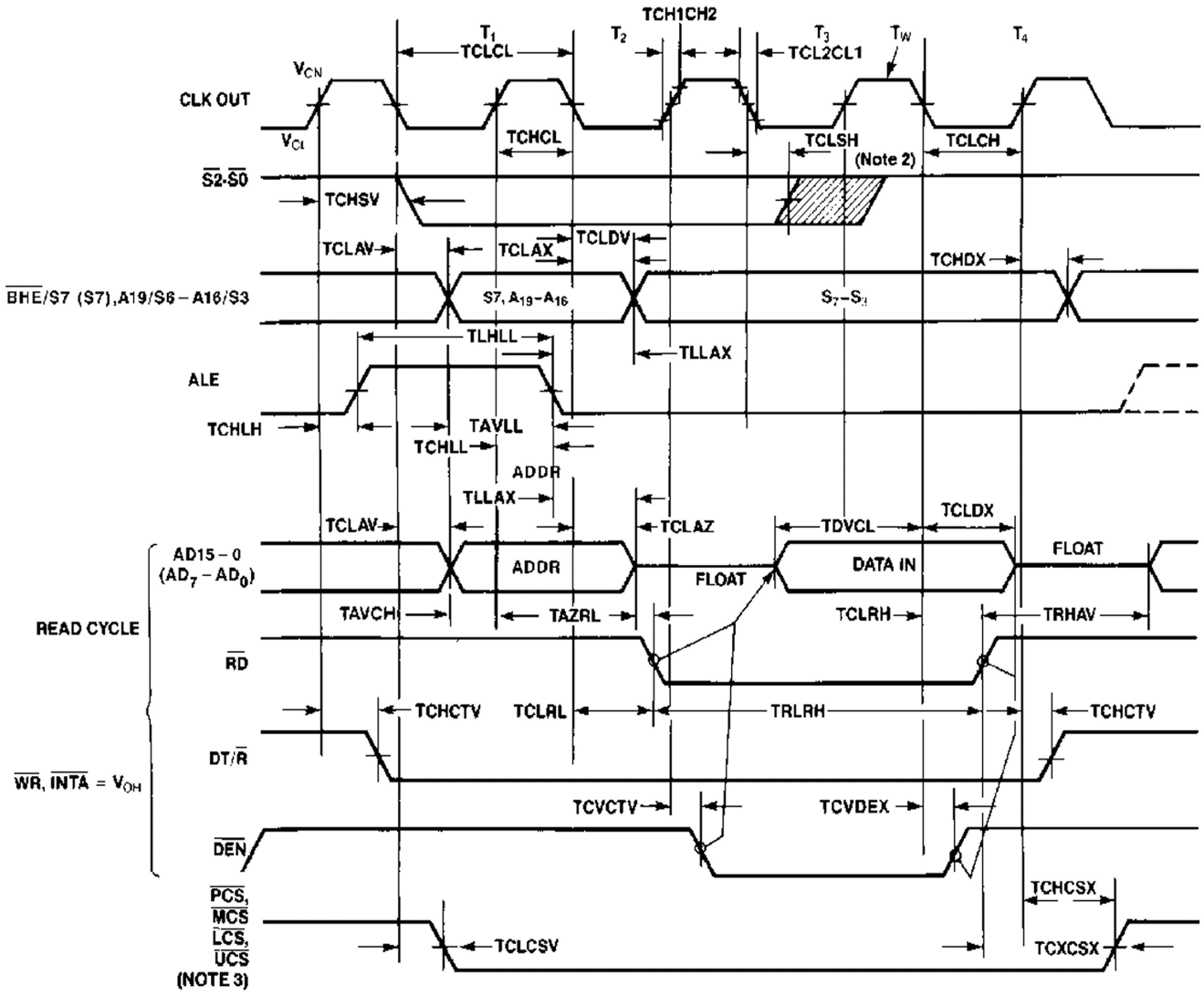
5/ 200pF load maximum for 10MHz or less.

6/ Tested functionally.

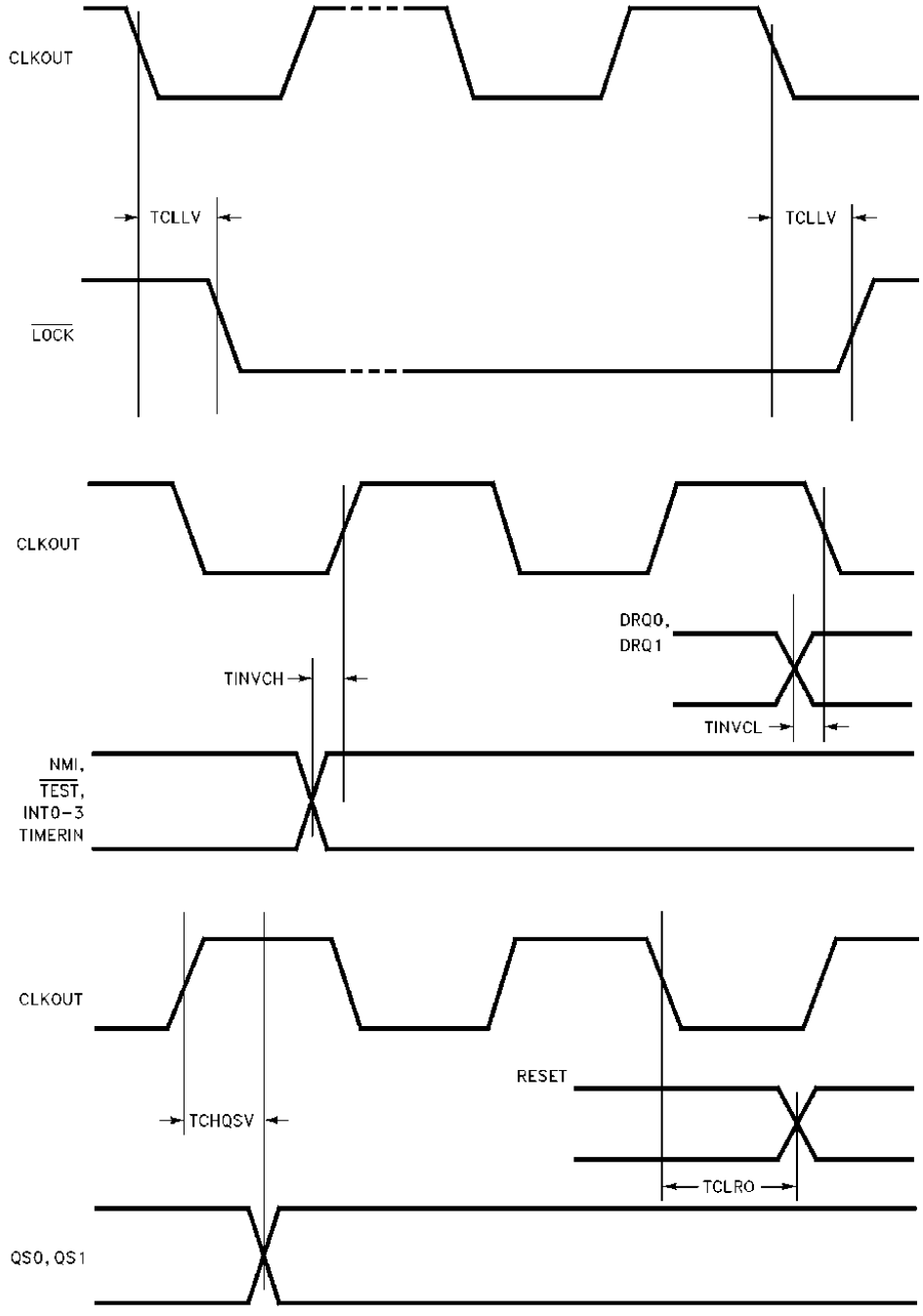
MAJOR CYCLE TIMING



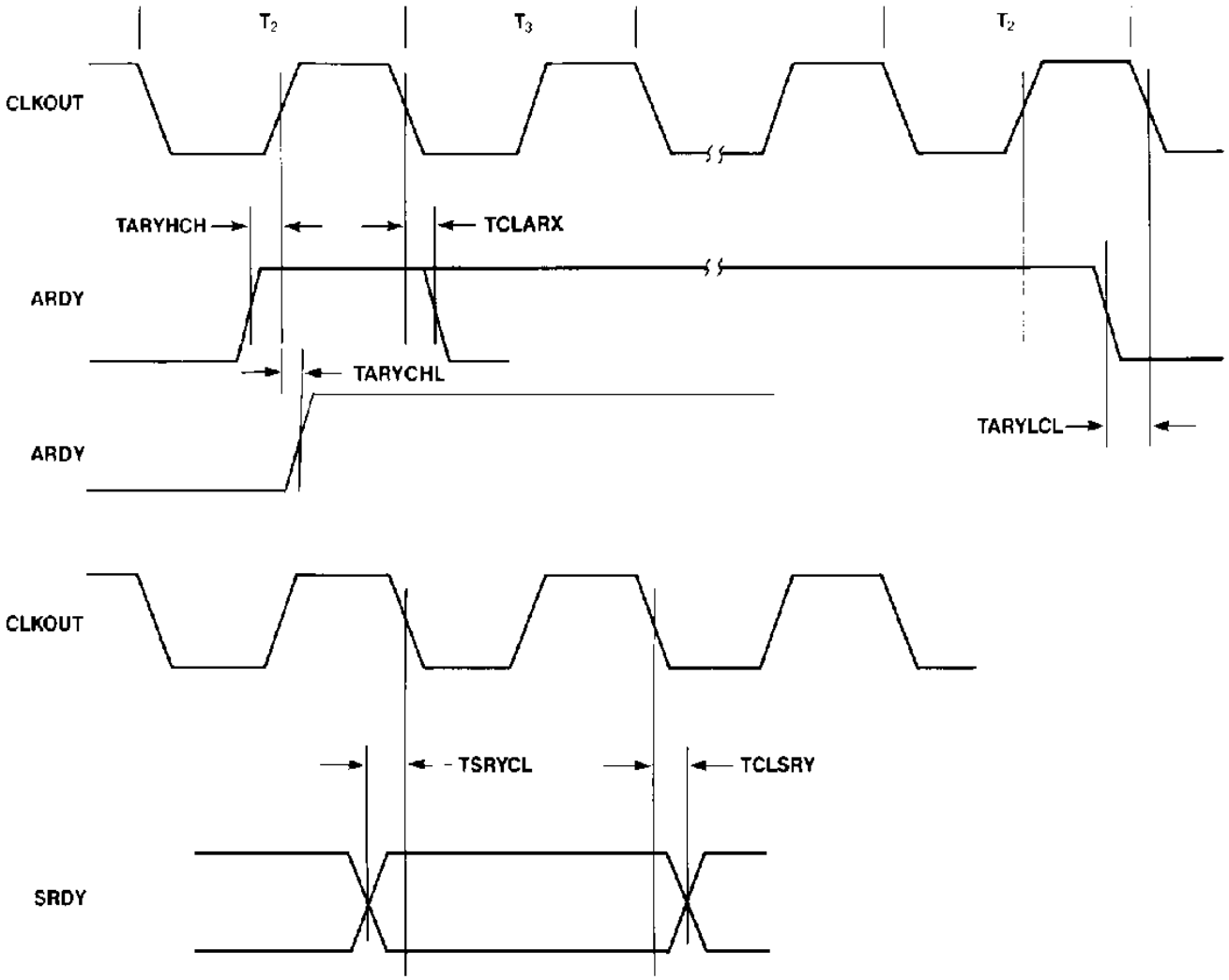
MAJOR CYCLE TIMING (CONTINUED)



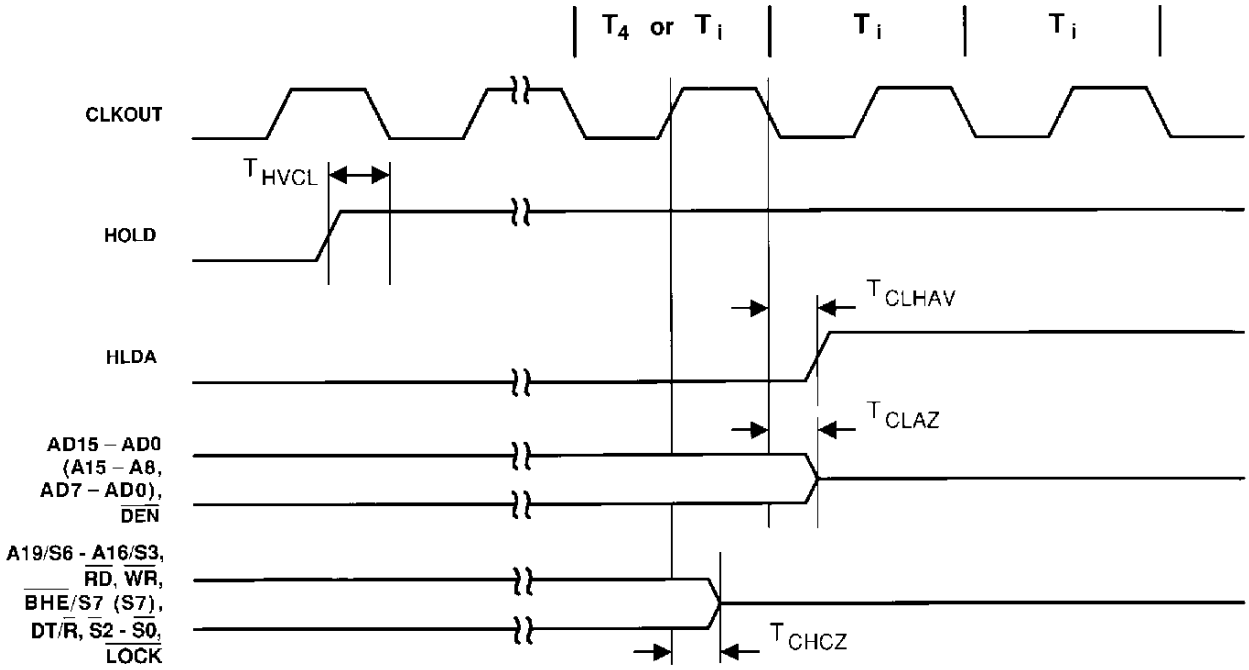
Note:
1. The data hold time last only until $\overline{\text{INTA}}$ goes inactive, even if the $\overline{\text{INTA}}$ transition occurs prior to TCLDX (min).
2. INTA occurs one clock later in Slave Mode.
3. Status inactive just prior to T4.
4. Latched A1 and A2 have the same timings as $\overline{\text{PCS5}}$ and $\overline{\text{PCS6}}$.
5. For Write cycle followed by Read.



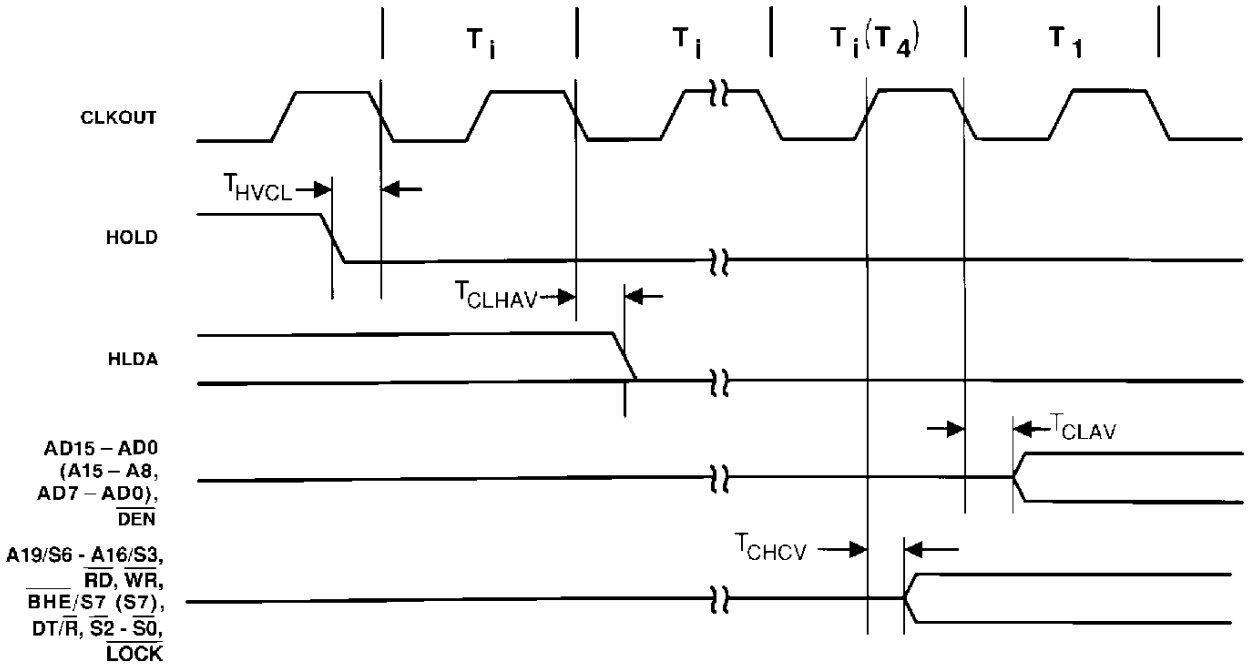
READY TIMING



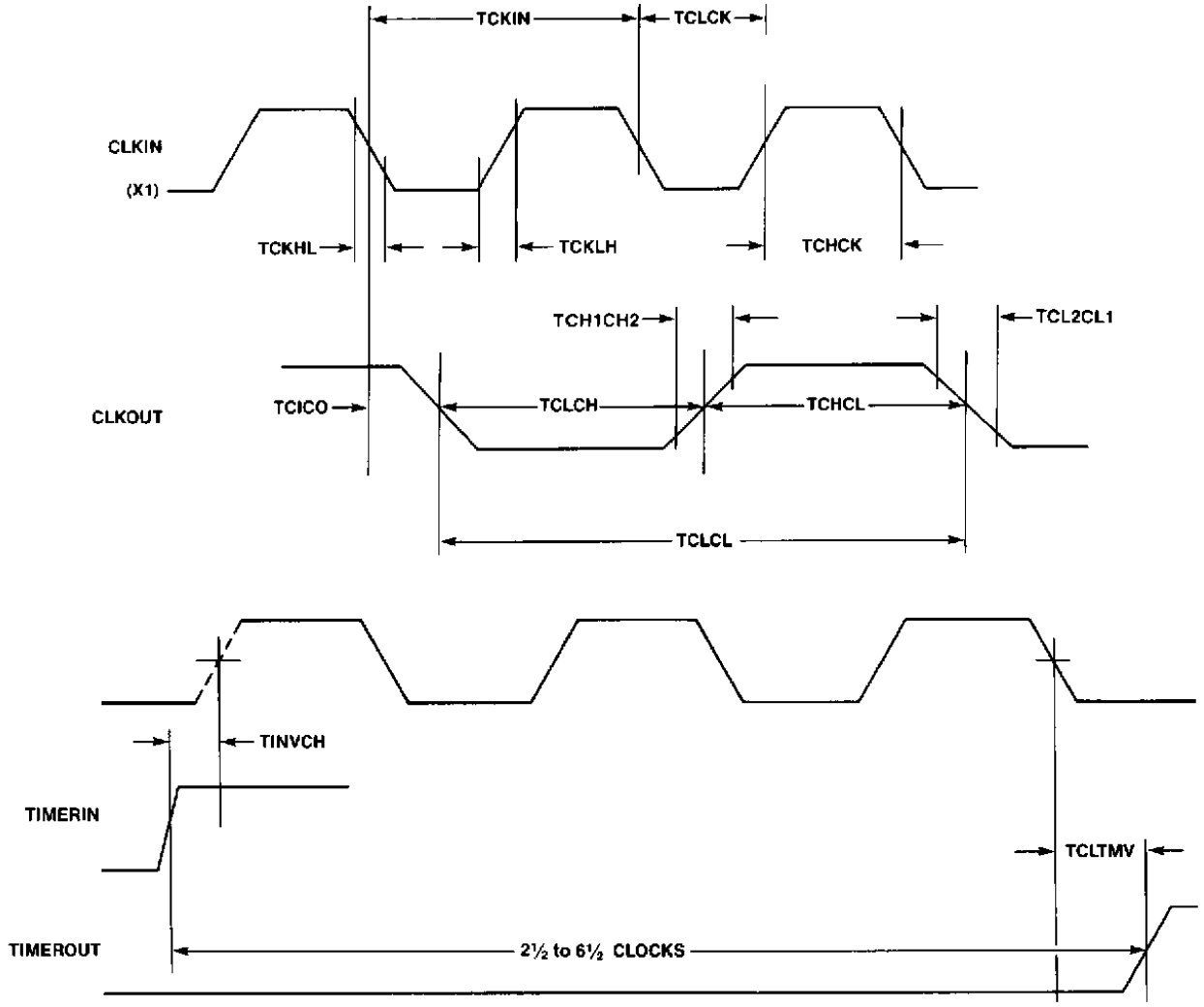
HOLD-HLDA TIMING (ENTERING HOLD)

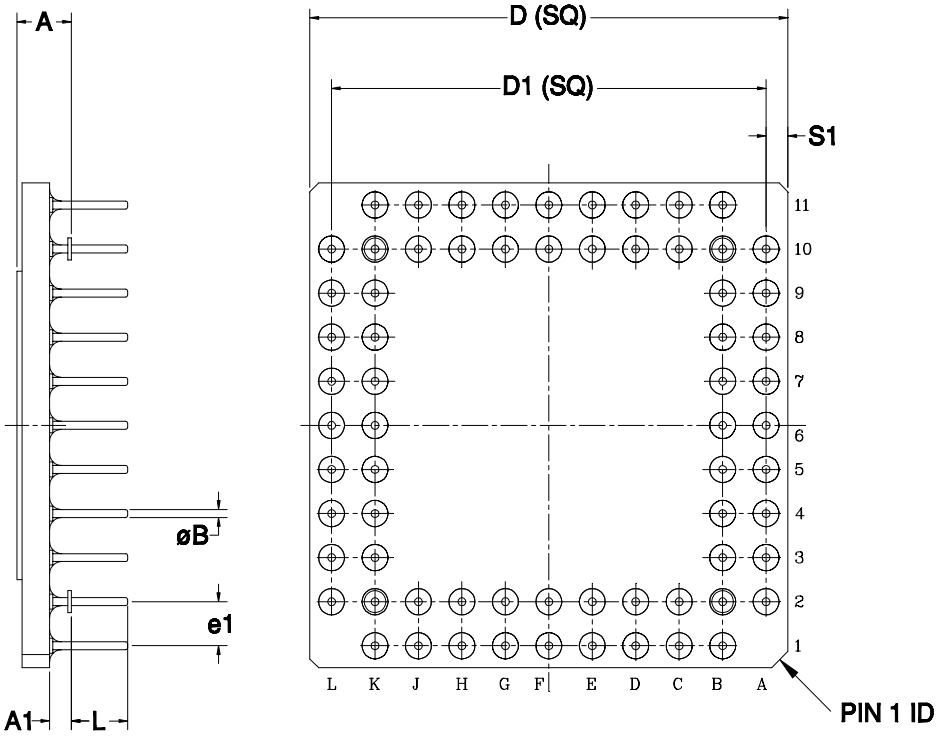


HOLD-HLDA TIMING (LEAVING HOLD)



TIMER ON 80C186





68 LEAD PIN GRID ARRAY PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.127	0.150	0.163
A1	0.065	0.070	0.075
B	0.016	0.018	0.020
D	1.092	1.100	1.108
D1	0.990	1.000	1.010
e1	0.095	0.100	0.105
Q	0.032	0.035	0.038
L	0.100	0.114	0.130
S1	0.042	0.050	0.058
N	68		

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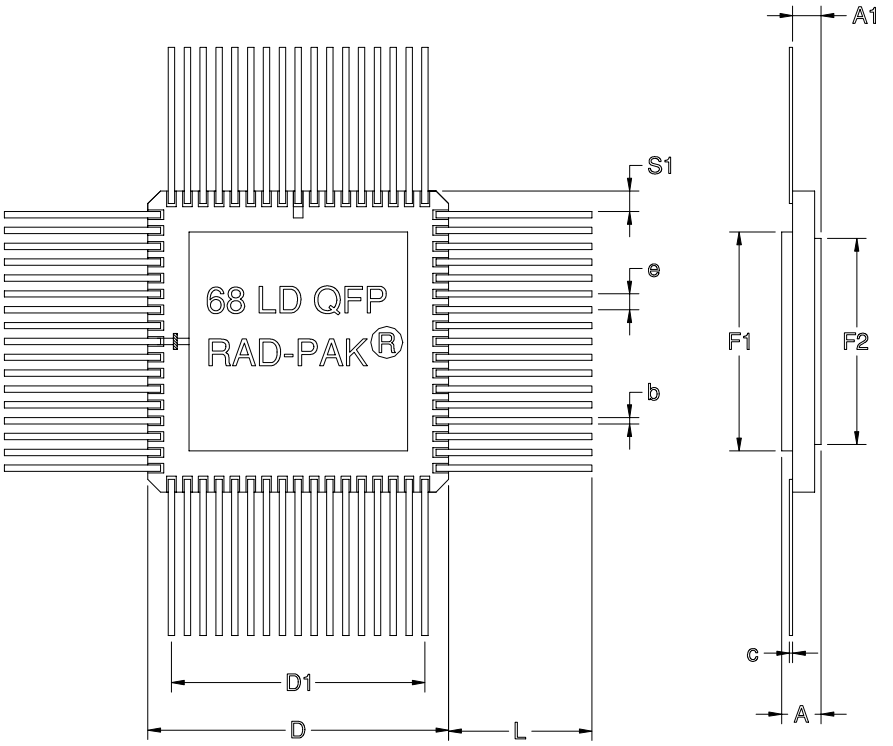
NOTE: ALL DIMENSIONS IN INCHES



SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.153	0.168	0.183
b	0.016	0.018	0.020
c	0.008	0.010	0.012
D	0.940	0.950	0.960
D1		0.800 BSC	
e		0.050 BSC	
S1	0.013	0.066	--
F1	0.645	0.650	0.655
F2	0.645	0.650	0.655
L	0.477	0.487	0.497
A1	0.111	0.123	0.135
N		68	

Q68-02
(All Dimensions are in Inches)