82562EH 1 Mb/s HomePNA LAN Connect Option

Application Note

Revision 1.0

June 2000

Order Number: 278312-001

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1.0 Overview

This application note provides information and design specific considerations for system designers interested in using the 82562EH in design applications.

2.0 Description

The 82562EH is a HomePNA compliant single-chip LAN Connect Option component designed for home networking applications.

Some features of the 82562EH are:

- Compliant with the *Home Phoneline Networking Alliance (HomePNA*) Specification* Revision 1.1.
- Contains a LAN Connect Interface for connection to the Intel I/O Communications Hub2 (ICH2).
- Fully supports the Home Media Independent Interface (hMII).
- Provides full hMII management (using the MII management data clock (mdc) and MII management data I/O (mdio) pins).
- Provides a General Purpose Serial Interface (GPSI 7-wire interface).
- Is a 3.3-V device optimized for low-power operation.
- Is available in a 64-pin TQFP package.

3.0 Related Documents

Other documentation about the 82562EH is listed in the following table:

Title	Location
82562EH 1 Mb/s HomePNA LAN Connect Option Datasheet, Order Number: 278313	http://developer.intel.com/design/network/

4.0 82562EH Interfaces

The 82562EH support three different interfaces:

- hMII (see Figure 1): Home Media Independent Interface (16 wire) for connecting to an external Media Access Controller (MAC)
- GPSI (see Figure 2): General Purpose Serial Interface (7 wire) for connecting to an external Media Access Controller (MAC)
- LAN Connect Interface (see Figure 3): LAN Connect Interface (4 wire) for connecting to the LAN controller in Intel ICH2 platforms

Table 1 describes the signals used and their status in each mode:

Table 1. Interface Signal Status

Signal	hMII	GPSI	LAN Connect I/F
mii/jord	Pull-up resistor	Pull-down resistor	Pull-down resistor
phad<4>/gpsi	PHY address	Pull-up resistor	Pull-down resistor
phad<3>/cs_l	PHY address	Pull-down resistor	Pull-down resistor
isolate	Pull-down resistor	Pull-down resistor	Pull-down resistor
test_en	Pull-down resistor	Pull-down resistor	Pull-down resistor
pint_l	Pull-up resistor	Pull-up resistor	Not connected
txd<3:1>	Active, connect to the controller	Pull-down resistor	Pull-down resistor
txd<0>/jtxd	Active, connect to the controller	Active, connect to the controller	Active, connect to the controller
tx_cl/jclk	Active, connect to the controller	Active, connect to the controller	Active, connect to the controller
rxd<3:1>	Active, connect to the controller	Not connected	Not connected
rxd<0>/jrxd	Active, connect to the controller	Active, connect to the controller	Active, connect to the controller
rx_clk	Active, connect to the controller	Active, connect to the controller	Not connected
tx_en	Active, connect to the controller	Active, connect to the controller	Pull-down resistor
rx_dv	Active, connect to the controller	Not connected	Not connected
crs	Active, connect to the controller	Active, connect to the controller	Not connected
col	Active, connect to the controller	Active, connect to the controller	Not connected
mdc	Active, connect to the controller	Active, connect to the controller	Pull-down resistor
mdio	Active, connect to the controller	Active, connect to the controller	Pull-down resistor

Figure 1. Home Media Independent Interface

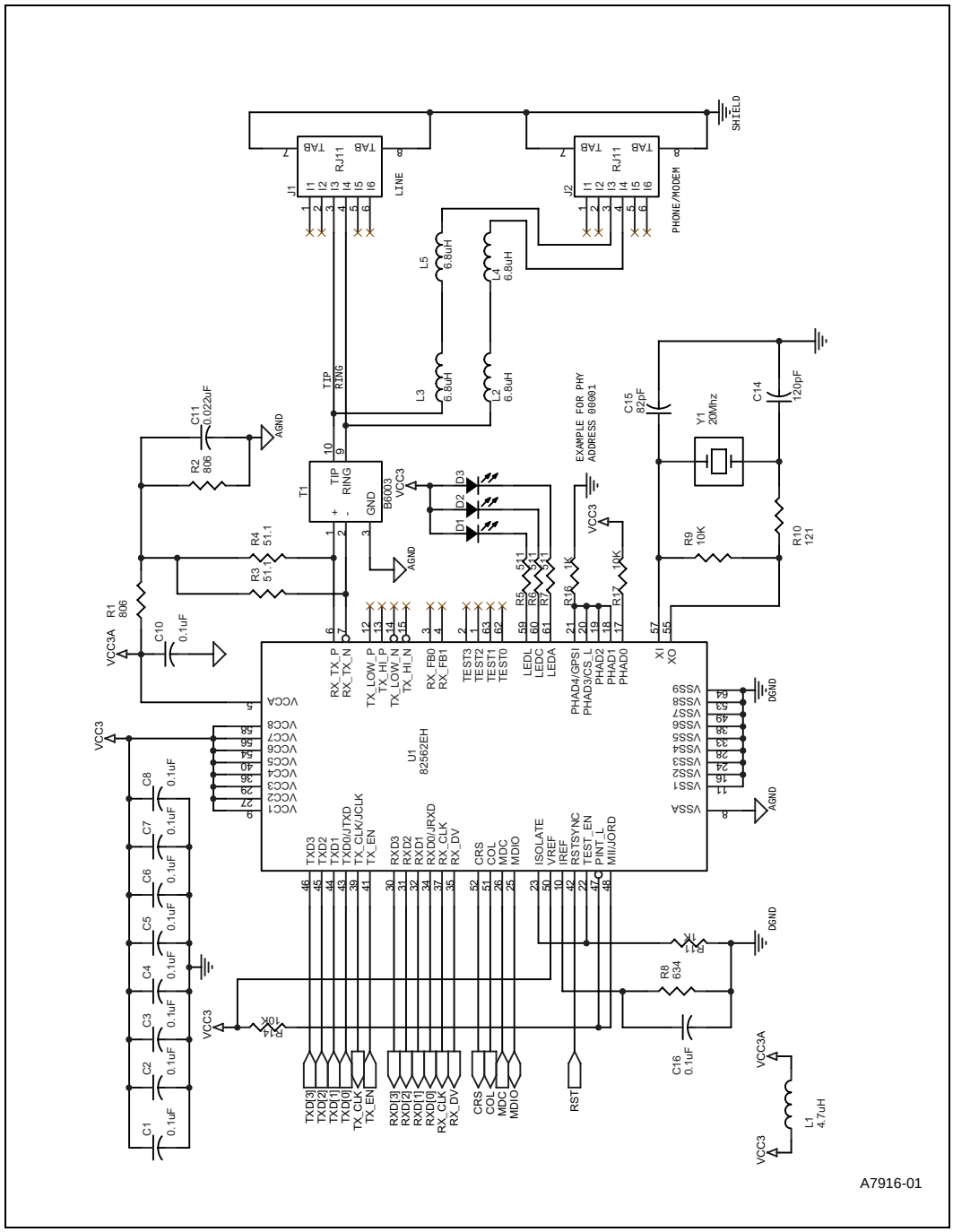


Figure 2. General Purpose Serial Interface

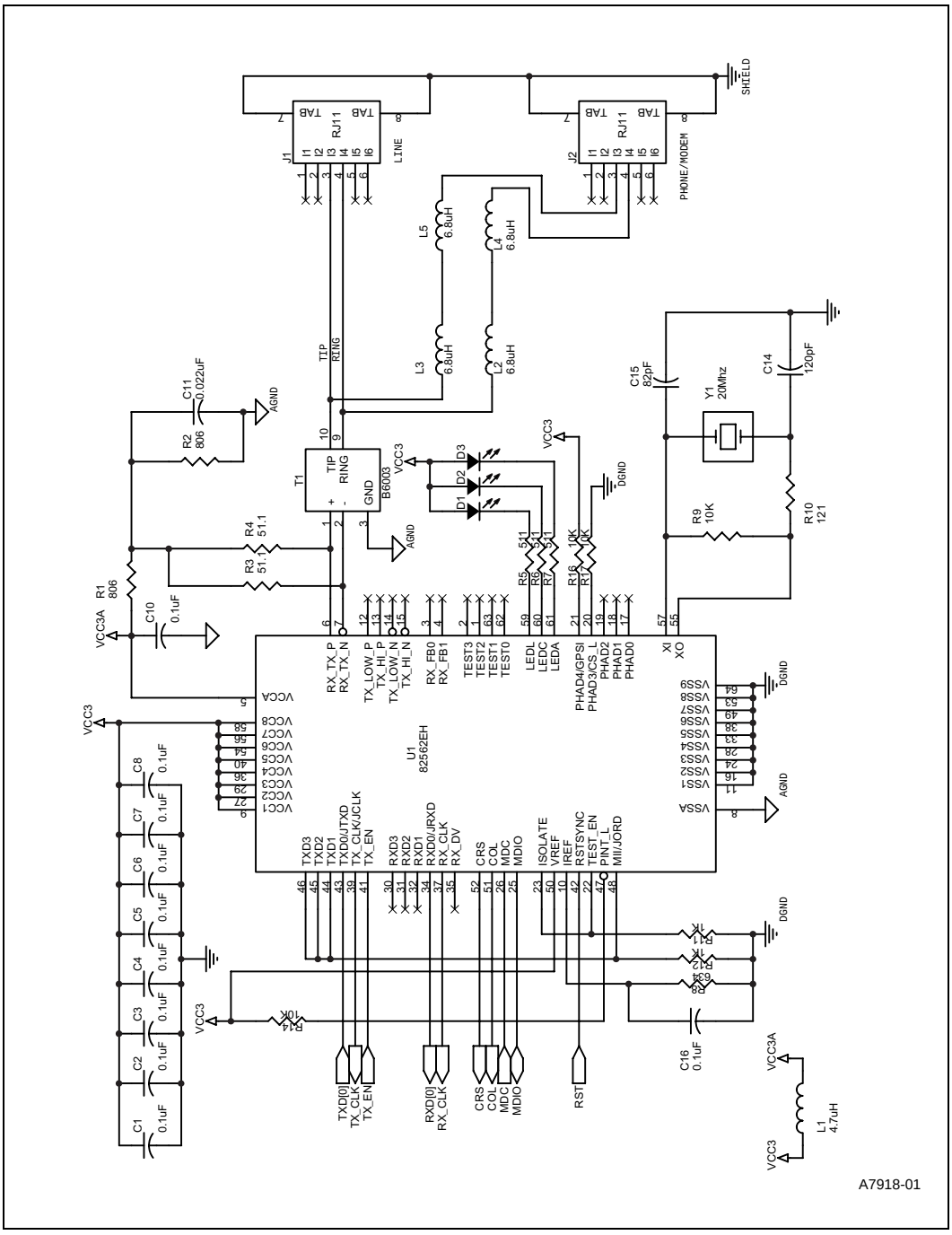
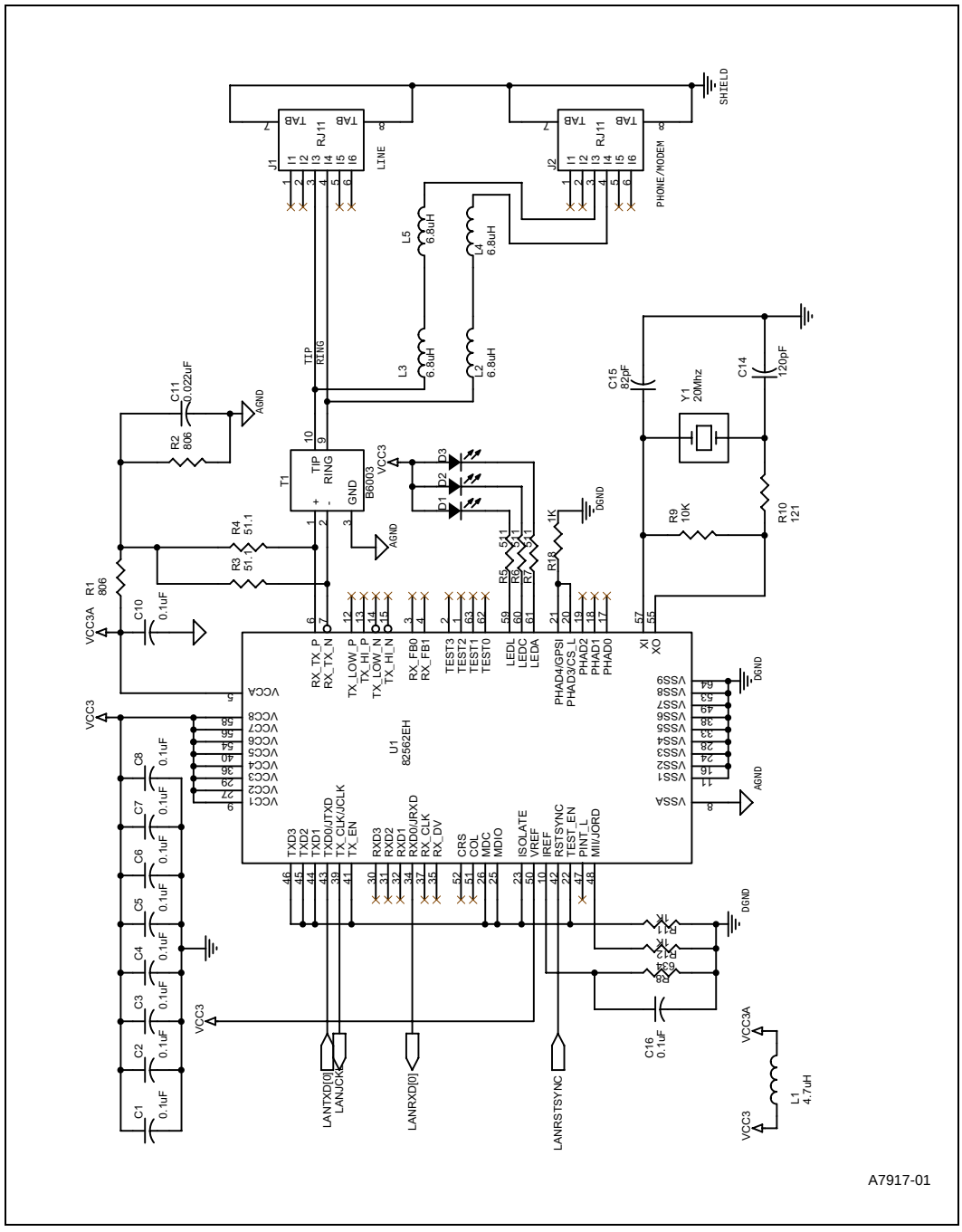


Figure 3. LAN Controller Interface



5.0 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA interface is important, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

5.1 Crystals and Oscillators

To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA magnetics module to prevent interference of communication. The retaining straps of the crystal (if they exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

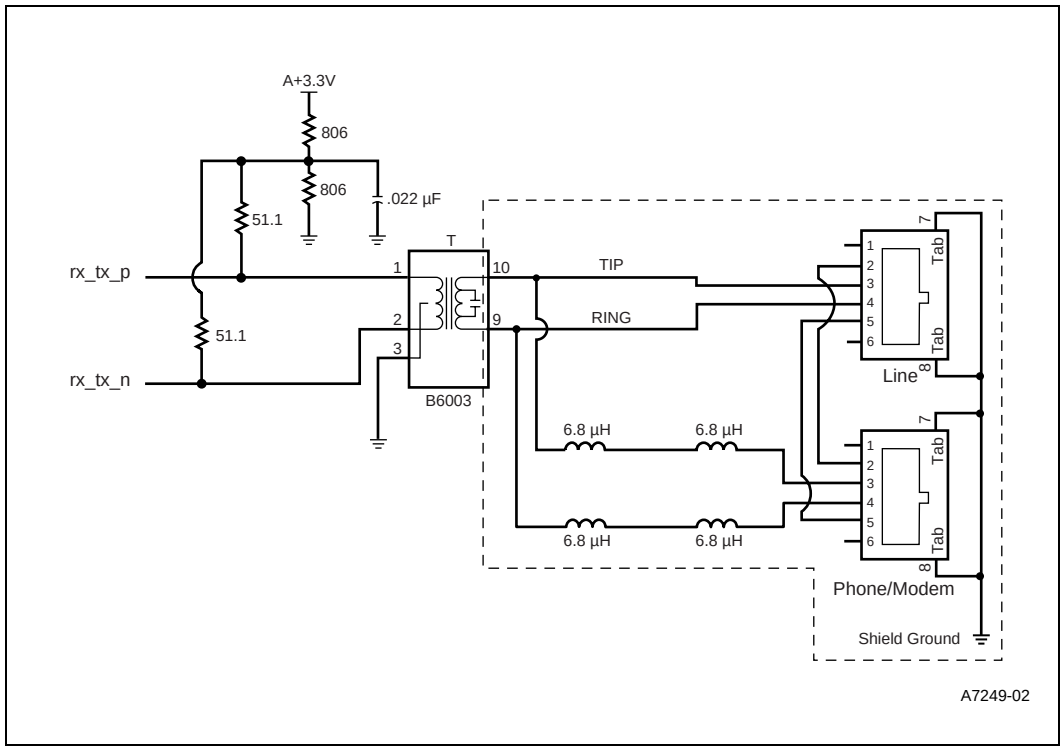
5.2 Termination Resistors

This section describes the HomePNA termination resistor guidelines.

5.2.1 Phoneline HomePNA Termination

The transmit/receive signal pair is terminated with 51.1 ohm resistors and pulled up to the mid-point of the analog 3.3 V supply, as shown in Figure 4. This termination should be placed as close as possible to the 82562EH.

Figure 4. HomePNA Circuit



The filter and magnetics component integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.

One RJ-11 jack (labeled “Line” in Figure 4) allows the node to be connected to the phoneline, and the second jack (labeled “Phone/Modem) allows other down line devices to be connected at the same time. This second connector is not required by the HomePNA. However, typical PCI adaptors and PC motherboard implementations are likely to include it for user convenience.

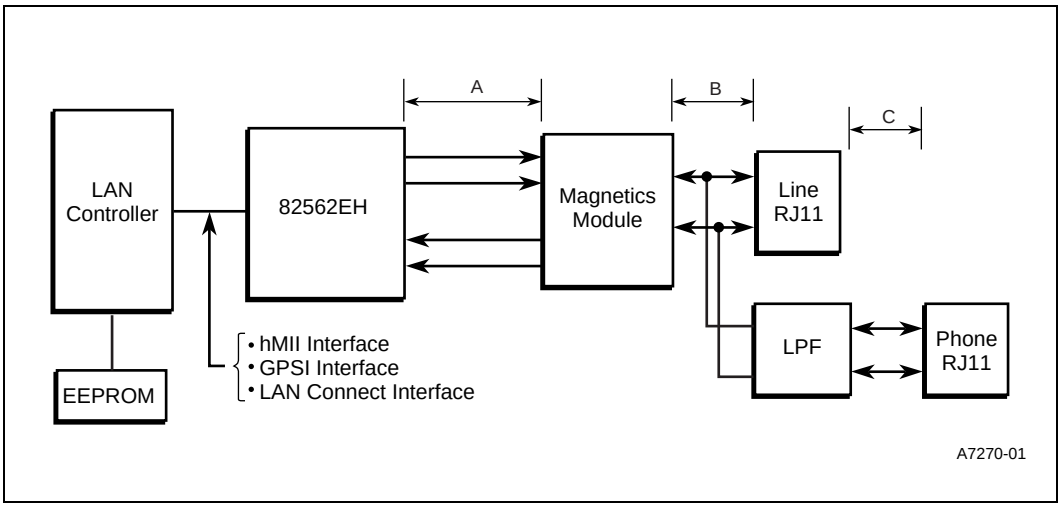
A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA to minimize interference between the HomePNA connection and a POTs voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is approximately set at 1.1 Mhz.

Please refer to the HomePNA website at **http://www.homepna.org** for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

6.0 Critical Dimensions

There are three dimensions to consider during layout. Distance ‘B’ from the line RJ11 connector to the magnetics module, distance ‘C’ from the phone RJ11 to the LPF (if implemented), and distance ‘A’ from 82562EH to the magnetics module, as shown in Figure 5.

Figure 5. Critical Dimension for Component Placement



6.1 Distance from the Magnetics Module to the Line RJ11

This distance “B” should be given highest priority and should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

6.2 Distance from the 82562EH to the Magnetics Module

Due to the high-speed of signals present, distance “A” between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance from connectors to the magnetics module.

And in general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

6.3 Distance from the LPF to the Phone RJ11

This distance ‘C’ should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions. Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

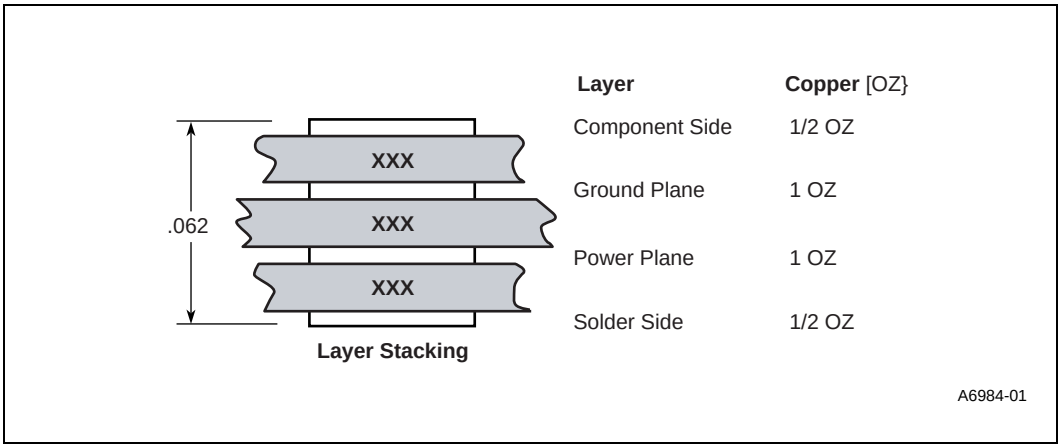
7.0 General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of cross-talk and propagation delays on sections of the board where high speed signals exist.

For example, as shown in Figure 6, the recommended stack-up for a four layer would be as follows:

- First Layer (Top): Signal/component
- Second Layer: Ground plane
- Third Layer: Power plane
- Fourth Layer (Bottom): Signal

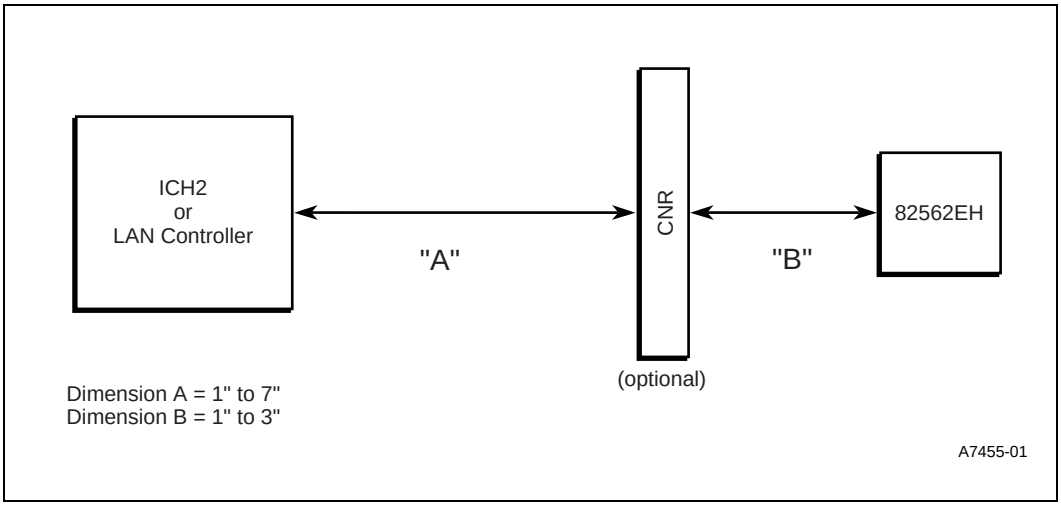
Figure 6. PCB Working Assembly Layer Stack



7.1 ICH2/LAN Controller Trace Guidelines

Figure 7 shows the 82562EH LAN-on-Motherboard suggested trace lengths using an optional Communication Network Riser Card (CNR) connector. Target trace impedance should be 60 ohms. In addition, maximum mismatch between clock and any data signals should not exceed 0.5 inches

Figure 7. 82562EH/ICH2 Trace Length Limitations



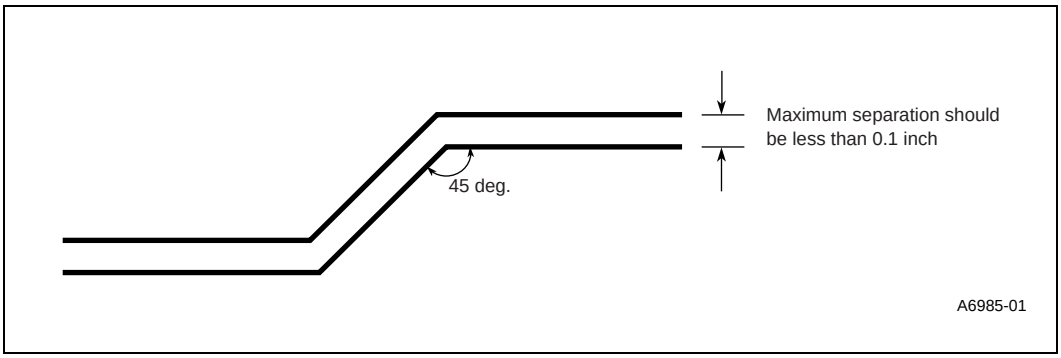
7.2 Trace Routing

Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

- Keep maximum separation distance between differential pairs to 6 mils. However, it is more important to keep the signal trace lengths equal to each other than to observe the 6 mil separation throughout the route.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead, as shown in Figure 8.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 8. Trace Routing



7.3 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and width as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane.

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signals terminations should be as short as possible and plated vias to the decoupling capacitors should be larger in diameter then standard signal vias to decrease series inductance.

8.0 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a minimum gap of 70 mil between all differential pairs and other nets, but group associated differential pairs together.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize cross-talk which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing Phoneline traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.

9.0 Power and Ground Connections

Some rules to follow for power and ground connections:

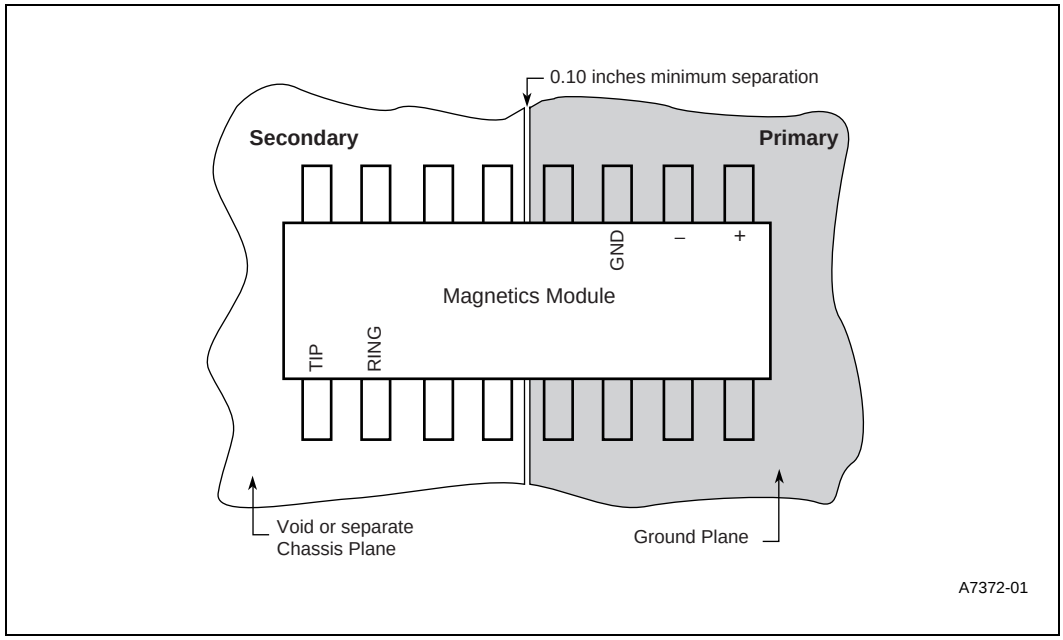
- All VDD pins should be connected to the same power supply.
- All VSS pins should be connected to the same ground plane.
- Use one decoupling capacitor per power pin.
- Place decoupling as close as possible to power pins.
- For best performance place decoupling capacitors on the backside of the PCB directly under the analog power supply pins for the 82562EH, with equal distance from both pins of the capacitor to power/ground.
- Connect AGND and DGND at a single point between pin 8 and pin 11.

The analog power supply pins for 82562EH (VCCA) should be isolated from the digital (VCC) through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between VDD and VSS, and VDDA and VSSA power supplies.

10.0 General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum, as shown in Figure 9.

Figure 9. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections, and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow which will help reduce circuit inductance in both backplanes and motherboards.

- Route traces over a continuous plane with no interruptions (do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling.
- Noisy digital grounds may effect sensitive DC subsystems.
- All ground vias should be connected to every ground plane and every power via connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics which can radiate EMI.
- Void the power plane beneath the filter/transformer module and RJ11 connector, and include a separate shield ground plan under the magnetics secondary side (port side). By removing power planes beneath the transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized.
- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.5 mm (59.0 mil). This is a critical requirement needed to pass FCC part 68 testing for phoneline connection.

11.0 A 4-Layer Board Design

11.1 Top Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

11.2 Ground Plane

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module.

11.3 Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply planes VDDA and VSSA.

11.4 Bottom Layer Routing

The digital high speed signals, which include all of the LAN Connect I/F signals, are routed on the bottom layer.

12.0 Recommended Components

Table 2 contains recommended components for use with the 82562EH.

Table 2. Recommended Components

Manufacturer	Part Number
Y1 - 20 Mhz 0.005% Crystal Oscillator	
Toyocom	TN4-30695
Toyocom	SM/18@20
Fox Electronic	HC49SD-20MHZ-18PF
Raltron	AS-20.000-18-SMD-T
KDS	DS200-18 T/R
L1 - 4.7uH, 30 mA Inductor	
TDK	MLF2012A4R7KTA1N
Murata	LQG21N4R7K10T2
L2, L3, L4, L5, L6 6.8 uH Inductor	
TDK	NL322522TL-6R8J
T1 - B6003 Magnetics Module	
Pulse Engineering	B6003T

13.0 Stepping Initialization Sequence

For optimal performance the 82562EH needs to be initialized. The initialization process is divided into three stages:

- Stage 1 – Setting the CSRs to Test mode.
- Stage 2 – Performing the Noise Floor calculation.
- Stage 3 – Setting the CSRs to Working mode.

The first stage prepares the 82562EH for the second stage. The second stage finds the optimal noise_floor value based on feedback from chip. The last stage returns the CSRs to normal operating mode values.

The following sections and the flow chart in Figure 10 and Figure 11 describe the detailed steps for each stage.

Note: This initialization sequence is only needed when operating in the hMII and GPSI modes. In LAN Connect mode the NDIS driver performs this function.

13.1 Switching to Test Mode

Write the following values to the CSRs (note that the write-order is significant).

To switch between pages modify the CONTROL register RAP bit (bit 0). Use the read-modify-write method.

- AFE_CONTROL1 (Page 1 - address 12H) to a value of A600.
- AFE_CONTROL2 (Page 1 - address 13H) to a value of 0100.
- RX_CONTROL (Page 0 - address 1BH) to a value of 0008.
- STATUS_MODE (Page 0 - address 11H) to a value of 0100.
- NSE_ATTACK/EVENTS (Page 0 - address 1AH) to a value of 0022.
- NOISE/PEAK (Page 0 - address 18H) to a value of 7F10.

13.2 Noise Floor Calculation

Follow the steps described in Figure 10 and Figure 11. The notes listed here (Notes 1 - 6) are referenced in the flow chart.

1. Clear noise action should be done by setting the Clear NSE_EVENTS (CNSEVR) bit of the CONTROL register (address 10H, bit 6). This bit is self cleared. Use the read-modify-write method.
2. The Noise events (NSE_EVNTS) value is the high byte of the NSE_ATTACK/EVENTS register (address 1AH, bits<15:8>).
3. The Noise Floor (NSE_FLR) is the low byte of NSE_FLOOR/CEILING register (address 19H, bits<7:0>). The value of the high byte, Peak ceiling (NSE_CLNG), must always be written as D0H.

4. The Stop and Restart PHY logic procedure should be performed as follows:
   - Read the CONTROL register (address 10H).
   - Set the Stop PHY (STP) bit (bit 4) and write to the CONTROL register.
   - Clear the Stop PHY (STP) bit (bit 4) and write to the CONTROL register.
5. The PEAK is the high byte of the NOISE/PEAK register (address 18H, bits <15:8>). When modifying this field use the read-modify-write method.
6. The NOISE is the low byte of the NOISE/PEAK register (address 18H, bits <7:0>).

13.3 Setting CSRs to Working Mode

To switch between Pages modify the CONTROL register RAP bit (bit 0). Use the read-modify-write method.

- NSE_EVENTS/ATTACK (Page 0 - address 1AH) to a value of FFF4.
- RX_CONTROL (Page 0 - address 1BH) to a value of 0008.
- NOISE/PEAK (Page 0 - address 18H) to a value of 7F10.
- AFE_CONTROL1 (Page 1 - address 12H) to a value of 6600.

Figure 10. Initialization Algorithm (Part 1)

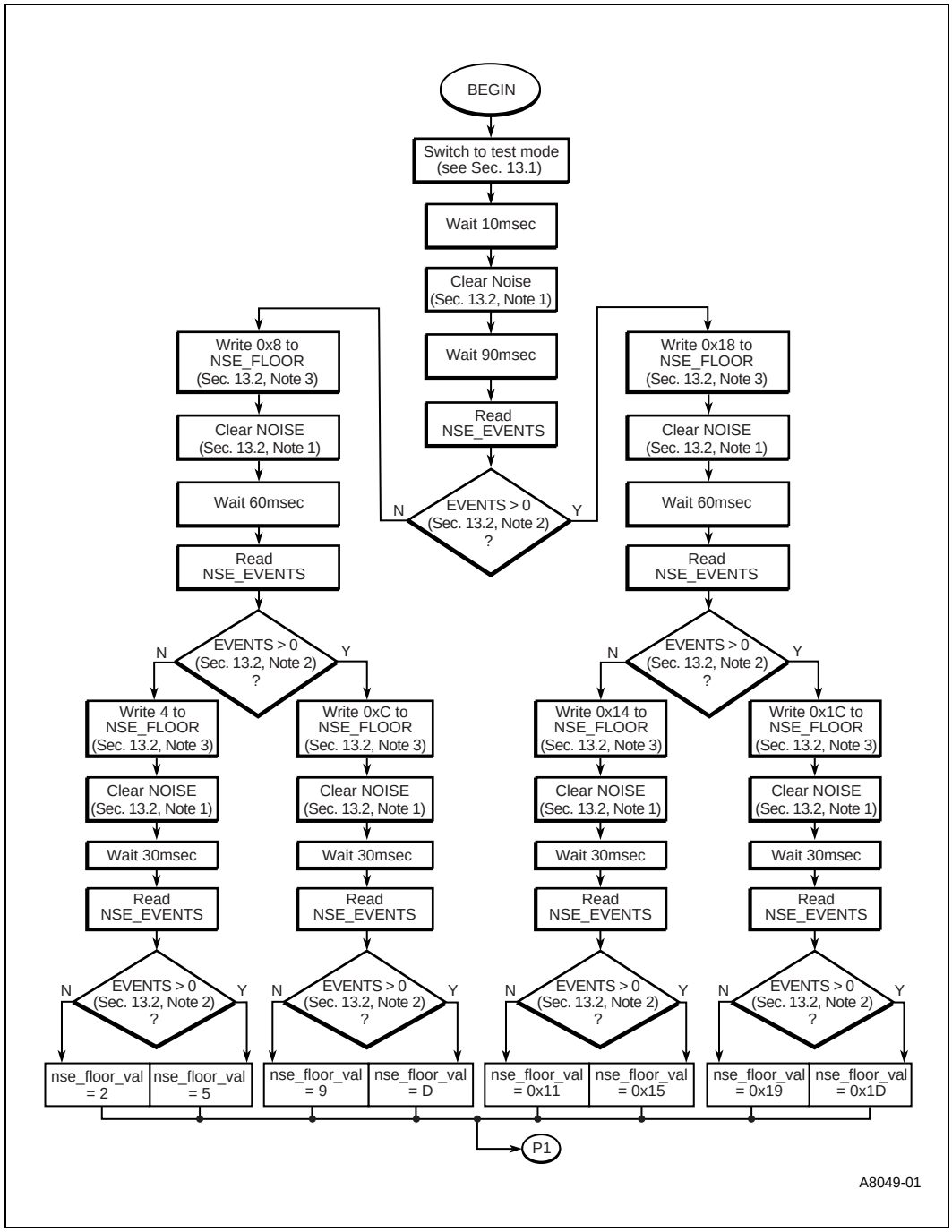
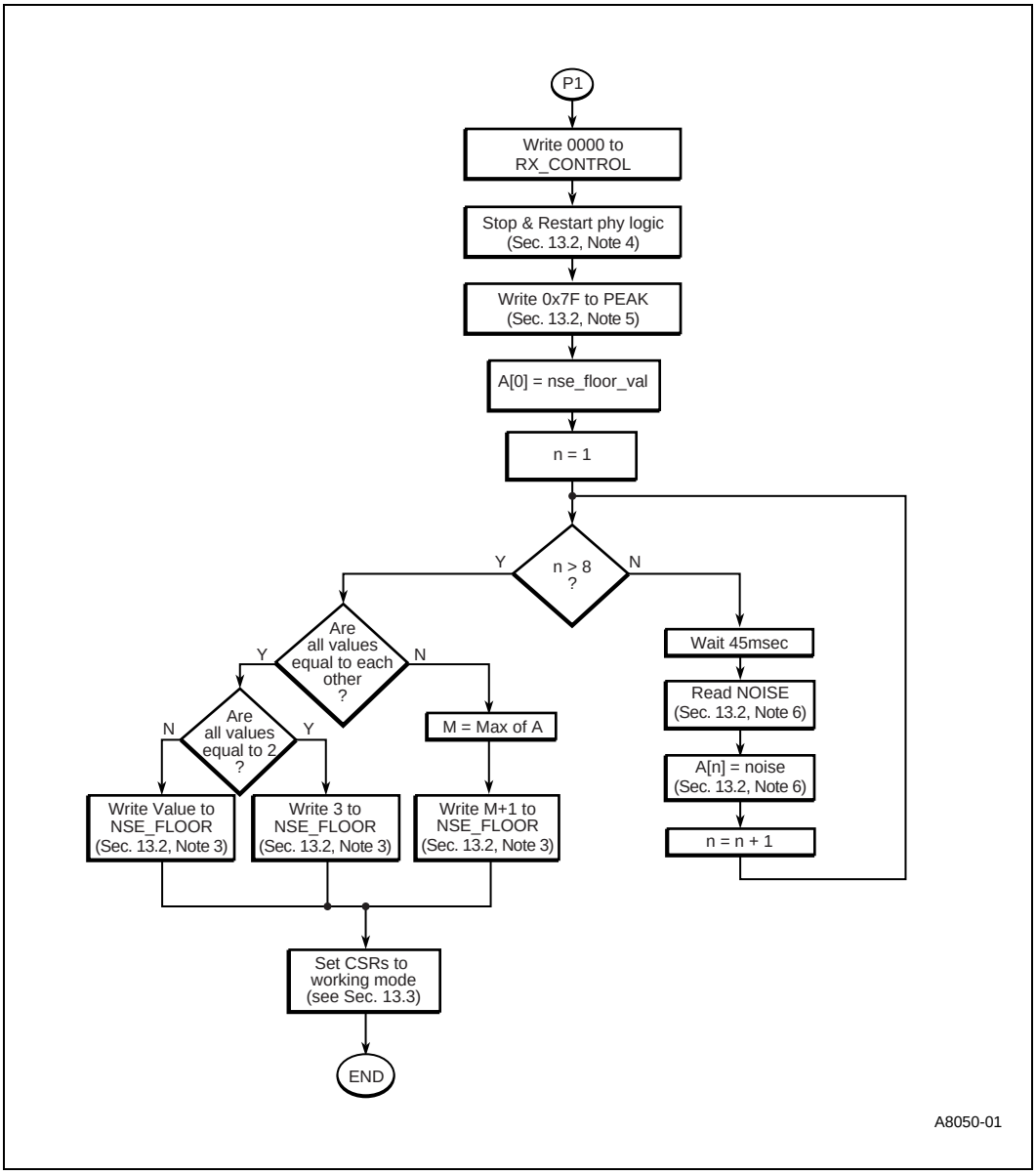


Figure 11. Initialization Algorithm (Part 2)



14.0 Disabling the 82562EH

You may want to disable the 82562EH in some ICH2 applications. Figure 12 shows a hardware disable implementation.

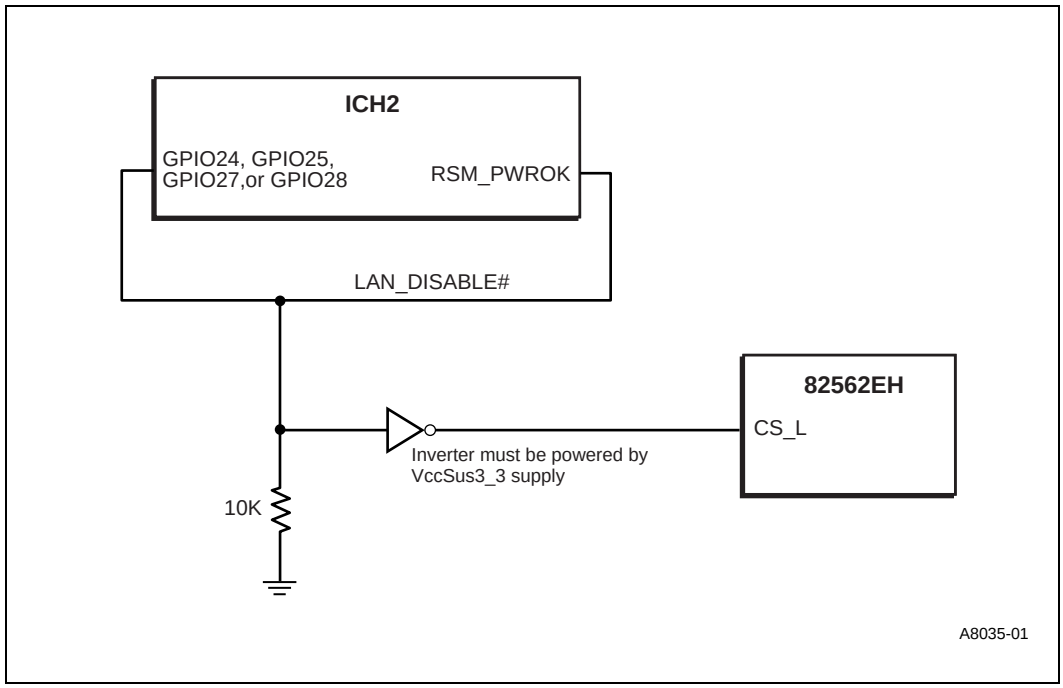
When CS_L is pulled high it causes the following to happen:

1. Floats the LAN Connect interface, which effectively hides and disables the LAN function in the PC configuration space.
2. Lowest 82562EH power consumption mode. All clocks are stopped.

To enable 82562EH after the disable:

1. Pull CS_L low.
2. Perform a hardware reset.

Figure 12. Disabling the 82562EH



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