MAC Interface Design Guide — Interfacing Intel® Ethernet Transceivers to Intel® Controllers

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN51*.

Application Note

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1.0 General Description

This application note describes operation of the Intel 82596 LAN controller with Intel Ethernet transceivers for IEEE 802.3 10BASE-T and AUI connections. The 82596 can be used with a variety of Intel devices including the LXT901, LXT905, and LXT907. The 82596 performs the Medium Access Control (MAC) functions, while the Intel transceivers perform the Physical (PHY) layer functions of Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link integrity testing, reversed polarity detection and correction, and AUI driving and receiving. This application note details the transceiver-to-controller interface. It also describes the Carrier Sense mode settings required for compatibility between the Intel LXT905 transceiver and the Intel 82596 LAN controller.

2.0 Features

- Integrated filters - No external filters required
- Integrated Manchester encoders/decoders
- 10BASE-T compliant transceivers
- AUI transceivers
- Automatic /Manual AUI/RJ45 Selection
- Automatic polarity correction
- SQE enable/disable
- Integrated LED drivers
- Full-duplex capability

Consult individual product data sheets for specific product feature sets.

3.0 Application Overview

3.1 CSMA/CD or Full-Duplex Ethernet

The Intel transceivers listed above support full-duplex operation, a feature that makes these transceivers an excellent choice for use with the Intel 82596. The 82596 has two link management algorithms, one of which is Carrier Sense Multiple Access with Collision Detection (CSMA/CD) for compliance with the IEEE 802.3 standard. In CSMA/CD operation, the presence of activity on the serial link delays any data transmission until the link is clear. Collisions can be detected internally or externally to the 82596. With external collision detection, the 82596 is notified of collisions by the COL output of the Intel transceiver.

In addition to CSMA/CD, the 82596 is capable of full-duplex communication. In full-duplex operation, the 82596 uses the $\overline{RTS}$ output to enable data transmission through the TEN input of a Intel transceiver. In order for Intel transceivers to operate in full-duplex mode, the transceiver collision detect circuits must be disabled. Collision detection disable is performed through the LEDC pin on the transceiver. In half-duplex operation (for CSMA/CD), the LEDC pin is an output for driving a collision indicator LED. Externally tying the LEDC pin Low disables internal twisted-pair loopback and collision detect, enabling full-duplex communication.

Full-duplex operation effectively doubles the bandwidth of an Ethernet connection, without any change in the physical media.

3.2 Transceiver to Controller Interface

Intel transceivers use an 8-pin interface to connect with LAN controllers. Table 1 describes the connections between Intel transceivers and the 82596. Note that the CD output from the transceiver is not used with the 82596 controller.

Table 1. Transceiver Pin Descriptions and 82596 Connections

Transceiver Pin Name	I/O	Signal Name	Signal Description	82596 Pin Name
TXD	I	Transmit Data	Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.	TXD
TEN	I	Transmit Enable	Enables data transmission and starts the watchdog timer. Synchronous to TCLK.	$\overline{RTS}$
TCLK	O	Transmit Clock	10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.	$\overline{TXC}$
RCLK	O	Receive Clock	Recovered 10 MHz clock which is synchronous to the received data and connected directly to the receive clock input of the controller.	$\overline{RXC}$
RXD	O	Receive Data	Output signal connected directly to the receive data input of the controller.	RXD
1. Loopback is an optional connection. Both devices recognize Loopback, but it is not necessary for normal operation.				

Table 1. Transceiver Pin Descriptions and 82596 Connections (Continued)

Transceiver Pin Name	I/O	Signal Name	Signal Description	82596 Pin Name
CD	O	Carrier Detect	Output to notify the controller of activity on the network. **Do not connect** when using an Intel 82596 with an LXT905.	$\overline{CRS}$
COL	O	Collision Detect	Output which drives the collision detect input of the controller.	$\overline{CDT}$
LBK	I	Loopback	Enables internal loopback mode.[1]	$\overline{LPBK}$
1. Loopback is an optional connection. Both devices recognize Loopback, but it is not necessary for normal operation.				

3.2.1 Carrier Sense Mode Settings

The Intel 82596 LAN controller offers two modes for the carrier sense function: Internal and External. Mode compatibility is listed in Table 2. The LXT901 and LXT907 may be used with either mode. The LXT905 may be used with the Internal mode only.

In the Internal Carrier Sense mode the external carrier sense on the 82596 $\overline{CRS}$ pin is ignored. Instead, the presence of the receive clock is interpreted as Carrier Sense active. The Carrier Detect output from the transceiver is not required and should not be connected to the controller. To set the 82596 controller to the Internal Carrier Sense mode, use the configure command to set the 82596 configuration parameter CARRIER SENSE SOURCE (Byte 9, Bit 3).

In External Carrier Sense mode the controller looks at the Carrier Detect signal from the transceiver. In the LXT905, the delay between the end-of-frame and the de-assertion of Carrier Detect may cause the 82596 to mis-read several bits. Selecting the Internal Carrier Sense mode eliminates this condition.

Table 2. Carrier Sense Mode Compatibility

Transceiver	Internal	External
LXT901	Yes	Yes
LXT905	Yes	No
LXT907	Yes	Yes