AB-66

APPLICATION BRIEF

Resolving Bus Contention When Interfacing the Intel386™ EX Embedded Processor with Intel Flash

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CONTENTS

FIGURES

REVISION HISTORY

Number	Description
-001	Original version

1.0 INTRODUCTION

Examining the worst-case timing relations for interfacing the Intel386™ EX embedded processor with flash indicates bus contention on a memory read followed by a memory write. However, the Intel386 EX embedded processor specification t_{50} resolves this issue and guarantees no bus contention if the flash data float time (t_{GHQZ}) is ≤ t_{50}. This document explains why there is no contention when interfacing with Intel Flash.

2.0 READ FOLLOWED BY WRITE TIMING ANALYSIS

Figure 1 shows the timing for a read followed by a write, along with the signals that must be evaluated to determine if bus contention exists. A full timing diagram is presented in Appendix A. To avoid bus contention, the flash memory must stop driving "read data" on the bus before the Intel386 EX embedded processor starts driving "write data" on the bus.

Controller AC timings are specified with a minimum and a maximum value. For example, at 5V V_{CC}, 25 MHz the RD# valid delay, t_{10a}, is specified as 4 ns minimum and 22 ns maximum. These minimum and maximum specifications are provided to account for variations in temperature, voltage, and processing.

Using these specifications, a timing analysis shows that contention occurs when RD# is deasserted late, i.e., 22 ns maximum delay, and D[15:0] is driven early, i.e., 4 ns minimum delay. However spec t_{50} guarantees by design that there is no contention. This is guaranteed because if RD# goes high late, D[15:0] will also be driven late as the logic delays of t_{10a} and t_{12} track each other across temperature, voltage, and processing variations. Since t_{10a} and t_{12} track each other, they are separated by a CLK2 (each are referenced to a rising clock edge, separated by a CLK2—20 ns at 25 MHz.). Therefore, the data float time of the flash memory must be less than CLK2, as specified by t_{50}.

The following example shows the calculation for data float without using t_{50} which yields an unrealistic float time requirement for flash memory. The example then shows the correct calculation using the Intel386 EX embedded processor specification of t_{50}.

At 5V V_{CC}:

t_{10a} = [4, 22] = RD#, WR# Valid Delay

t_{12} = [4, 23] = D[15:0] Write Data Valid Delay

t_{GHQZ} = Flash Data Float Time (20 ns for 28F400BV)

Analysis without t_{50} (incorrect):

$t_{GHQZ} = CLK2 - t_{10a}(max) + t_{12}(min)$

t_{GHQZ} = 20 ns – 22 + 4 = 2 ns.

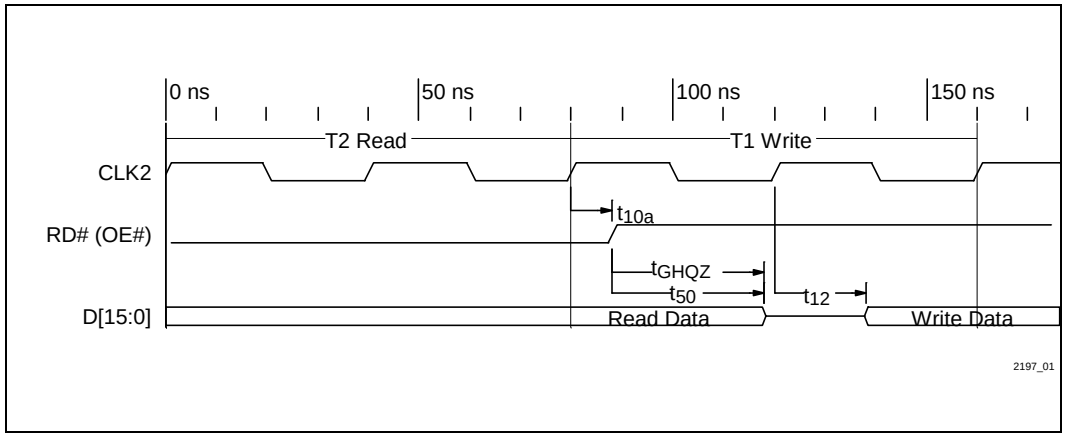


Figure 1. Interfacing the Intel386™ EX Embedded Processor with Intel Flash

Since the flash memory data float time, t_{GHQZ}, is longer than 2 ns, this would indicate a transceiver would be necessary to avoid bus contention. However, as previously described, this analysis is incorrect because t_{50} guarantees no contention, if $t_{GHQZ} \leq t_{50}$.

Analysis using t_{50} (correct):

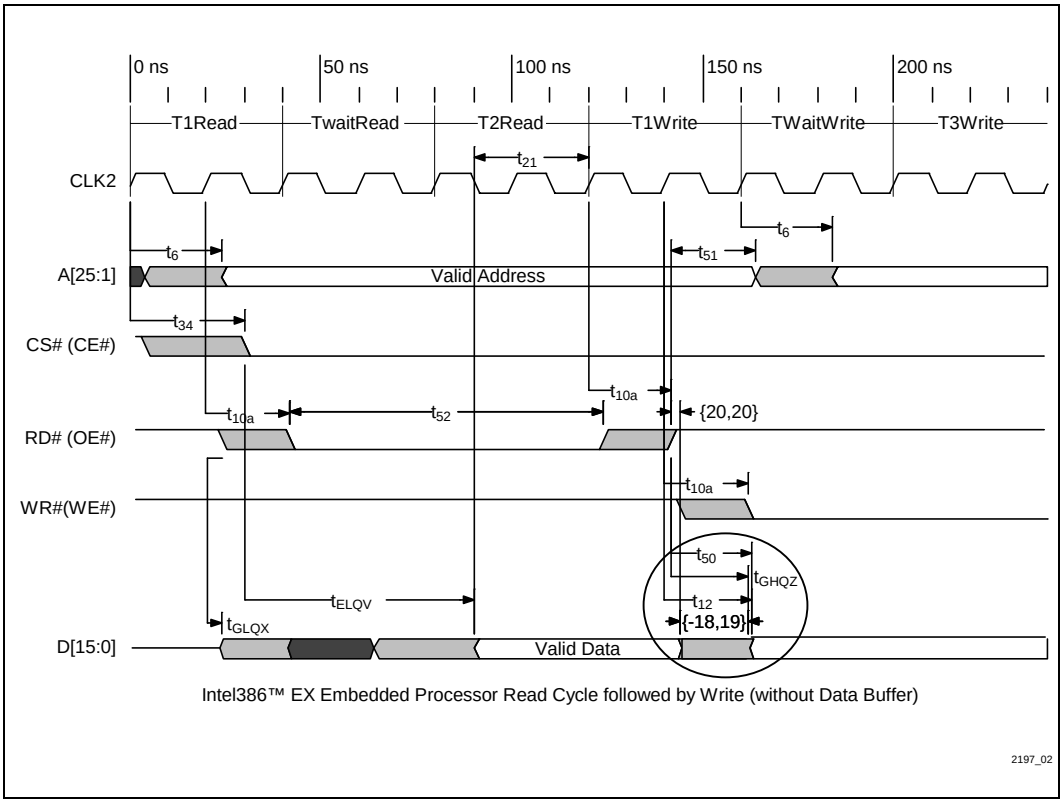
$t_{GHQZ} \leq t_{50}$ = CLK2 = 20 ns @ 25 MHz.

3.0 CONCLUSION

The Intel386 EX embedded processor specification t_{50} guarantees no bus contention, if $t_{GHQZ} \leq t_{50}$. The Intel386 EX embedded processor and Intel Flash can be interfaced with no glue logic.

APPENDIX A
ADDITIONAL INFORMATION

Figure 2 shows all timing parameters for interfacing the Intel386™ EX embedded processor with flash. Note t_{10a} and t_{12} **should not** be used to determine bus contention; t_{50} **should** be used to determine bus contention.



Intel386™ EX Embedded Processor Read Cycle followed by Write (without Data Buffer)

Figure 2. Interfacing the Intel386™ EX Embedded Processor with Intel Flash