Design Considerations for Migrating Intel386™ and Intel486™ Processor Embedded Systems to the Pentium® Processor

Application Note

August 1998

Order Number: 273192-001

Application Note

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1.0 Introduction

Intel® architecture (IA) processors, from the Intel386™ processor to the Pentium® processor, provide a compelling option for embedded designs. With strong tools support, a robust development environment, and a clearly defined upgrade path, IA is being used in a variety of embedded systems, from point-of-sale (POS) terminals and retail kiosks to advanced networking equipment. Pentium processors are enabling high-end embedded product developers to step up to new levels of performance.

The personal computer migrated from the 8-MHz ISA bus architecture in the 80386 microprocessor generation to the 33-MHz VL-bus architecture in the 80486 microprocessor generation. In just a short time, designers adopted the 33- and 66-MHz PCI bus architecture to enable the latest Pentium processor PCs.

Embedded system design differs slightly from classic PC system design. Many chip vendors introduced supporting chipsets for 80386 and 80486 microprocessors, that integrated peripherals onto the bus controller and the memory controller. Embedded systems based on these chipsets were easy to implement. However, these designs were often unique and did not possess a smooth upgrade path.

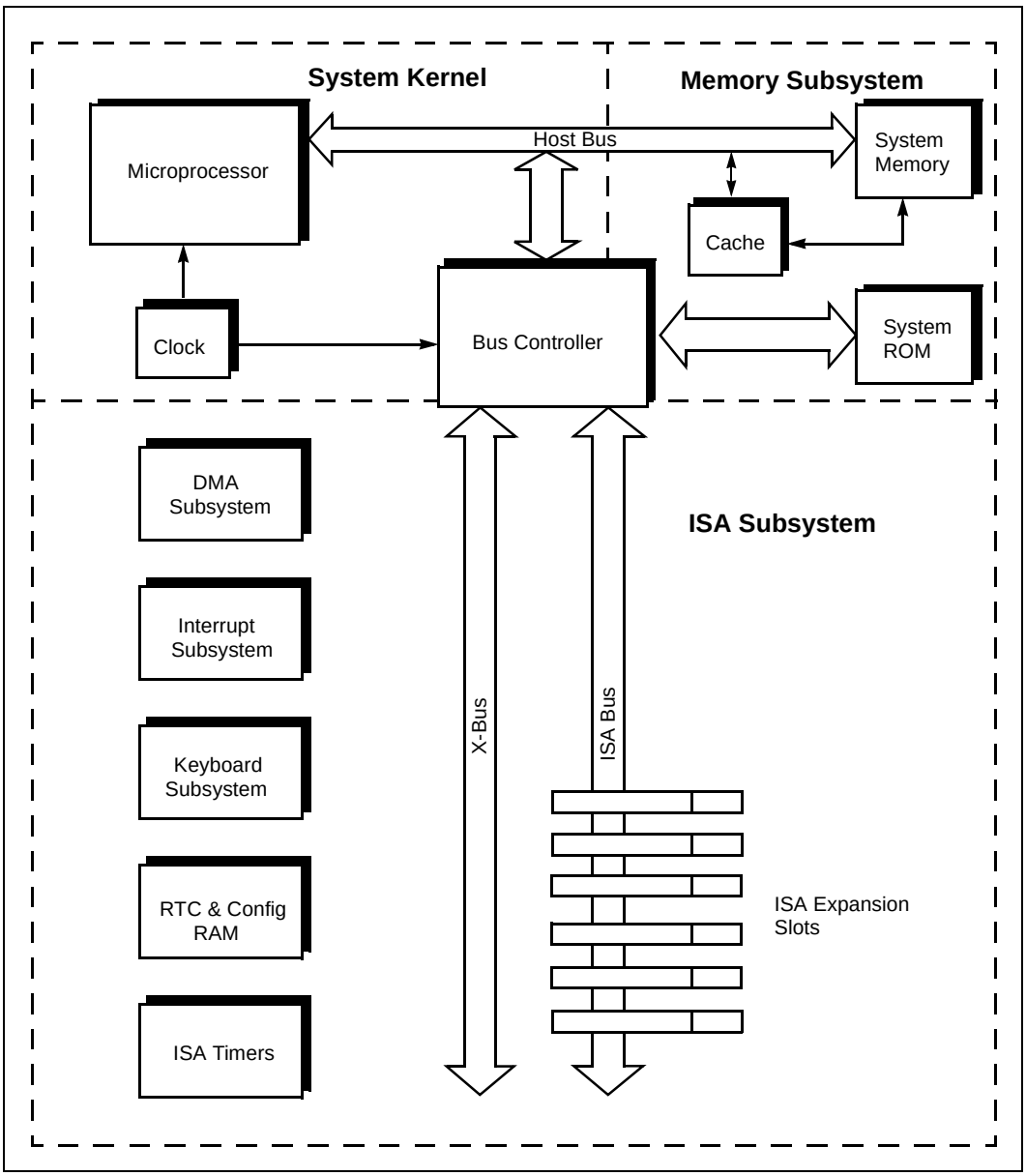
This application note is intended to assist embedded systems designers in migrating from previous 80386 or 80486 processor-based designs to higher performance Pentium processor-based designs. This application note can be used with the following documents: *33 MHz 386 System Design Considerations* (order number 240725), *Intel 430HX PCIset Design Guide* (order number 297467), and application note *AP-479 Pentium® Processor Clock Design* (order number 241574).

This application note discusses the bus technologies and design structures for the earlier 80386 and 80486 microprocessor systems and addresses design considerations for migrating to Pentium processor designs. Software considerations, BIOS, and operating system issues are not discussed.

2.0 Intel386™ Processor System Overview

2.1 Block Diagram

Figure 1. Intel386™ Processor System Block Diagram



2.2 System Kernel

The CPU subsystem consists of the 80386 microprocessor, the ISA bus controller, and other support logic. The primary function of the bus control logic is to provide the basic signals, timing, and protocols necessary for the microprocessor to communicate with the rest of the system.

The bus control logic assists the microprocessor in running bus cycles. There are many bus controllers with integrated peripherals to ease the task of system design.

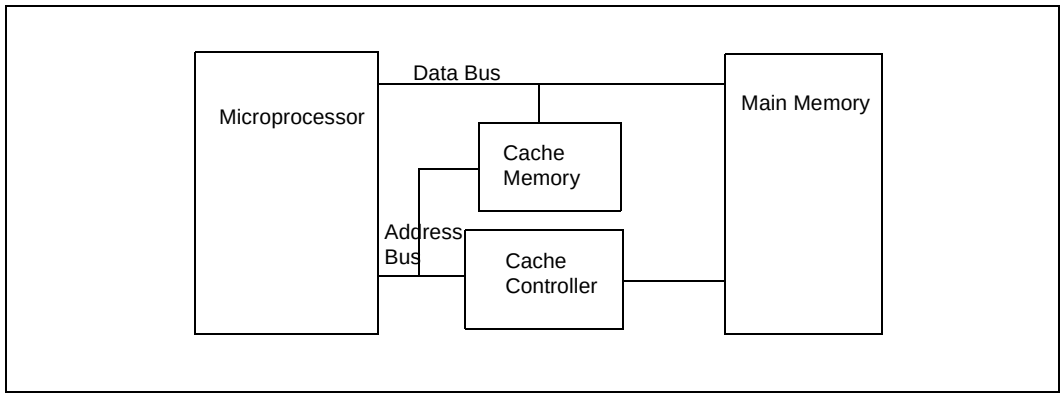
2.3 Memory Subsystem

The memory system consists of the main memory, cache memory, and system ROM. The performance of a system largely depends on the memory performance. The 80386 processor did not contain Level-1 cache; many systems designers used off-chip cache to enhance the performance of these systems. Typically, this cache ranged from 64 Kbytes to 512 Kbytes, and was fast SRAM running at the processor clock speed.

2.3.1 DRAM

DRAM modules are normally connected to the processor bus or host bus through a cache controller. The DRAM used in 80386 processor systems is based on Fast Paged Mode (FPM) memory architecture. However, some bus controllers or later chipsets have an integrated memory controller and can interface directly to the DRAMs.

Figure 2. Intel386™ Processor System Memory Block Diagram



2.3.2 System ROM

The system ROM or BIOS ROM normally occupies the address range from F0000H to FFFFFH. To chip-select the ROM, all upper bits of the address A[31:16] are decoded. Either address FFFFxxxxH or 000FxxxxH chip selects the ROM chip. Address bus lines A[15:0] are not connected to the address decoder but directly to the ROM.

2.4 ISA Bus Subsystem

The Industry Standard Architecture (ISA) bus subsystem consists of the ISA bus and all the devices that reside on it. The ISA bus operation speed ranges from 8 MHz to 8.33 MHz. Both 8- and 16- bit devices are supported. Some common functions that use the ISA bus include direct memory access (DMA), keyboard, real-time clock, and non-volatile configuration RAM (used for BIOS).

2.4.1 Address Decoding Logic

Because there are many devices that utilize the ISA bus, each ISA device must have a unique address range to prevent bus and device contention. Address decoding logic must be implemented for this purpose. Only higher-order address bits LA[23:17] of the ISA bus are decoded. If the address is within a device's designated address range, the address decoder chip selects the device. The selected device then decodes the lower-order address of the ISA bus to determine which internal registers are being accessed. Due to the possible address conflict from using the same address range on add-in cards, many designers normally have two to three address range options with jumpers. This issue does not normally surface on an embedded PC because add-in cards are not supported; the required functionality is designed into the base board.

ISA I/O addresses range from 0100H through 03FFH. To achieve cost reduction, many ISA I/O devices perform an incomplete decode. The address decoder typically decodes A[9:5] to acknowledge the addressed I/O space. If it is within region, A[4:0] is examined for particular access locations. Although implemented at lower cost, this method risks bus contention problems and renders some I/O address ranges unusable.

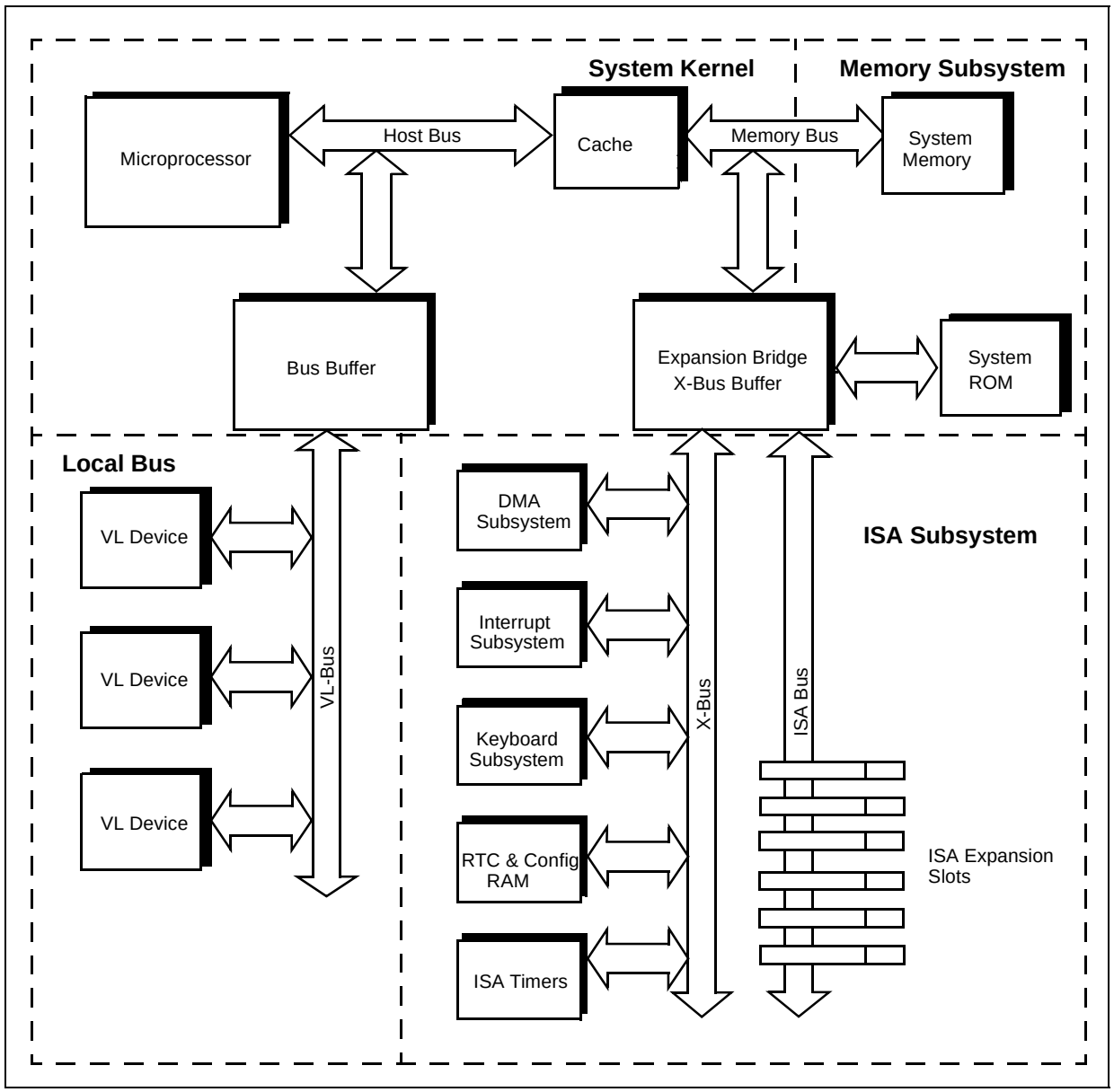
2.4.2 X-Bus

The X-bus is a buffered version of an ISA bus in which the system peripherals such as keyboard, mouse, and DMA controllers are connected. Because some integrated 80386 chipsets in embedded systems have integrated peripherals such as the keyboard, DMA controller, and UARTs, these chipsets provide a direct interface to the supported peripherals. Other embedded system designs may place a Super I/O* extension chip on the ISA bus to provide interfaces to various peripherals.

3.0 Intel486™ Processor System Overview

3.1 Block Diagram

Figure 3. Intel486™ Processor Block Diagram



3.2 CPU Subsystem

Intel486™ processor subsystem designs consist of the microprocessor, bus controller, and other support logic. The system design is not much different from the typical 80386 processor system. 80486 chipsets with integrated solutions provide the same functionality as the 80386 processor chipsets, but with a noticeable performance boost in typical applications. These integrated solutions generally do not provide a smooth upgrade path.

Figure 3 shows a typical 80486 processor system adapted from a standard PC design. Note the local bus buffer on the host bus. The local bus concept was introduced to speed up data fetches. This is particularly useful for devices that need a high data transfer rate, such as video graphics memory. This is also known as VESA local bus.

The local bus buffer is connected directly to the processor's bus structure. This buffer drives all the local bus signals, permitting fanout to other local bus devices. This method supports more than one local bus device, but gives only one load to the local bus, preventing congestion at the processor bus.

One example of this design is to connect to the local bus a cacheable video memory device that supports burst mode. When a 80486 processor performs a read burst transfer (zero wait state) at a bus speed of 33 MHz, the data can be transferred at a rate of 132 Mbytes per second.

3.3 Memory and ISA Subsystem

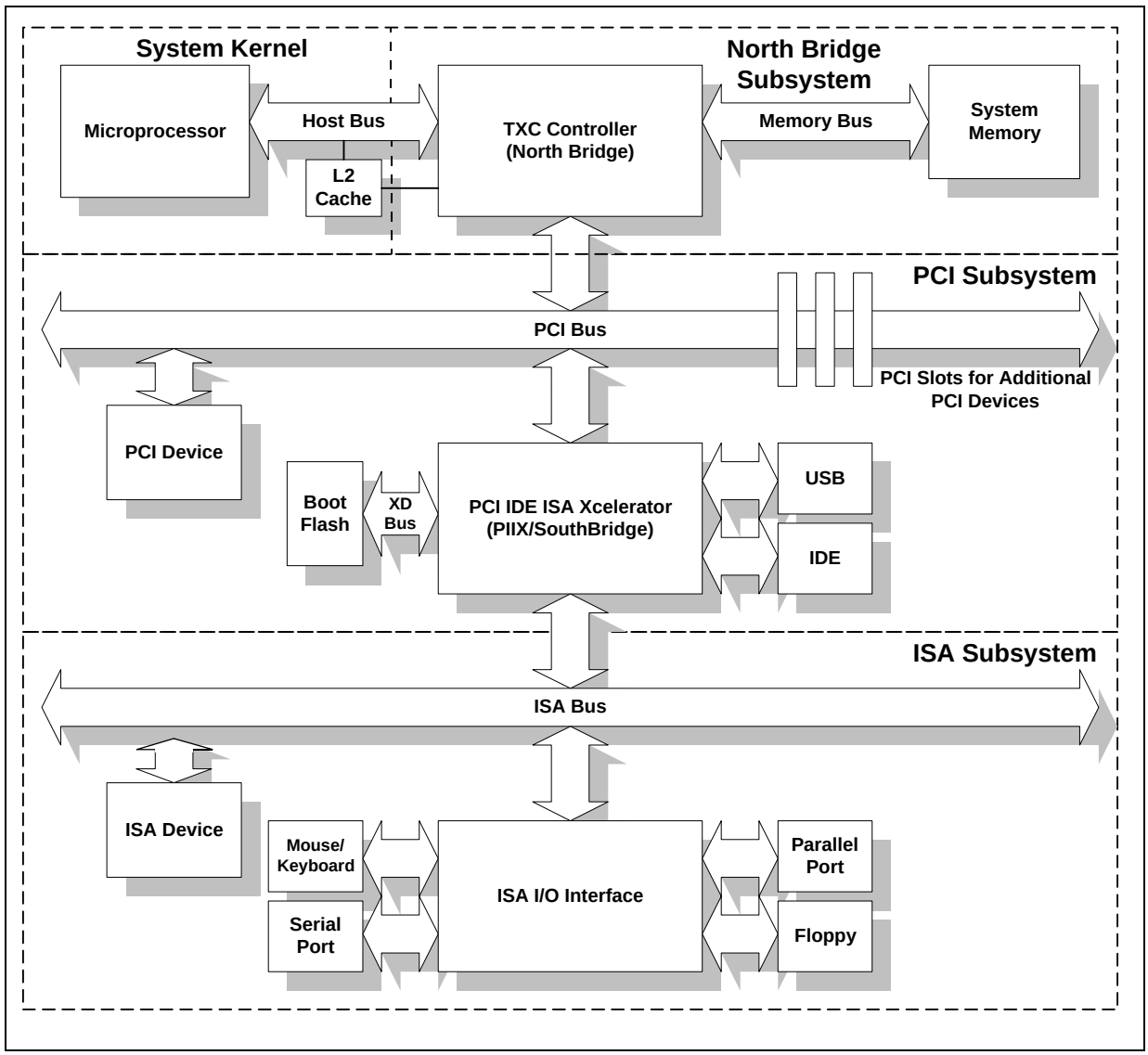
System memory DRAMs can be integrated in the chipsets or on the host bus to connect to the memory controller.

ISA bus design is the same as in 80386 processor systems. All devices located on this bus must have address decoding logic.

4.0 Pentium® Processor System Overview

4.1 Block Diagram

Figure 4. Pentium® Processor System Block Diagram



The introduction of high-performance Pentium processors into embedded designs enables new levels of system performance, but presents a new challenge: as processor performance increases, system performance bottlenecks can occur due to slow system buses. The PCI bus was introduced in Pentium processor-based systems to provide a high-speed communication path from the processor to other devices. The ISA bus remains to provide legacy support and is a low-cost solution for slower devices that do not require PCI performance.

4.2 Pentium® Processor Design Considerations

The Pentium processor at 100/133/166 MHz is a 3.3 V processor that operates at 100, 133 and 166 MHz core speeds (66 MHz external bus speeds). These processors are unified plane processors that use 3.3 V for all V_{CC} pins.

The Pentium processor with MMX™ technology at 166/200 MHz is the newest addition to the embedded Pentium processor family. These processors provide several architectural enhancements. The internal data and code cache sizes have each been doubled from 8 Kbytes to 16 Kbytes, the branch prediction algorithm has been improved, and support for Intel MMX technology has been added. MMX technology is an extension to the Intel architecture (IA) instruction set that adds 57 new opcodes and a new MMX register set.

In the 80486 device, the cache was four-way set associative. The Pentium processors and Pentium processors with MMX technology are two-way set associative.

The Pentium processor with MMX technology operates at core frequencies of 166 and 200 MHz with a 66 MHz external bus. The Pentium processor with MMX technology uses 2.8 V for its internal core, while its peripheral I/O operates at 3.3 V (to provide full compatibility with existing chipset and SRAM). It is pin, package, and functionally compatible with the Pentium processor at 100/133/166 MHz and is operating system transparent.

Table 1. Differences between Pentium® Processors and Pentium Processors with MMX™ Technology

	Pentium® Processor	Pentium® Processor with MMX™ Technology
Core Frequency	100, 133, 166	200
Bus Frequency	66	66
Frequency Ratio	1/2, 2/3, 2/5	1/3
Clock Level	3.3 V or 5 V	3.3 V
Core Supply	3.135 V – 3.60 V	2.7 V – 2.9 V
I/O Supply	3.135 V – 3.60 V	3.135 V – 3.60 V

4.2.1 Pinout Considerations

V_{CC2}, V_{CC3}: The internal bus logic on the Pentium processor with MMX technology is isolated from the core logic so that the core can run at a lower voltage (2.8 V), enabling higher core frequencies while lowering overall power consumption. The bus logic remains at 3.3 V to remain compatible with existing chipsets and cache SRAM. The voltage for the core logic is supplied through the V_{CC2} pins and the voltage for the bus logic is supplied through the V_{CC3} pins. The motherboard design therefore splits the processor power plane into a separate 2.8 V core voltage island and a 3.3 V I/O voltage island.

VCC2DET#: This is a new signal on the Pentium processor with MMX technology that indicates to the system that the processor installed in the processor socket uses an isolated 2.8 V core supply on the VCC2 pins. This pin is internally connected to ground on the Pentium processor with MMX technology. On Pentium processors at 100/133/166 MHz, this pin is defined as INC (Internal No Connect). This signal is pulled high externally or left unconnected.

- **BF[1-0]**: The bus fraction selection pins determine the bus-to-core frequency ratio. The BF pins are sampled by the processor at RESET, and are not sampled by the processor again until another cold-boot (1 ms) assertion of RESET. The signal on the BF pins is not an indication of the bus speed—only the ratio of the processor core with respect to the bus.
- **CLK, PICCLK**: The clock inputs to the processor are driven by an appropriate 3.3 V clock driver. Driving the clock at 3.3 V is also compatible with the Pentium processor at 100/133/166 MHz.

Note: The CLK and PICCLK buffers on the Pentium processor with MMX technology are not 5 V tolerant.

For Pentium processor clock design techniques, refer to application note *AP-479 Pentium® Processor Clock Design* (order number 241574).

4.3 Northbridge Subsystem

4.3.1 TXC System Controller

The microprocessor bus is isolated from other devices by the TXC system controller (Nortbridge), which reduces host bus traffic. 80386 and 80486 systems share the host bus with other controllers, which can create congestion in the host bus and reduce the available processor bandwidth and system performance. The host interface of the TXC supports 50 MHz, 60 MHz, and 66 MHz bus speeds. The TXC also supports the Pentium processor's available dual processing mode. The TXC supports the Pentium processor with a full 64-bit data bus, 32-bit address bus, and associated internal write-back cache logic. Host bus addresses are decoded by the TXC for accesses to main memory, PCI memory, and PCI I/O. The TXC also supports the Pentium processor's pipelined addressing capability.

4.3.1.1 PCI Interface

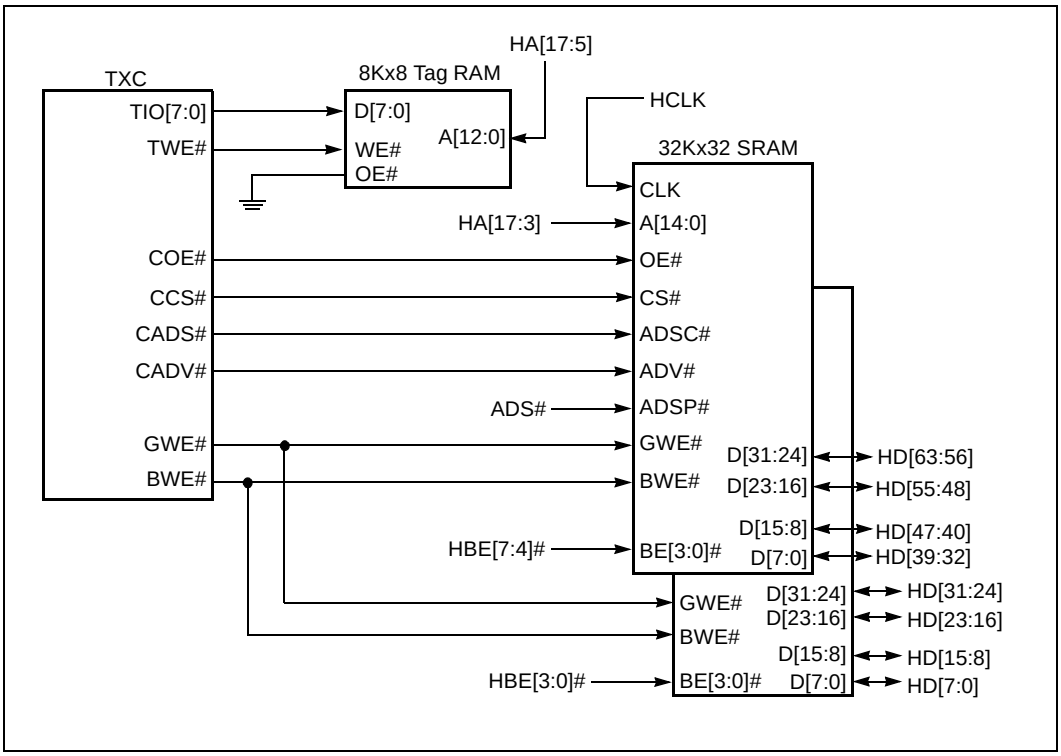
The TXC implements a high-performance interface to the PCI local bus, taking full advantage of the high bandwidth and low latency of the PCI bus. The integrated bus arbiter supports up to five PCI masters, including four general purpose PCI masters and an optimized arbitration for the PCI-to-ISA bridge. The PCI-to-ISA bridge arbitration dynamically allocates bandwidth to the PIIX to optimize system latencies and provide superior Universal Serial Bus (USB) performance.

4.3.1.2 Integrated Cache Controller

The TXC integrates a high performance write-back level-2 cache controller using internal/external tags and provides a full level-1 and level-2 cache coherency mechanism. The level-2 cache is direct mapped and non-sectored, and supports a write-back cache policy. Cache lines are not allocated on write misses.

The level-2 cache can be configured to support either a 256-Kbyte or 512-Kbyte cache using synchronous pipelined burst SRAMs. 64-Mbytes cacheability coverage is obtained with 8Kx8 standard SRAM to store the tags for 256-Kbyte configuration. For the 512-Kbyte configurations, a 16Kx8 standard SRAM is used to store the tags and the valid bits for 64-Mbyte cacheability. Only main memory controlled by the TXC DRAM interface is cached. PCI memory is not cached. Figure 5 shows a typical connection for 256 Kbyte cache with 64 Mbyte cacheability.

Figure 5. 256 Kbyte Level-2 Cache with PBSRAM (64 Mbyte Cacheability)



4.3.1.3 DRAM Interface

The TXC implements a DRAM controller that supports a 64-bit memory array and main memory sizes from 4 Mbytes to 512 Mbytes (430HX) and 4 Mbytes to 256 Mbytes (430TX). The TXC generates all control signals (such as RAS#, CAS#, WE# using MWE#) and multiplexed addresses for the DRAM array. The address and data flows through the TXC for all DRAM accesses.

Seven Programmable Attribute Map (PAM) registers are used to specify cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbyte. Each PAM register defines a specific address area, enabling the system to selectively mark specific memory ranges as cacheable, read-only, write-only, read/write, or disabled. When a memory range is disabled, all CPU accesses to that range are automatically forwarded to the PCI bus.

The TXC also supports one of two memory “holes”, either from 512 Kbytes to 640 Kbytes or from 15 Mbytes to 16 Mbytes in main memory. Accesses to the memory holes are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control register. All other memory from 1 Mbyte to 512 Mbytes is read/write and is cacheable. This is necessary to support some legacy applications that use memory I/O accesses, such as video capture devices that need fast memory I/O access.

4.3.1.4 Clock Generation

Clock generation and distribution is important in high-speed design. The skew between any two HCLK (Host clock) loads must be less than or equal to 1 ns. The skew between HCLK at the pin of the TXC and the pin of the CPU must be less than or equal to 0.3 ns. The skew between any two PCLK (PCI Clock, HCLK/2) loads must be less than or equal to 2 ns, the requirement of the PCI Rev 2.0 specification. For HCLK to PCLK ratios of 2-to-1, the rising edge of PCLKIN must be within 1 to 6 ns of the rising edge of HCLKIN, with HCLK leading PCLK.

4.3.2 PCI Bus

The PCI (Peripheral Component Interconnect) bus specification was developed to establish an industry standard, high-performance local bus architecture that is low-cost and allows product differentiation. It was first introduced in 1992. Revision 2.1 of the PCI Local Bus Specification has been available since June 1995.

With the PCI bus, devices that require fast access to system memory or to other devices can run at a high bus speed, up to 66 MHz. Also, with PCI system design, the PCI bus controller isolates other PCI devices from the processor host bus, preventing bus congestion and providing processor upgradability.

4.3.2.1 PCI Bus Features

The PCI bus logically supports 32 physical PCI devices. However, in a typical implementation at 33 MHz, it can support up to 10 electrical loads.

Each PCI device may support up to eight PCI functions. With PCI-to-PCI bridges, a system can have up to 256 PCI buses.

PCI bus speed is specified from 0 to 33 MHz and 66 MHz operation. The bus width can be implemented as either 32 bits or 64 bits wide. When a PCI bus is running at 33 MHz, all the PCI devices on this bus should be configured and able to operate at the same frequency. All read and write transfers on the PCI bus are burst transfers. With four transfers at a time at 33 MHz, the PCI bus supports up to 132 Mbytes/sec. PCI has a maximum transfer rate of 528 Mbytes/sec at 66 MHz and a 64-bit bus width.

One major difference between the PCI and ISA buses is that PCI devices are software-configurable. At initialization, the PCI devices may be configured through their configuration registers in the configuration address space. This differs from the ISA bus, where hard-wired address decoders are used to decode ISA device addresses.

Note: The PCI connectors are considered an electrical load as well. A PCI device connected to the connector appears as two electrical loads on the bus.

4.3.2.2 PCI Bus Clock

All activities on the PCI bus need to be synchronized by the PCI clock. The frequency of the CLK signal may range from 0 to 33 MHz. Operation at 66 MHz is also supported with proper design and initialization. All inputs to PCI devices are sampled and all PCI timing parameters are specified with respect to the rising edge of the CLK signal.

4.3.2.3 PCI Pin Signals

Table 2 gives a brief description of all signals available on the PCI bus and device.

Table 2. PCI Signal Description (Sheet 1 of 2)

Signals	Type(1)	Description
CLK	I	Clock signal providing timing for all PCI transactions and bus arbitration.
RST#	I	Reset signal to initialize all PCI configuration registers, master/target state machines and output drivers.
AD[31:0]	T/S	Time multiplexed address/data bus.
C/BE[3:0]#	T/S	Command/Byte Enable bus. Defines transaction type.
PAR	T/S	Driven by initiator/addressed target after write/read to ensure even parity across AD[31:0] and C/BE[3:0]#.
FRAME#	S/T/S	Driven by initiator indicating the start and the duration of a transaction.
TRDY#	S/T/S	Target Ready driven by target when it is ready to complete the current data transfer.
IRDY#	S/T/S	Initiator Ready driven by initiator when it is ready to drive/accept data onto/ from the data bus.
STOP#	S/T/S	Asserted by target when it wishes to stop transaction half way during the data phase.
LOCK#	S/T/S	Asserted by initiator to lock the currently address memory target during an atomic transaction series.
IDSEL	IN	Input to the PCI device as a chip select during initialization to access the device's configuration registers.
DEVSEL#	S/T/S	Device Select asserted by a target when it positively decodes an address range.
REQ#	T/S	Bus request signal for PCI bus arbitration.
GNT#	T/S	Bus grant signal during PCI bus arbitration.
PERR#	S/T/S	Data Parity error signal asserted by a PCI device during any data parity error detection.
SERR#	O/D	System Error signal asserted by a PCI device to report address parity error, special cycle data parity error and catastrophic error.
SBO#	IN or OUT	Snoop Back Off asserted by the bridge when PCI memory access is about to read/update stale information in memory.
SDONE	IN or OUT	Snoop Done asserted by the bridge when the snoop has been completed.
AD[63:32]	T/S	Upper address and data bus for 64-bit extension.
C/BE[7:4]#	T/S	Byte Enables for 64-bit extension.
REQ64#	S/T/S	Request 64-bit transfer generated by initiator to indicate 64-bit transaction.

NOTE:
1. The signal types are defined as follows:
   I: Input only signal
   O: Output active driver
   T/S: Three-state bi-directional I/O pin
   S/T/S: Sustained three-state, active low and driven by one and only one agent at a time. Must be driven high for at least one clock before float. Pullup by the central resource is needed to sustain inactive state until driven by another agent.
   O/D: Open Drain allows multiple devices to share as a wired-OR. Pull-up by the central resource is needed to sustain inactive state until driven by another agent.

Table 2. PCI Signal Description (Sheet 2 of 2)

Signals	Type(1)	Description
ACK64#	S/T/S	Acknowledge 64-bit transfer generated by address target in response to a REQ64#.
PAR64	T/S	Parity for the upper doubleword associated with AD[63:32] and C/BE[7:4]#.
TCK	IN	Test Clock used to clock state information and data into and out of the device during boundary scan.
TDI	IN	Test Input to shift data and instructions into the Test Access Port in a serial bit stream.
TDO	OUT	Test Output used to shift data out of the Test Access Port in a serial bit stream.
TMS	IN	Test Mode Select used to control the state of the Test Access Port controller.
TRST#	IN	Test Reset used to force the Test Access Port controller into an initialized state.
INTA#	O/D	Interrupt request line.
INTB#	O/D	Interrupt request line.
INTC#	O/D	Interrupt request line.
INTD#	O/D	Interrupt request line.

NOTE:
1. The signal types are defined as follows:
   I: Input only signal
   O: Output active driver
   T/S: Three-state bi-directional I/O pin
   S/T/S: Sustained three-state, active low and driven by one and only one agent at a time. Must be driven high for at least one clock before float. Pullup by the central resource is needed to sustain inactive state until driven by another agent.
   O/D: Open Drain allows multiple devices to share as a wired-OR. Pull-up by the central resource is needed to sustain inactive state until driven by another agent.

4.3.2.4 PCI Subsystem Design Considerations

During initialization or configuration, software executed by the processor instructs the bridge to configure or define address ranges to particular PCI devices. Before the address is defined, IDSEL (Initialization Device Select) is asserted. Each PCI device has a unique IDSEL signal. The device that samples its IDSEL asserted is the target device to be configured or initialized.

One easy way to implement the IDSEL signals on the system board is to use the upper 21 address lines, AD[31:11]. These lines are not used during the address phase of a type 0 configuration access. Each address line can be used as a unique IDSEL signal to a particular PCI device.

For 33 MHz PCI implementation, the minimum CLK cycle time is 30 ns. For 66 MHz PCI implementation, the minimum CLK cycle time is 15 to 30 ns. CLK skew between any two devices on the PCI bus must be less than 2 ns for 33 MHz and 1 ns for 66 MHz implementation. PCI CLK is delivered to all components with at least 12 ns of high/low time for 33 MHz and 6 ns for 66 MHz operation.

PCI supports either 5 V or 3.3 V component technology. A 5 V system is designed to work only in a 5 V signaling environment, and vice versa. At 5 V signaling, peak-to-peak CLK swing is at least 2 V (0.4 V to 2.4 V). At 3.3 V signaling, peak-to-peak CLK swing is at least 0.4 V_{CC} (0.2 V_{CC} to 0.6 V_{CC}). All PCI bus signals must be driven by compliant components.

The designer must make sure both edges of RST# at reset are monotonic through the switching range. Prior to RST# deassertion, power must be stable for at least 1 ms and CLK has to be stable for at least 100 µS. If the 5 V or 3.3 V rails go out of tolerance by more than 500 mV, RST# should be asserted within 500 ns. The same case happens when the 5 V supply falls below the 3.3 V rail by more than 300 mV, RST# should be asserted within 100 ns.

For signal pins such as REQ64# and ACK64#, they should be pulled high at all components/slots that are NOT connected to the 64-bit data path, and should never be driven low. Other signals such as FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, and LOCK# are to be pulled up with a resistor of the correct value.

Propagation time (T_{prop}) from any driver to any receiver should be less than or equal to:

$T_{cyc} - (T_{val} + T_{skew} + T_{su})$

This evaluates to:

T_{prop} = 10 ns for T_{cyc} = 30 ns in 33 MHz PCI, and

T_{prop} = 5 ns for T_{cyc} = 15 ns in 66 MHz PCI.

For system designs with PCI connectors, the designer must ensure that all four power rails (+5 V, +3.3 V, +12 V, -12 V) are provided to each PCI connector in the system, as well as GND connections. The 3.3 V pins at each connector are to be bussed together and adequately decoupled even if not delivering power. All other reserved pins should be unconnected and not bussed together.

Note: Utilize 0.1 µF, .01 µF, and .001 µF bypass caps liberally in your design. By spreading different values of bypass caps you achieve best overall noise suppression.

For further information on PCI bus architecture, the latest revision of the *PCI Local Bus Specification* can be obtained from the PCI Special Interest Group. Contact information for the PCI-SIG is contained Section 6.0, “Related Information” on page 20.

4.4 Southbridge Subsystem

The PCI ISA IDE Xcelerator (PIIX), or Southbridge, integrates a PCI-ISA bridge, IDE interface, DMA controllers, and support for USB and other peripherals in a single chip. The PIIX connects the PCI bus with the ISA bus, providing a path for the processor to access ISA devices. The ISA bus structure is similar to the 80386 and 80486 design to provide compatibility with legacy ISA hardware.

When a CPU wishes to access an I/O device located at the ISA bus, it first issues an I/O address aimed at the target device. None of the PCI devices during the PCI transaction decode the I/O address. Using subtractive decoding, the PIIX positively claims the I/O address after a period of time when no other PCI devices respond. The PIIX then broadcasts the I/O address to the ISA bus. The address decoder at the targeted ISA device decodes the I/O address and responds to the processor's request.

The IDE controller is integrated in the PIIX device (in 80386 and 80486 chipsets, the IDE controller was not integrated). Therefore, designers can directly connect hard drives or IDE devices to the PIIX.

More information on the Northbridge and Southbridge can be obtained from the PCIsets datasheets listed in Section 6.0, "Related Information" on page 20.

5.0 Summary

With the higher performance offered by the PCI bus, data transactions can be performed at higher speeds to improve total system performance. When migrating 80386 or 80486 processor systems to the Pentium processor, design engineers should place devices that need high-speed transactions, such as video controllers and network adapters, on the PCI bus. The PCI bus offers proven longevity and upgradability. Many high-speed systems such as the Pentium II processor-based systems use the PCI bus. Existing lower-speed devices such as keyboard, mouse, and Super I/O* extensions can be left on the ISA bus, reducing the cost of redesign. However, the designer must carefully evaluate the needs of the application. Systems that keep the ISA bus as a legacy component may incur a performance penalty.

As technology advances, more embedded applications are migrating to the Pentium processor. Migrating older 80386 or 80486 processor systems is facilitated by the continued support for ISA devices. Designers can focus on the northbridge subsystem and the PCI subsystem design.

6.0 Related Information

Intel offers a variety of information through the World Wide Web at http://www.intel.com.

To order printed Intel literature, contact the nearest Intel Sales Office or call 1-800-548-4725.

Questions regarding the PCI specification or membership in the PCI Special Interest Group may be directed to:

PCI Special Interest Group,
P.O. Box 14070,
Portland, OR 97214
(800)433-5177 (U.S.)
(503)797-4207 (International)
(503)234-6762 (FAX)
URL: http://www.pcisig.com

Table 3. Related Documents

Document Name	Order Number
AP-442 33 MHz 386 System Design Considerations	Intel # 240725
AP-479 Pentium® Processor Clock Design	Intel #241574
AP-579 Pentium® Processor Flexible Motherboard Design Guidelines	Intel #243187
Intel 430HX PCIset Datasheet	Intel #290551
82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator Datasheet	Intel #290550
Intel 430HX PCIset Design Guide	Intel #297467
ISA System Architecture, 3rd Edition, Mindshare	ISBN: 0-201-40996-8
PCI System Architecture, 3rd Edition, Mindshare	ISBN: 0-201-40993-3
PCI Local Bus Specification, Revision 2.1	see http://www.pcisig.com
PCI Compliance Checklist, Revision 2.1	see http://www.pcisig.com