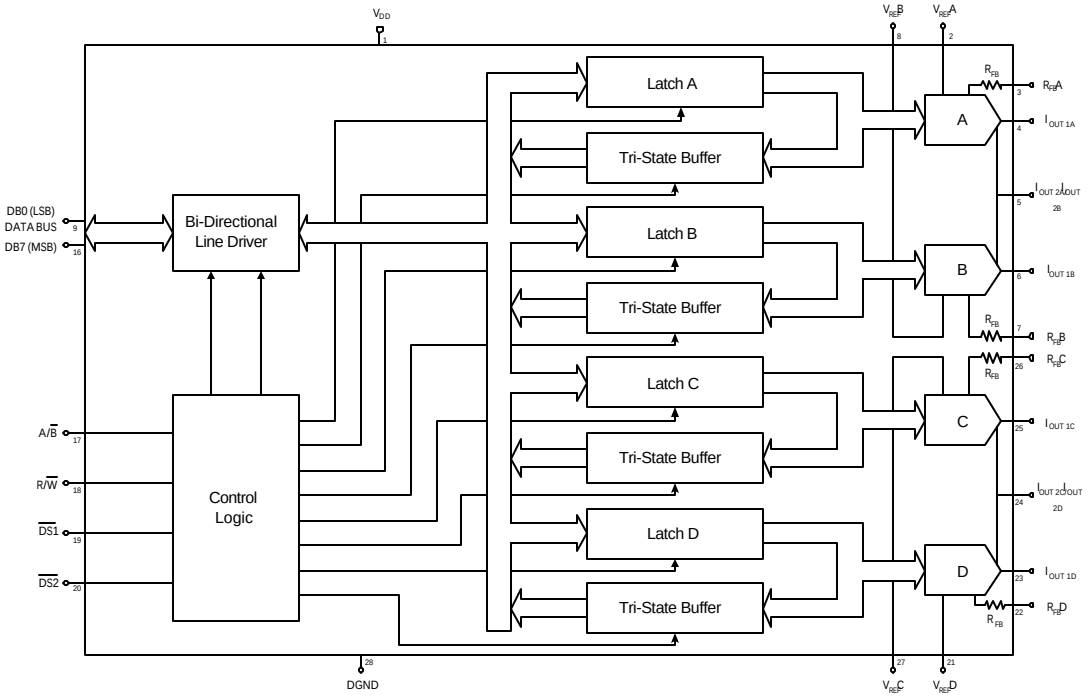
PRELIMINARY

SPACE ELECTRONICS INC.
SPACE PRODUCTS

QUAD 8-BIT MULTIPLYING D/A CONVERTER

8408RP



FEATURES:

- Four DACs in a 28-pin RAD-PAK®
- ± ½ LSB endpoint linearity
- Microprocessor compatible
- TTL/CMOS compatible
- Four quadrant multiplication
- Single supply operation (5V)
- Low power consumption
- Total dose tolerant to 100 krads (Si); dependent on orbit and mission life
- Single event latchup immune to 116 MeV

DESCRIPTION:

Space Electronics' 8408RP is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and onboard data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ determine which DAC will accept data. Data loading is similar to that os a RAMs write cycle. Data can be read back onto the same data bus with control line R/$\overline{W}$. The 8408RP is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The device operates on a single 5V supply and dissipates less than 20 mW.

Space Electronics' RAD-PAK® advanced technology incorporates radiation shielding in microcircuit packages. It eliminates box shielding while providing lifetime in orbit. This product with packaging and screening up to Class S.

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TABLE 1. 8408RP ELECTRICAL CHARACTERISTICS

(@ V_{DD} = 5V; V_{REF} = ± 10V; V_{OUT} A, B, C, D = 0V; T_A = -55 °C TO 125 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
STATIC ACCURACY						
Resolution	N		8	--	--	LSB
Nonlinearity [1,2]	INL	DAC8408 B/F/H	--	--	±½	LSB
Differential Nonlinearity	DNL	DAC8408 B/F/H	--	--	±1	LSB
Gain Error	G_{FSE}	Using internal RFB	--	--	±1	LSB
Gain Tempco [3,4]	TC_{GFS}		--	±2	±40	ppm/°C
Power Supply Rejection	PSR	ΔV_{DD} = ±10%	--	--	0.001	%FSR/%
$I_{OUT\ 1A, B, C, D}$ Leakage Current [5]	I_{LKG}	T_A = 25 °C, T_A = Full temperature range	-- --	-- --	±30 ±200	nA
REFERENCE INPUT						
Input Voltage Range			--	--	±20	V
Input Resistance Match [6]		$R_{A, B, C, D}$	--	--	±1	%
Input Resistance	R_{IN}		6	10	14	kΩ
DIGITAL INPUTS						
Digital Input Low	V_{IL}		--	--	0.8	V
Digital Input High	V_{IH}		2.4	--	--	V
Input Current [7]	I_{IN}	T_A = 25 °C T_A = Full temperature range	-- --	±0.01 --	±1.0 ±10.0	µA
Input Capacitance [4]	C_{IN}		--	--	8	pF
DATA BUS OUTPUTS						
Digital Output Low	V_{OL}	16 mA Sink	--	--	0.4	V
Digital Output High	V_{OH}	400 µA Source	4	--	--	V
Output Leakage Current	I_{LKG}	T_A = 25 °C T_A = Full temperature range	-- --	±0.005 ±0.075	±1.0 ±10.0	µA
DAC OUTPUTS [4]						
Propagation Delay [8]	t_{PD}		--	150	180	ns
Settling Time [9,10]	t_S		--	190	250	ns
Output Capacitance	C_{OUT}	DAC latches all "0s" DAC latches all "1s"	-- --	-- --	30 50	pF
AC Feedthrough	FT	20 V_{p-p} @ F = 100 kHz	54	--	--	dB
SWITCHING CHARACTERISTICS [4,11]						
Write to Data Strobe Time	t_{DS1} or t_{DS2}	T_A = 25 °C T_A = Full temperature range	90 145	-- --	-- --	ns
Data Valid to Strobe Set-Up Time	t_{DSU}	TA = 25 °C TA = Full temperature range	150 175	-- --	-- --	ns
Data Valid to Strobe Hold Time	t_{DH}		10	--	--	ns
DAC Select to Strobe Set-Up Time	t_{AS}		0	--	--	ns

TABLE 1. 8408RP ELECTRICAL CHARACTERISTICS

(@ V_{DD} = 5V; V_{REF} = ± 10V; V_{OUT} A, B, C, D = 0V; T_A = -55 °C TO 125 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DAC Select to Strobe Hold Time	t_{AH}		0	--	--	ns
Write Select to Strobe Set-Up Time	t_{WSU}		0	--	--	ns
Write Select to Strobe Hold Time	t_{WH}		0	--	--	ns
Read to Data Strobe Width	t_{RDS}	T_A = 25 °C T_A = Full temperature range	220 350	-- --	-- --	ns
Data Strobe to Output Valid Time	t_{CO}	T_A = 25 °C T_A = Full temperature range	320 430	-- --	-- --	ns
Output Data to Deselect Time	t_{OTD}	T_A = 25 °C T_A = Full temperature range	200 270	-- --	-- --	ns
Read Select to Strobe Set-Up Time	t_{RSU}		0	--	--	ns
Read Select to Strobe Hold Time	t_{RH}		0	--	--	ns
POWER SUPPLY						
Voltage Range	V_{DD}		4.5	--	5.5	V
Supply Current [12]	I_{DD}		--	--	50	µA
Supply Current [13]	I_{DD}	T_A = 25 °C T_A = Full temperature range	-- --	-- --	1.0 1.5	mA

1. This is an end-point linearity specification.
2. Guaranteed to be monotonic over the full operating temperature range.
3. ppm/°C of FSR (FSR = Full Scale Range = V_{REF}-1 LSB).
4. Guaranteed by design.
5. All digital inputs = 0V; V_{REF} = 10V.
6. Input resistance temperature coefficient = 300 ppm/°C.
7. Logic inputs are MOS gates. Typical input current at 25 °C is less than 10 nA.
8. From digital input to 90% of final analog output current.
9. Digital input = 0V to V_{DD} or V_{DD} to 0V.
10. Extrapolated: t_S (½ LSB) = t_{PD} + 6.2τ where τ = the measured first time constant of the final RC decay.
11. See timing diagram.
12. All digital inputs "0" or V_{DD}.
13. All digital inputs V_{IH} or V_{IL}.

TABLE 2. 8408RP ABSOLUTE MAXIMUM RATINGS [1,2,3,4]

(T_A = 25 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	MIN	MAX	UNIT
V_{DD} to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$	0	7	V
V_{DD} to DGND	0	7	V
$I_{OUT\ 1A}$, $I_{OUT\ 1B}$, $I_{OUT\ 1C}$, $I_{OUT\ 1D}$ to DGND	-0.3	V_{DD} + 0.3	V
R_{FB}A, R_{FB}B, R_{FB}C, R_{FB}D to I_{OUT}	-25	25	V

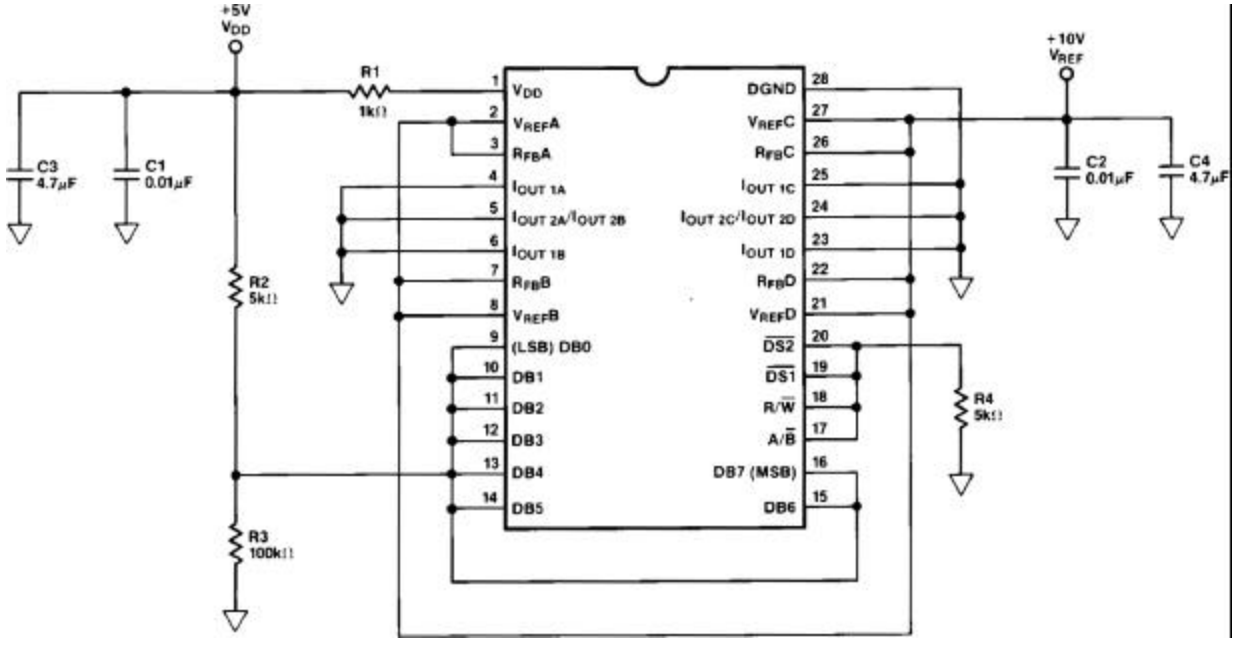
TABLE 2. 8408RP ABSOLUTE MAXIMUM RATINGS [1,2,3,4]

(T_A = 25 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	MIN	MAX	UNIT
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$, to DGND	-0.3	V_{DD} + 0.3	V
DB0 through DB7 to DGND	-0.3	V_{DD} + 0.3	V
Control Logic Input Voltage to DGND	-0.3	V_{DD} + 0.3	V
$V_{REF}A$, $V_{REF}B$, $V_{REF}C$, $V_{REF}D$ to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$	-25	25	V
Operating Temperature Range - Commercial Grade (GP) - Industrial Grade (ET, FT, FP, FPC, FS) - Military Grade (AT, BT)	 0 -40 -55	 70 85 125	°C
Junction Temperature	--	150	°C
Storage Temperature	-65	150	°C
Lead Temperature (soldering, 10 sec)	--	300	°C

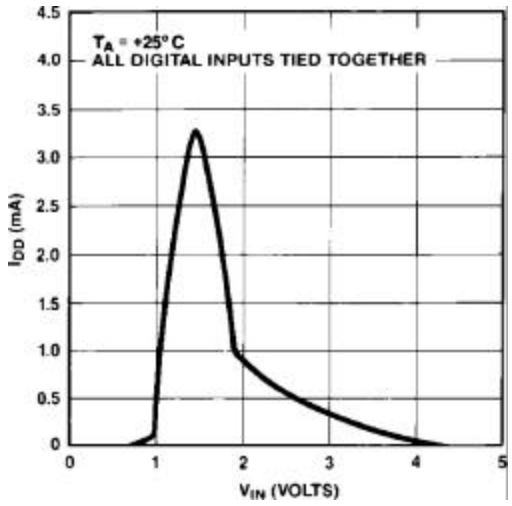
1. Do not apply voltages higher than V_{DD} + 0.3V or less than -0.3V potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high energy electrostatic fields. Keep in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

BURN-IN CIRCUIT

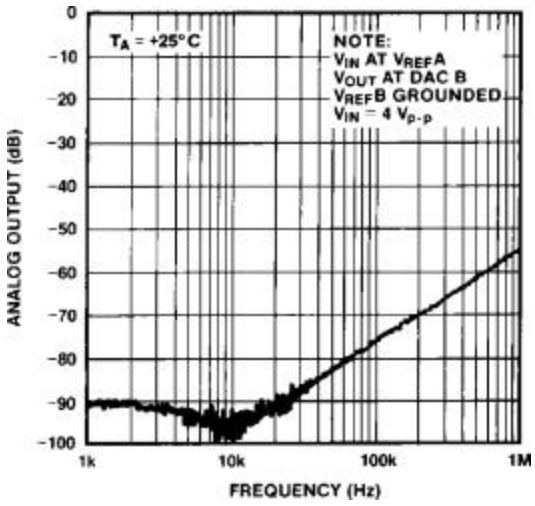


TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT VS. LOGIC LEVEL



ANALOG CROSSTALK VS. FREQUENCY



TIMING DIAGRAM

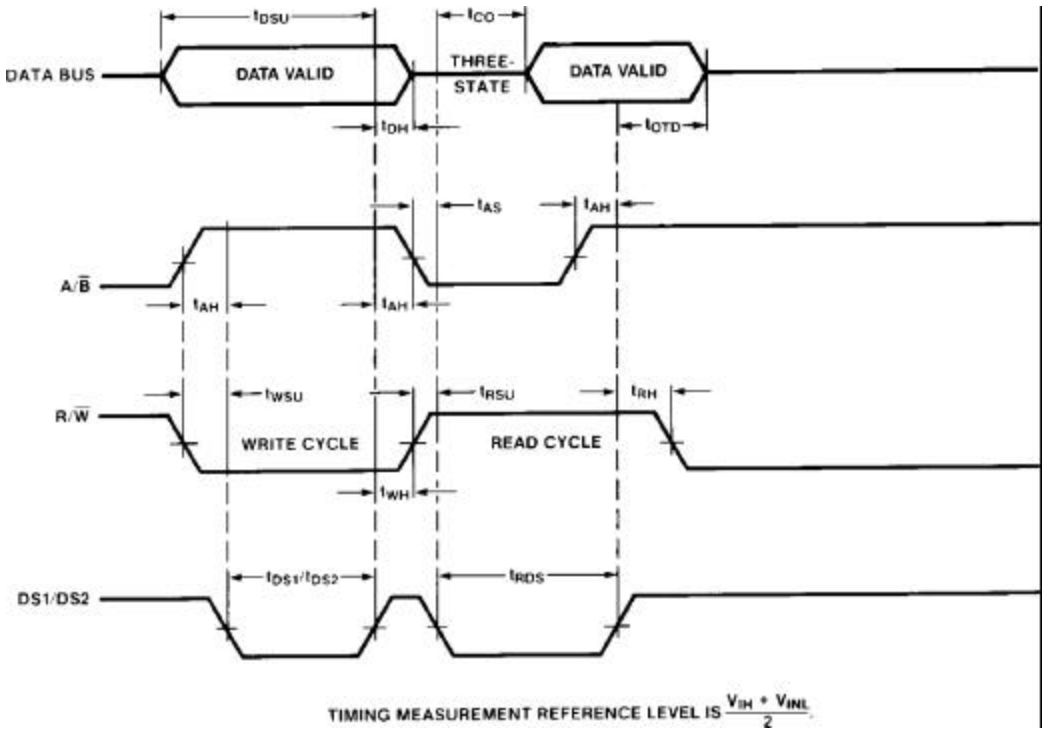


FIGURE 1. SIMPLIFIED D/A CIRCUIT 8408RP

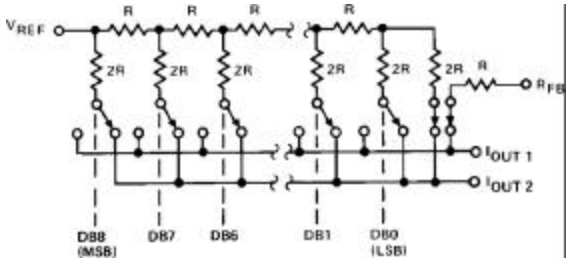


FIGURE 2. N-CHANNEL CURRENT STEERING SWITCH

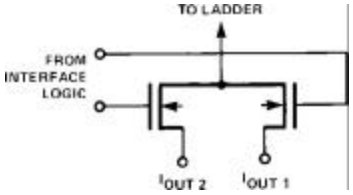


FIGURE 3. EQUIVALENT DAC CIRCUIT (ALL DIGITAL INPUTS HIGH)

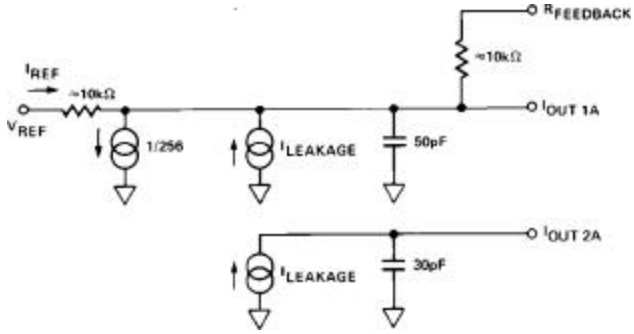
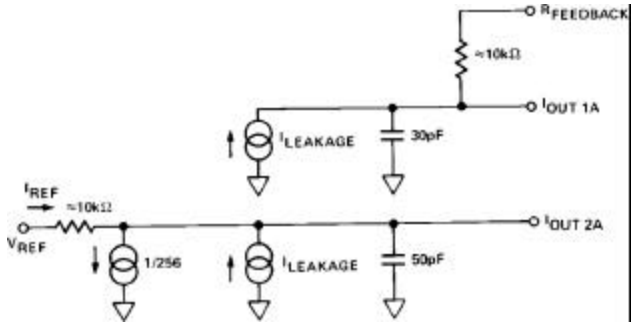


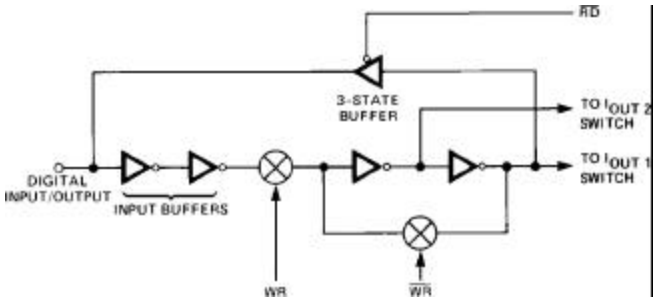
FIGURE 4. EQUIVALENT DAC CIRCUIT (ALL DIGITAL INPUTS LOW)



DIGITAL SECTION

Figure 5 shows the digital input/output structure for one bit. The digital WR, $\overline{WR}$, and $\overline{RD}$ controls shown in the figure are internally generated from the external A/$\overline{B}$, R/$\overline{W}$, $\overline{DS1}$, and $\overline{DS2}$ signals. The combination of these signals decide which DAC is selected. The digital inputs are CMOS inverters, designed such that TTL input levels (2.4V and 0.8V) are converted into CMOS logic levels. When the digital input is in the region of 1.2V to 1.8V, the input stages operate in their linear region and draw current from the 5V supply (see Typical Supply Current vs. Logic Level curve on page 5). It is recommended that the digital input voltages be as close to VDD and DGND as is practical in order to minimize supply currents. This allows maximum savings in power dissipation inherent with CMOS devices. The three state readback digital output drivers (in the active mode) provide TTL-compatible digital outputs with a fan-out of one TTL load. The three state digital readback leakage-current is typically 5 nA.

FIGURE 5. DIGITAL INPUT/OUTPUT STRUCTURE



INTERFACE LOGIC SECTION

DAC Operating Modes

- All DACs in HOLD MODE.
- DAC A, B, C, or D individually selected (WRITE MODE).
- DAC A, B, C, or D individually selected (READ MODE).
- DACS A and C simultaneously selected (WRITE MODE).
- DACs B and D simultaneously selected (WRITE MODE).

DAC Selection:

Control inputs, $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ select which DAC can accept data from the input port (see Mode Selection Table).

Mode Selection:

Control inputs $\overline{DS}$ and R/$\overline{W}$ control the operating mode of the selected DAC.

Write Mode:

When the control inputs $\overline{DS}$ and R/$\overline{W}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent, and its analog output responds to activity on the data inputs DB0-DB7.

Hold Mode:

The selected DAC latch retains the data that was present on the bus line just prior to $\overline{DS}$ or R/$\overline{W}$ going to a high state. All analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and R/$\overline{W}$ is high, the selected DAC is in the read mode, and the data held in the appropriate latch is put back onto the data bus.

TABLE 3. MODE SELECTION TABLE

(L = LOW STATE, H = HIGH STATE, X = IRRELEVANT)

CONTROL LOGIC				MODE	DAC
DS1	DS2	A/B	R/W		
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A & C
L	L	L	L	WRITE	B & D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

BASIC APPLICATIONS

Same basic circuit configurations are shown in Figures 6 and 7. Figure 6 shows the 8408RP connected in a unipolar configuration (2-Quadrant Multiplication) and Table 4 shows the code table. Resistors R1, R2, R3, and R4 are used to trim full scale output. Full-scale output voltage = V_{REF} -1 LSB = V_{REF} (1-2^{-8}) of V_{REF} x (255/256) with all digital inputs high. Low temperature coefficient (approximately 50 ppm/ºC) resistors or trimmers should be selected if used. Full scale can also be adjusted using V_{REF} voltage. This will eliminate resistors R1, R2, R3, and R4. In many applications, R1 through R4 are required, and the maximum gain error will then be that of the DAC.

Each DAC exhibits a variable output resistance that is code-dependent. This produces a code-dependent, differential non-linearity term at the amplifier's output which can have a maximum value of 0.67 x the amplifier's offset voltage. This differential nonlinearity term adds to the R-2R resistor ladder differential-nonlinearity; the output may no longer be monotonic. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (1 LSB = 2^{-8} x V_{REF} or 1/256 x V_{REF}), or less than 3.9 mV over the operating temperature range. Zero-scale output voltage (with all difital inputs low) may be adjusted using the op amp offset adjustment. Capacitors C1, C2, C#, and C4 provide phase compensation and help prevent overshoot and ringing when using high speed op amps.

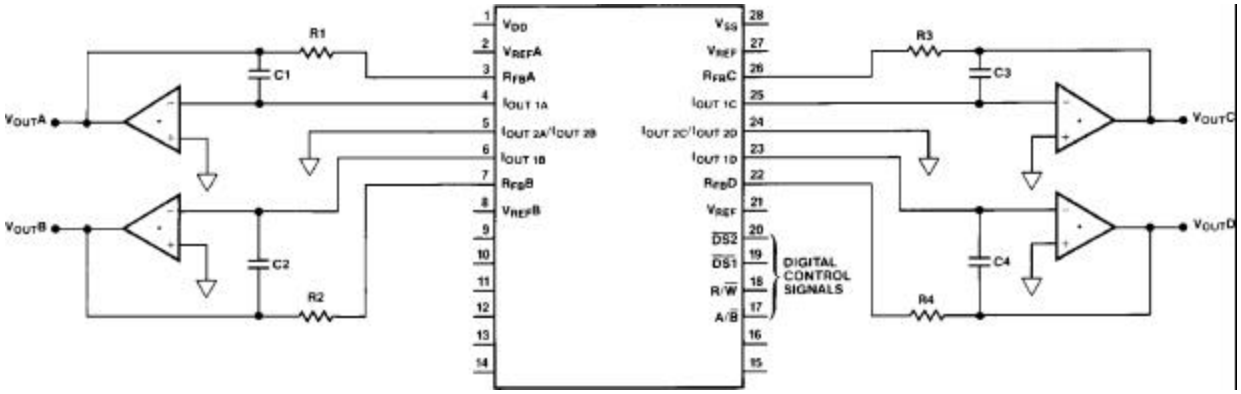
Figure 7 shows the recommended circuit configuration for the bipolar operation (4-quadrant multiplication), and Table 5 shows the code table. Trimmer resistors R17, R18, R19, and R20 are used only if gain error adjustments are required and range between 50 Ω and 1000 Ω. Resistors R21, R22, R23, and R24 will range between 50 Ω and 500 Ω. If these resistors are ued, it is essential that resistor pairs R9-R13, R10-R14, R11-R15, R12-R16 are matched both in value and tempco. They should be within 0.01%; wire wound or metal foil types are preferred for best temperature coefficient matching. The circuits of Figure 6 and 7 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage

TABLE 4. UNIPOLAR BINARY CODE TABLE REFER TO FIGURE 6)[1]

DAC DATA INPUT								ANALOG OUTPUT
MSB							LSB	
1	1	1	1	1	1	1	1	$-V_{REF}(^{255}/_{256})$
1	0	0	0	0	0	0	1	$-V_{REF}(^{129}/_{256})$
1	0	0	0	0	0	0	0	$-V_{REF}(^{128}/_{256}) = -V_{IN}/2$
0	1	1	1	1	1	1	1	$-V_{REF}(^{127}/_{256})$
0	0	0	0	0	0	0	1	$-V_{REF}(^{1}/_{256})$
0	0	0	0	0	0	0	0	$-V_{REF}(^{0}/_{256}) = 0$

1. 1 LSB = $(2^{-8})(V_{REF}) = {}^{1}/_{256}(V_{REF})$

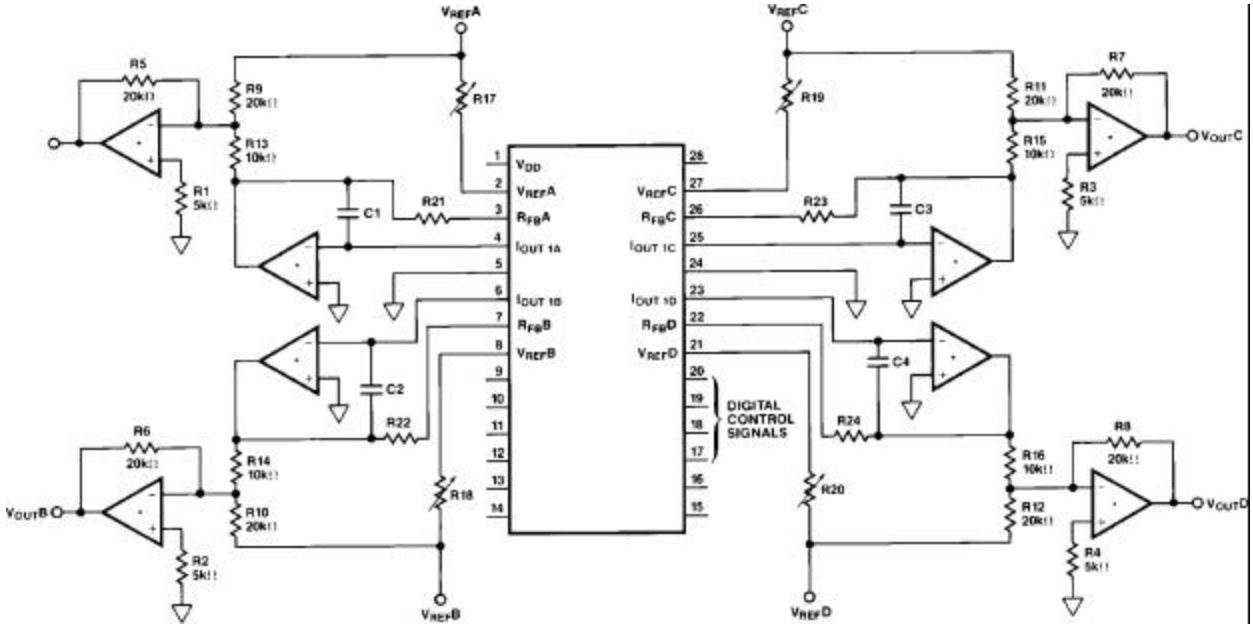
FIGURE 6. QUAD DAC UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION) [1]



Note:

1. All amplifiers are OP-27s, ¼ OP-420s, or ¼ OP-421s.

FIGURE 7. QUAD DAC BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION) [1]



Note:

1. All amplifiers are OP-27s, ¼ OP-420s, or ¼ OP-421s.

TABLE 5. BIPOLAR (OFFSET BINARY) CODE TABLE (REFERE TO FIGURE 7)

DAC DATA INPUT								ANALOG OUTPUT
MSB							LSB	(DAC A OR DAC B)
1	1	1	1	1	1	1	1	$V_{REF}(^{127}/_{128})$
1	0	0	0	0	0	0	1	$V_{REF}(^{1}/_{128})$
1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	$-V_{REF}(^{1}/_{128})$
0	0	0	0	0	0	0	1	$-V_{REF}(^{127}/_{128})$
0	0	0	0	0	0	0	0	$-V_{REF}(^{128}/_{128})$

APPLICATION HINTS

General Ground Management:

AC or transient voltages between AGND and DGND can appear as noise at the analog output. Note that in Figures 5 and 6, $I_{OUT\,2A}/I_{OUT\,2B}$ and $I_{OUT\,2C}/I_{OUT\,2D}$ are connected to AGND. Therefore, it is recommended that AGND and DGND be tied together at the device socket. In systems where AGND and DGND are tied together on the backplace, two diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND.

Write Enable Timing:

During the period when both $\overline{DS}$ and R/$\overline{W}$ are held low, the DAC latches are transparent and the analog output responds directly to the digital data input. To prevent unwanted variations of the analog output, the R/$\overline{W}$ should not go low until the data bus is fully settled (DATA VALID).

Single Supply, Voltage Output Operation

The 8408RP can be connected with a single 5V supply to produce DAC output voltages from 0V to 1.5V. In Figure 8, the device R-2R ladder is inverted from its normal connection. A + 1.500V reference is connected to the current output pin 4 (IOUT 1A), and the normal VREF input pin becomes the DAC output. Instead of a normal current output, the R-2R ladder outputs a voltage. The OP-490, consisting of four precision low power op-amps that can operate its inputs and outputs to zero volts, buffers the DAC to produce a low impedance output voltage from 0V to 1.5V full-scale. Table 6 shows the code table.

With the supply and reference voltages as shown, better than ½ LSB differential and integral nonlinearity can be expected. To maintain this performance level, the 5V supply must not drop below 4.75V. Similarly, the reference voltage must be no higher than 1.5V. This is because the CMOS switches require a minimum level of bias in order to maintain the linearity performance.

SINGLE SUPPLY BINARY CODE TABLE (REFER TO FIGURE 8)

DAC DATA INPUT								ANALOG OUTPUT
MSB							LSB	
1	1	1	1	1	1	1	1	$V_{REF}(^{255}/_{256})$, + 1.4941V
1	0	0	0	0	0	0	1	$V_{REF}(^{129}/_{256})$, + 0.7559V
1	0	0	0	0	0	0	0	$V_{REF}(^{128}/_{256})$, + 0.7500V
0	1	1	1	1	1	1	1	$V_{REF}(^{127}/_{256})$, + 0.7441V
0	0	0	0	0	0	0	1	$V_{REF}(^{1}/_{256})$, + 0.0059V
0	0	0	0	0	0	0	0	$V_{REF}(^{0}/_{256})$, 0.0000V

FIGURE 8. UNIPOLAR SUPPLY, VOLTAGE OUTPUT DAC OPERATION

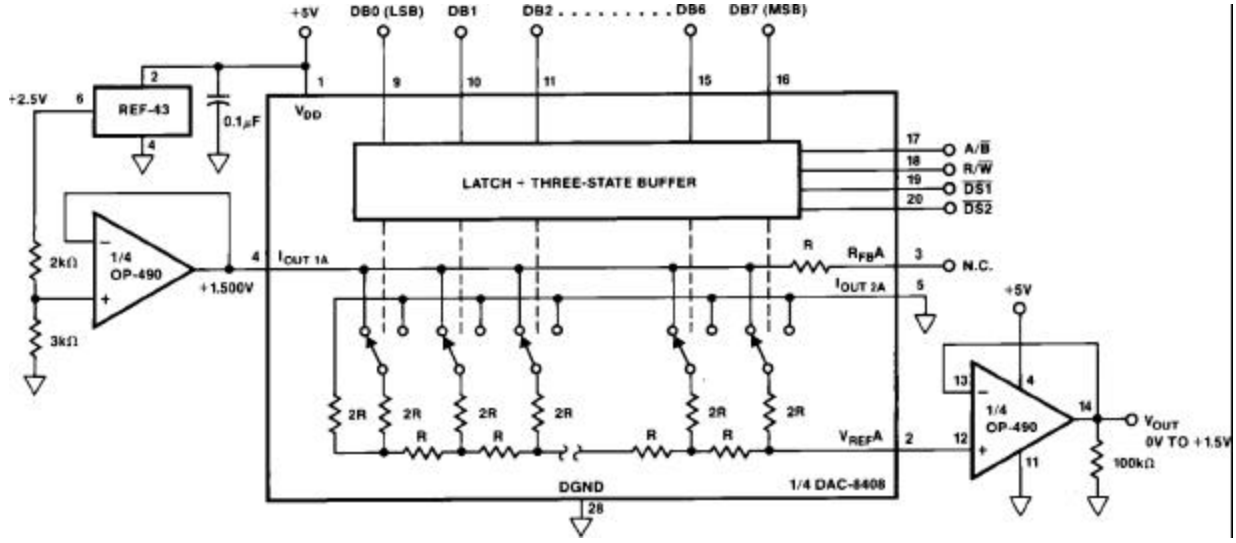
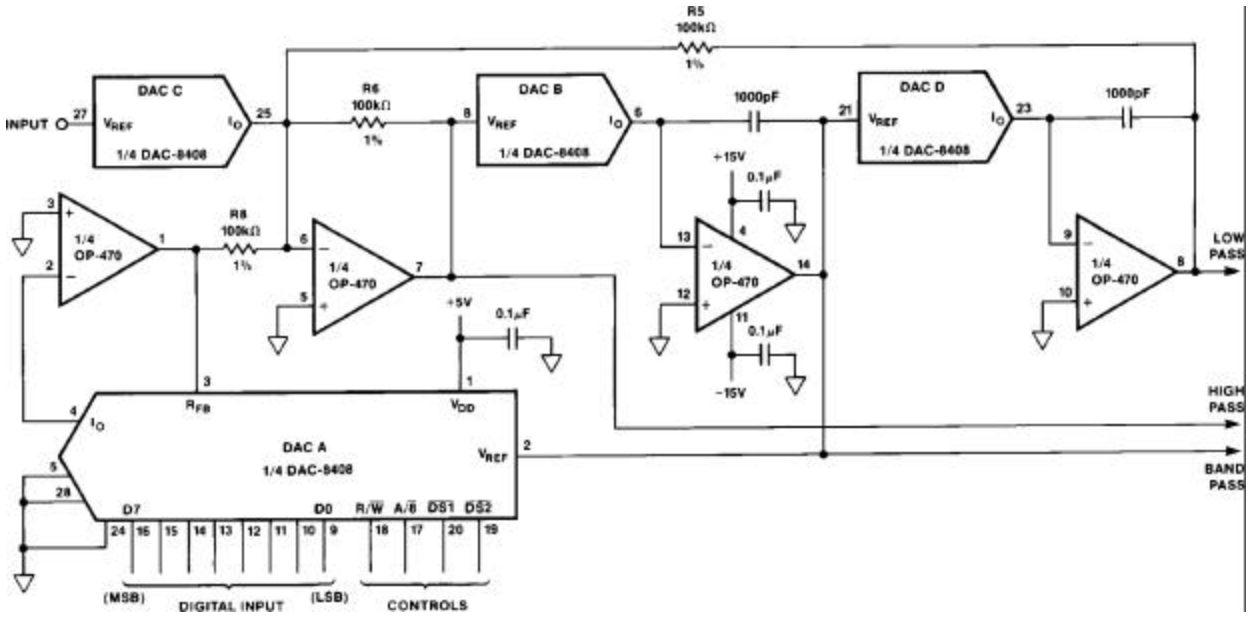


FIGURE 9. A DIGITALLY PROGRAMMABLE UNIVERAL ACTIVE FILTER



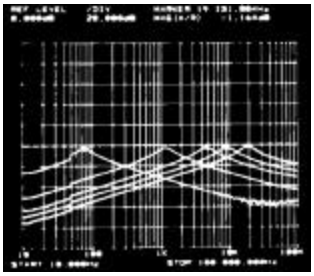
A Digitally Programmable Active Filter

A power D/A converter application is a programmable active filter design as shown in Figure 9. The design is based on the state-variable filter topology that offers stable and repeatable filter characteristics. DAC B and DAC D can be programmed in tandem with a single digital byte load that sets the center frequency of the filter. DAC A sets the Q of the filter. DAC C sets the gain of the filter transfer function. The unique feature of this design is that varying the gain of filter does not affect the Q of the filter. Similarly, the reverse is true. This makes the programmability of the filter extremely reliable and predictable. Note that low-pass, high-pass, and bandpass outputs are available. This sophisticated function is achieved in only two IC packages.

The network analyzer photo shown in Figure 10 superimposes five actual bandpass responses ranging from the lowest frequency of 7 5 Hz (1 LSB ON) to a full-scale frequency of 19.132 kHz (all bits ON), that is equivalent to a 256 to 1 dynamic range. The frequency is determined by $f_C = \frac{1}{2}\pi RC$ where R is the ladder resistance (R_{IN}) of the 8408RP and C is 1000 pF. Note that from device to device, the resistance R_{IN} varies. Thus, some tuing may be necessary.

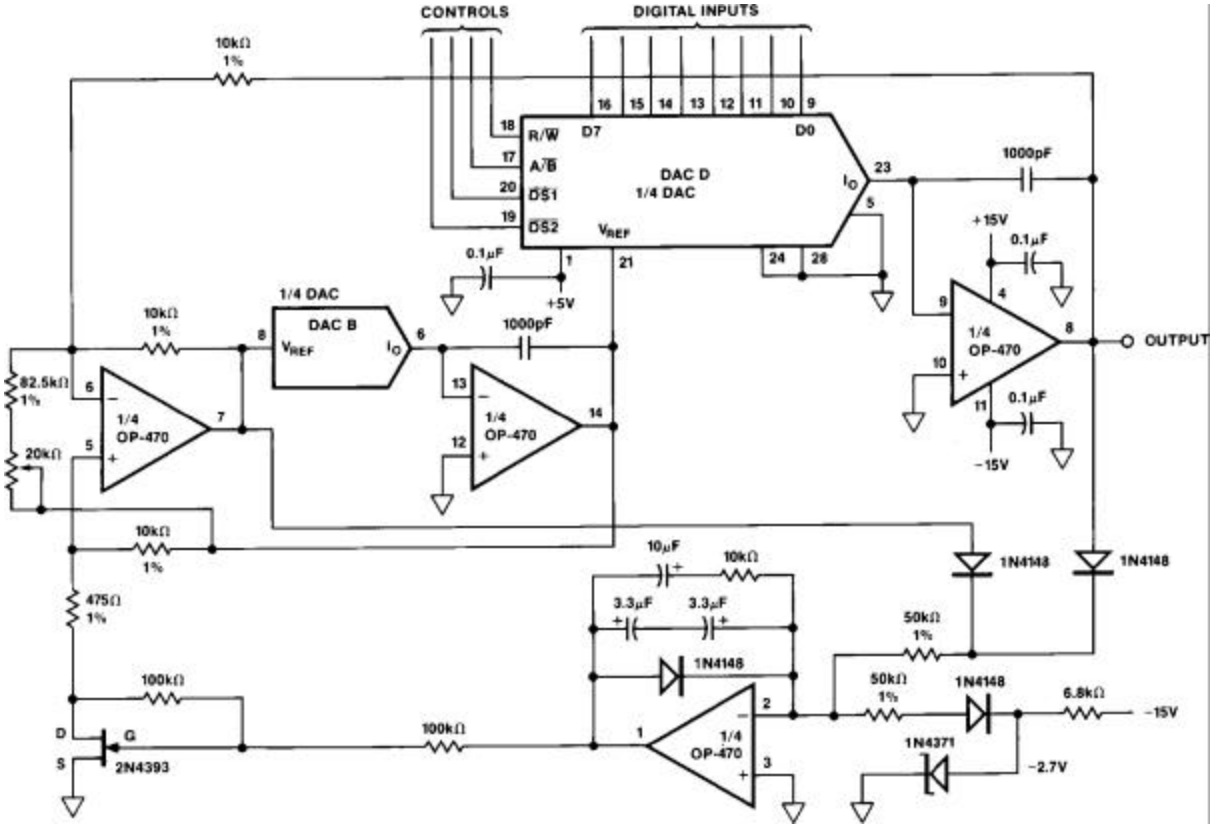
All components used are available off-the-shelf. Using low drift thin-film resistors, the 8408RP exhibits very stable performance over temperature. The wide bandwidth of the OP-470 produces excellent high frequency and high Q response. In addition, the OP470's low input offset vo ltage assures an unusually low DC offset at the filter output.

FIGURE 10. PROGRAMMABLE ACTIVE FILTER BAND-PASS FREQUENCY RESPONSE



The circuit provides full 8-bit (> 2 decade) dynamic range of frequency control.

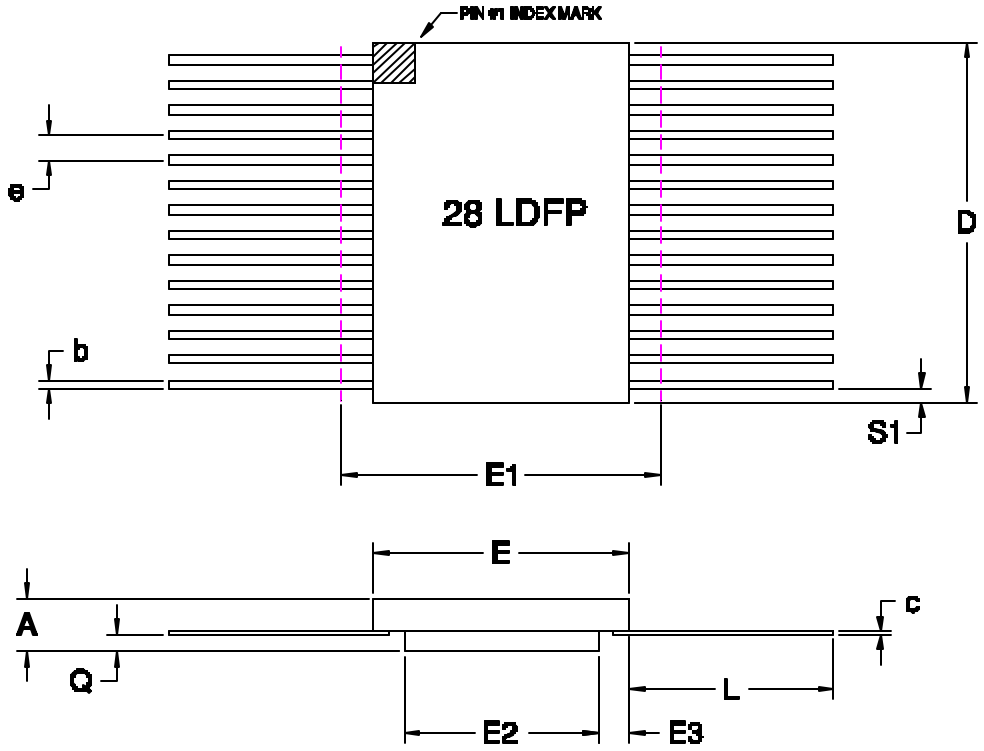
FIGURE 11. A DIGITALLY PROGRAMMABLE, LOW-DISTORTION SINEWAVE OSCILLATOR



A Low-Distortion, Programmable Sinewave Oscillator

By varying the previous state-variable filter topology slightly, one can obtain a very low distortion sinewave oscillator with programmable frequency feature as shown in Figure 11. Again, DAC B and DAC D in tandem control the oscillating frequency based on the relationship $f_c = \frac{1}{2}\pi RC$. Positive feedback is accomplished via the 82.5 kΩ and the 20 kΩ potentiometer.The Q of the oscillator is determined by the ratio of 10 kW and 475 W in series with the FET transistor, which acts as an automatic gain control variable resistor. The AGC action maintains a very stable sinewave ampli tude at any frequency. Again, only two ICs accomplish a very useful function.

At the highest frequency setting, the harmonic distortion level measures 0.016%. As the frequencies drop, distortion also drops to a low of 0.006%. At the lowest frequency setting, distortion came back up to a worst case of 0.035%.



28 PIN FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.129	0.142	0.155
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.720	0.740
E	0.400	0.410	0.420
E1	--	--	0.440
E2	0.180	0.250	--
E3	0.005	0.080	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.021	0.033	0.045
S1	0.005	0.028	--
N	28		

F28-07

Note: All dimensions in inches.

Important Notice:

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