8XC251SB
HIGH-PERFORMANCE
CHMOS SINGLE-CHIP MICROCONTROLLER

Commercial

- **Binary-code Compatible with MCS® 51 Microcontrollers**
- **Pin Compatible with 44-lead PLCC MCS 51 Microcontrollers**
- **Register-based MCS 251 Architecture**
  - **— 40-byte Register File**
  - **— Registers Accessible as Bytes, Words, and Double Words**
- **Enriched Instruction Set**
  - **— 16-bit and 32-bit Arithmetic and Logic Instructions**
  - **— Compare and Conditional Jump Instructions**
  - **— Expanded Set of Move Instructions**
- **Linear Addressing**
- **128-Kbyte External Code/Data Memory Space**
- **16-Kbyte On-chip OTPROM/ROM (Optional device without ROM available)**
- **16-bit Internal Code Fetch**
- **64-Kbyte Extended Stack Space**
- **1-Kbyte On-chip Data RAM**
- **8-bit, 2-clock External Code Fetch in Page Mode**
- **Instruction Pipeline**
- **User-selectable Configurations:**
  - **— External Wait State**
  - **— Address Range**
  - **— Page Mode**
- **32 Programmable I/O Lines**
- **Seven Maskable Interrupt Sources with Four Programmable Priority Levels**
- **Three Flexible 16-bit Timer/counters**
- **Hardware Watchdog Timer**
- **Programmable Counter Array**
  - **— High-speed Output**
  - **— Compare/Capture Operation**
  - **— Pulse Width Modulator**
  - **— Watchdog Timer**
- **Programmable Serial I/O Port**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **Power-saving Idle and Powerdown Modes**
- **High-performance CHMOS Technology**
- **0–16 MHz Operation**
- **Complete System Development Support**
  - **— Compatible with Existing Tools**
  - **— New Tools Available: Compiler, Assembler, Debugger, ICE**

A member of the Intel family of 8-bit MCS 251 microcontrollers, the 8XC251SB is binary-code compatible with MCS 51 microcontrollers and pin compatible with 44-lead PLCC MCS 51 microcontrollers. MCS 251 microcontrollers feature an enriched instruction set, linear addressing, and efficient C-language support. The 8XC251SB has 1 Kbyte of on-chip RAM and is available with 16 Kbytes of on-chip OTPROM (87C251SB), with 16 Kbytes of ROM (83C251SB), or without ROM (80C251SB). A variety of features can be selected by user-programmed OTPROM configuration (87C251SB) or factory-programmed ROM configuration (83C251SB).

September 1995 **Order Number:** 272616-003

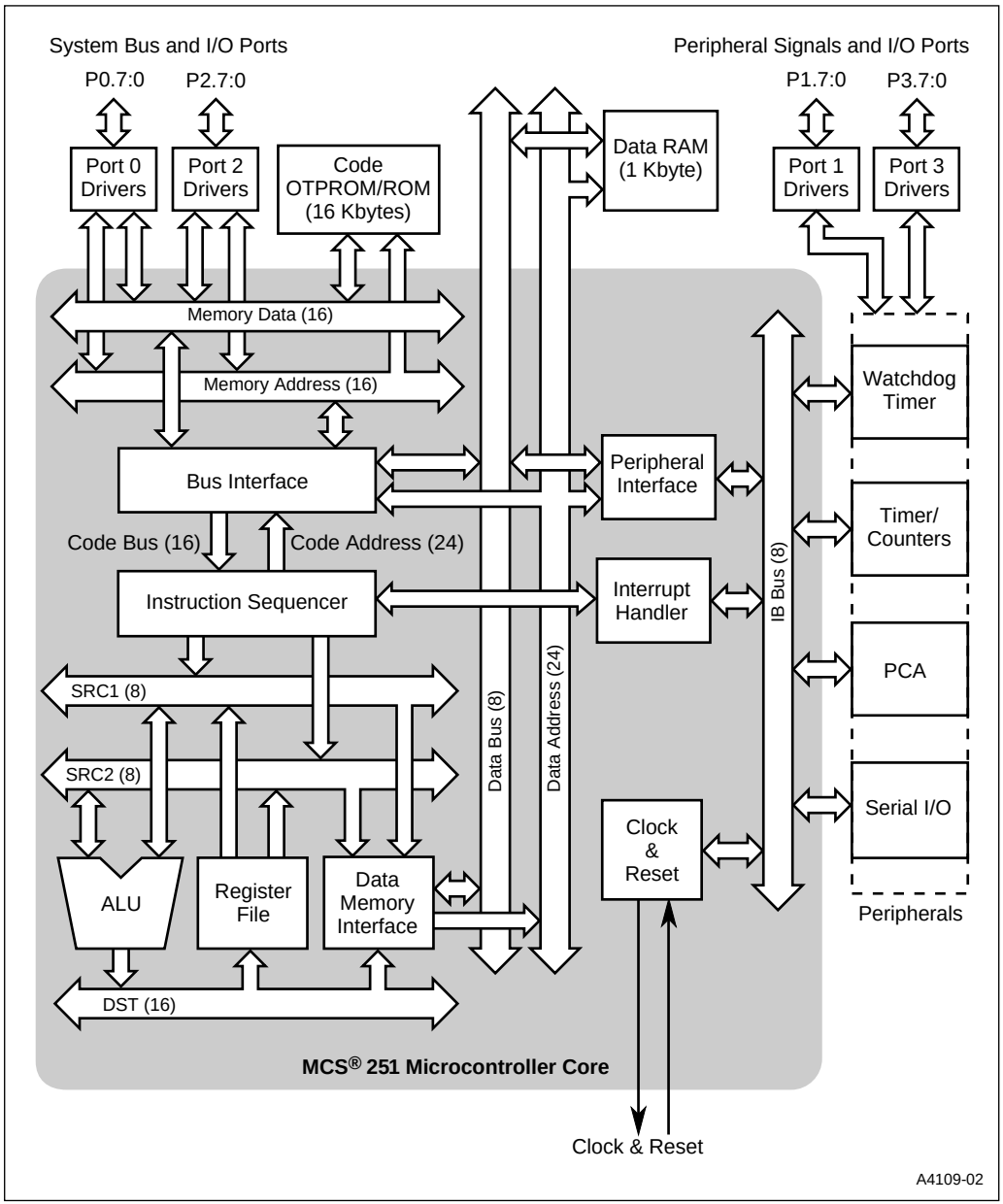


Figure 1. 8XC251SB Block Diagram

COMMERCIAL TEMPERATURE RANGE

With the commercial (standard) temperature option, the device operates over the temperature range 0°C to +70°C.

PROLIFERATION OPTIONS

Table 1. Proliferation Options

8XC251SB (1) (0 – 12 MHz; 5 V ±10%)	8XC251SB-16 (1) (0 – 16 MHz; 5 V ±10%)
80C251SB (2)	80C251SB-16 (3)
83C251SB	83C251SB-16
87C251SB	87C251SB-16

NOTES:

1. The 8XC251SB and 8XC251SB-16 are binary-code compatible with MCS 51 microcontrollers.
2. Configurations available for 80C251SB:
   a. Nonpage mode and no wait states (Table 13)
   b. User-defined configurations
3. Configurations available for 80C251SB-16:
   a. Nonpage mode and one wait state (Table 13)
   b. User-defined configurations

NOTE:

Data for the 8XC251SB also applies to the 8XC251SB-16 unless otherwise noted.

PROCESS INFORMATION

This device is manufactured on a complimentary high performance metal-oxide semiconductor (CHMOS) process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook* (order number 210997).

All thermal impedance data is approximate for static air conditions at 1 watt of power dissipation. Values change dependent upon operating conditions and application requirements. The Intel *Packaging Handbook* (order number 240800) describes Intel's thermal impedance test methodology.

Table 2. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}
44-pin PLCC	46°C/W	16°C/W

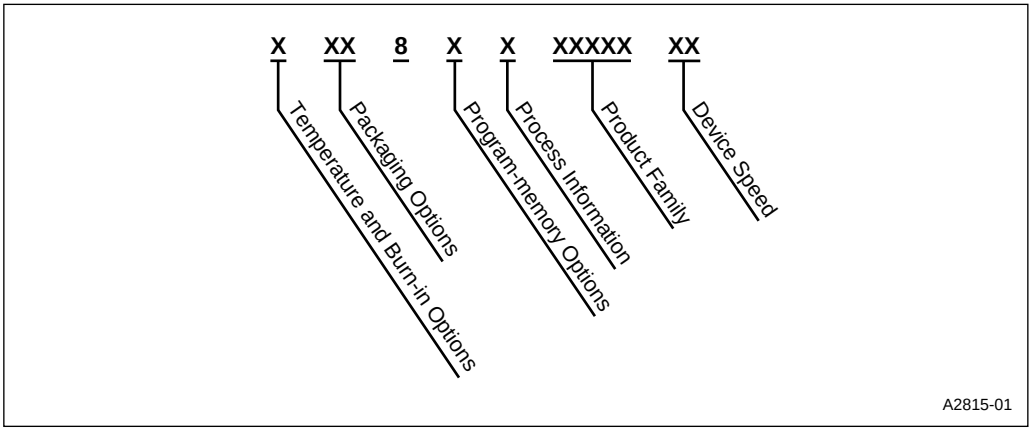


Figure 2. The 8XC251SB Family Nomenclature

Table 3. Description of Product Nomenclature

Parameter	Options	Description
Temperature and Burn-in Options	no mark	Commercial operating temperature range (0°C to 70°C) with Intel standard burn-in.
Packaging Options	N	Plastic Leaded Chip Carrier (PLCC)
Program Memory Options	0	Without ROM
	3	With ROM
	7	With OTPROM
Process Information	C	CHMOS
Product Family	251SB	Advanced 8-bit control architecture
Device Speed	no mark	12 MHz
	-16	16 MHz

Table 4. 8XC251SB Memory Map

Address (Note 1, 2)	Description	Notes
FF:FFFFH FF:4000H	External Memory	3
FF:3FFFH FF:0000H	87C251SB/83C251SB: 16-Kbyte Internal OTPROM/ROM or External Memory, as determined by EA# pin (Table 7) 80C251SB: External Memory	3, 4, 5
FE:FFFFH FE:0000H	External Memory	3
FD FFFFH 02:0000H	Reserved	6
01:FFFFH 01:0000H	External Memory	3
00:FFFFH 00:E000H	87C251SB/83C251SB: External Memory or redirected to OTPROM/ROM 80C251SB: External Memory	5, 7
00:DFFFH 00:0420H	External Memory	7
00:041FH 00:0080H	On-chip RAM	7
00:007FH 00:0020H	On-chip RAM	8
00:001FH 00:0000H	Storage for R0–R7 of Register File	9

NOTES:
1. Only 16/17 address lines are bonded out (A15:0 or A16:0 as selected during chip configuration).
2. The special function registers (SFRs) and the register file have separate address spaces.
3. Data is accessible by indirect addressing only.
4. The 8XC251SB resets to location FF:0000H.
5. The 87C251SB/83C251SB can be configured so that locations FF:2000H–FF:3FFFH in internal OTPROM/ROM are also mapped to locations 00:E000H–00:FFFFH. In this case, if EA# = 1, a data read to 00:E000H–00:FFFFH is redirected to internal OTPROM/ROM (see bit 1 in CONFIG0).
6. This reserved area of memory is unavailable for use. Reading a location in this area returns an unspecified value. A write to this area does execute, but nothing is actually written.
7. Data is accessible by direct and indirect addressing.
8. Data is accessible by direct, indirect, and bit addressing.
9. Data is accessible by direct, indirect, and register addressing.

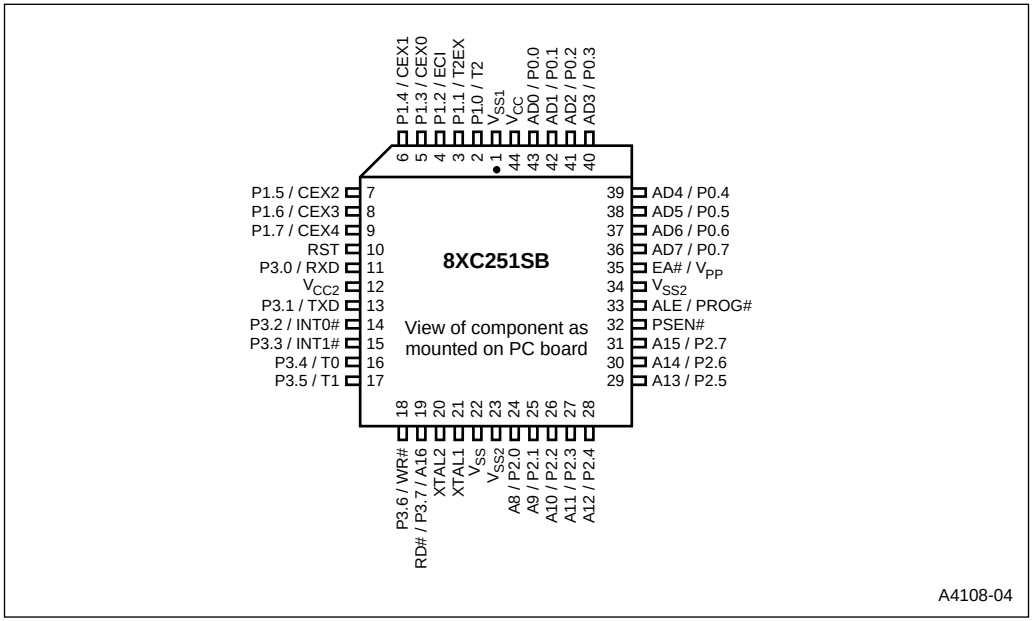


Figure 3. 8XC251SB 44 Lead PLCC Package

Table 5. 44-pin PLCC Pin Assignment

Pin	Name	Pin	Name
1	V_{SS1}	23	V_{SS2}
2	T2/P1.0	24	A8/P2.0
3	T2EX/P1.1	25	A9/P2.1
4	ECI/P1.2	26	A10/P2.2
5	CEX0/P1.3	27	A11/P2.3
6	CEX1/P1.4	28	A12/P2.4
7	CEX2/P1.5	29	A13/P2.5
8	CEX3/P1.6	30	A14/P2.6
9	CEX4/P1.7	31	A15/P2.7
10	RST	32	PSEN#
11	RXD/P3.0	33	ALE/PROG#
12	V_{CC2}	34	V_{SS2}
13	TXD/P3.1	35	EA#/V_{PP}
14	INT0#/P3.2	36	AD7/P0.7
15	INT1#/P3.3	37	AD6/P0.6
16	T0/P3.4	38	AD5/P0.5
17	T1/P3.5	39	AD4/P0.4
18	WR#/P3.6	40	AD3/P0.3
19	RD#/P3.7	41	AD2/P0.2
20	XTAL2	42	AD1/P0.1
21	XTAL1	43	AD0/P0.0
22	V_{SS}	44	V_{CC}

Table 6. 44-pin PLCC Pin Assignment Arranged by Functional Categories

Address & Data	
Name	**Pin**
AD0/P0.0	43
AD1/P0.1	42
AD2/P0.2	41
AD3/P0.3	40
AD4/P0.4	39
AD5/P0.5	38
AD6/P0.6	37
AD7/P0.7	36
A8/P2.0	24
A9/P2.1	25
A10/P2.2	26
A11/P2.3	27
A12/P2.4	28
A13/P2.5	29
A14/P2.6	30
A15/P2.7	31

Processor Control	
Name	**Pin**
INT0#/P3.2	14
INT1#/P3.3	15
EA#/V_{PP}	35
RST	10
XTAL1	21
XTAL2	20

Input/Output	
Name	**Pin**
T2/P1.0	2
T2EX/P1.1	3
ECI/P1.2	4
CEX0/P1.3	5
CEX1/P1.4	6
CEX2/P1.5	7
CEX3/P1.6	8
CEX4/P1.7	9
RXD/P3.0	11
TXD/P3.1	13
T0/P3.4	16
T1/P3.5	17

Power & Ground	
Name	**Pin**
V_{CC}	44
V_{CC2}	12
V_{SS}	22
V_{SS1}	1
V_{SS2}	23, 34

Bus Control & Status	
Name	**Pin**
WR#/P3.6	18
RD#/P3.7	19
ALE/PROG#	33
PSEN#	32

PIN DESCRIPTIONS

Table 7. Pin Descriptions

Signal Name	Type	Description	Multiplexed With
A16	O	**Address Line 16**. See RD#.	N.A.
A15:8†	O	**Address Lines**. Upper address lines for the external bus.	P2.7:0
AD7:0†	I/O	**Address/Data Lines**. Multiplexed lower address lines and data lines for external memory.	P0.7:0
ALE	O	**Address Latch Enable**. ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from the address/data bus.	PROG#
CEX4:0	I/O	**Programmable Counter Array (PCA) Input/Output Pins**. These are input signals for the PCA capture mode and output signals for the PCA compare mode and PCA PWM mode.	P1.7:3
EA#	I	**External Access**. Directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is to on-chip OTPROM/ROM if the address is within the range of the on-chip OTPROM/ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground.	V_{PP}
ECI	I	**PCA External Clock Input**. External clock input to the 16-bit PCA timer.	P1.2
INT1:0#	I	**External Interrupts 0 and 1**. These inputs set bits IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits INT1:0 are clear, bits IE1:0 are set by a low level on INT1:0#.	P3.3:2
P0.7:0	I/O	**Port 0**. This is an 8-bit, open-drain, bidirectional I/O port.	AD7:0
P1.0 P1.1 P1.2 P1.7:3	I/O	**Port 1**. This is an 8-bit, bidirectional I/O port with internal pullups.	T2 T2EX ECI CEX4:0
P2.7:0	I/O	**Port 2**. This is an 8-bit, bidirectional I/O port with internal pullups.	A15:8
P3.0 P3.1 P3.3:2 P3.5:4 P3.6 P3.7	I/O	**Port 3**. This is an 8-bit, bidirectional I/O port with internal pullups.	RXD TXD INT1:0# T1:0 WR# RD#
PROG#	I	**Programming Pulse**. The programming pulse is applied to this pin for programming the on-chip OTPROM.	ALE

NOTE: †The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Pin Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
PSEN#	O	**Program Store Enable**. Read signal output. This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte CONFIG1 (see also RD#): **RD1 RD0 Address Range for Assertion** 0 0 Reserved 0 1 All addresses 1 0 All addresses 1 1 All addresses ≥ 80:0000H	—
RD#	O	**Read or 17th Address Bit (A16).** Read signal output to external data memory or 17th external address bit (A16), depending on the values of bits RD0 and RD1 in configuration byte CONFIG1. (See also PSEN#): **RD1 RD0 Function** 0 0 Reserved 0 1 The pin functions as A16 only. 1 0 The pin functions as P3.7 only. 1 1 RD#: asserted for reads at all addresses ≤ 7F:FFFFH	P3.7
RST	I	**Reset**. Reset input to the chip. Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pulldown resistor, which allows the device to be reset by connecting a capacitor between this pin and V_{CC}. Asserting RST when the chip is in idle mode or powerdown mode returns the chip to normal operation.	—
RXD	I/O	**Receive Serial Data**. RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2, and 3.	P3.0
T1:0	I	**Timer 1:0 External Clock Inputs**. When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	P3.5:4
T2	I/O	**Timer 2 Clock Input/Output**. For the timer 2 capture mode, this signal is the external clock input. For the clock-out mode, it is the timer 2 clock output.	P1.0
T2EX	I	**Timer 2 External Input**. In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 registers to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data**. TXD outputs the shift clock in serial I/O mode 0 and transmits serial data in serial I/O modes 1, 2, and 3.	P3.1
V_{CC}	PWR	**Supply Voltage**. Connect this pin to the +5V supply voltage.	—

NOTE: †The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 7. Pin Descriptions (Continued)

Signal Name	Type	Description	Multiplexed With
V_{CC2}	PWR	**Secondary Supply Voltage 2.** This supply voltage connection is provided to reduce power supply noise. Connection of this pin to the +5V supply voltage is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility.	—
V_{PP}	I	**Programming Supply Voltage**. The programming supply voltage is applied to this pin for programming the on-chip OTPROM.	EA#
V_{SS}	GND	**Circuit Ground**. Connect this pin to ground.	—
V_{SS1}	GND	**Secondary Ground**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51BH, V_{SS1} can be unconnected without loss of compatibility.	—
V_{SS2}	GND	**Secondary Ground 2**. This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the 8XC251SB as a pin-for-pin replacement for the 8XC51FX, V_{SS2} can be unconnected without loss of compatibility.	—
WR#	O	**Write**. Write signal output to external memory. For configuration bits RD1 = RD0 = 1, WR# is strobed only for writes to locations 00:0000H–01:FFFFH. For other values of RD1:0, WR# is strobed for writes to all memory locations.	P3.6
XTAL1	I	**Input to the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	—
XTAL2	O	**Output of the On-chip, Inverting, Oscillator Amplifier**. To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	—

NOTE: †The descriptions of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the nonpage-mode chip configuration (compatible with 44-lead PLCC MCS 51 microcontrollers). If the chip is configured for page-mode operation, port 0 carries the lower address bits (A7:0), and port 2 carries the upper address bits (A15:8) and the data (D7:0).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on EA#/V_{PP} Pin to V_{SS} ..... 0 V to +13.0 V
Voltage on any other Pin to V_{SS} ..... -0.5 V to +6.5 V
I_{OL} Per I/O Pin ..... 15 mA
Power Dissipation ..... 1.5 W

NOTE:

Maximum power dissipation is based on package heat-transfer limitations, not device power consumption.

OPERATING CONDITIONS†

T_A (Ambient Temperature Under Bias):
Commercial ..... 0°C to +70°C
V_{CC} (Digital Supply Voltage) ..... 4.5 V to 5.5 V
V_{SS} ..... 0 V

NOTICE: This datasheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

DC Characteristics

Parameter values apply to all devices unless otherwise indicated.

Table 8. DC Characteristics at V_{CC} = 4.5 – 5.5 V

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	-0.5		$0.2V_{CC} - 0.1$	V	
V_{IL1}	Input Low Voltage (EA#)	0		$0.2V_{CC} - 0.3$	V	
V_{IH}	Input High Voltage (except XTAL1, RST)	$0.2V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Port 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (Note 1, Note 2)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (Note 1, Note 2)
V_{OH}	Output High Voltage (Port 1, 2, 3, ALE, PSEN#)	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$			V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA (Note 3)

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   - port 0: 26 mA
   - ports 1–3: 15 mA

   Maximum Total I_{OL} for All Output Pins: 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25° C and are not guaranteed.

Table 8. DC Characteristics at V_{CC} = 4.5 – 5.5 V (Continued)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Address)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{OH2}	Output High Voltage (Port 2 in External Address during Page Mode)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
I_{IL}	Logical 0 Input Current (Port 1, 2, 3)			-50	µA	VIN = 0.45 V
I_{LI}	Input Leakage Current (Port 0)			+/-10	µA	0.45 < VIN < V_{CC}
I_{TL}	Logical 1–to–0 Transition Current (Port 1, 2, 3)			-650	µA	VIN = 2.0 V
R_{RST}	RST Pulldown Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10 (Note 4)		pF	F_{OSC} = 16 MHz T_A = 25 °C
I_{PD}	Powerdown Current		10 (Note 4)	75	µA	
I_{DL}	Idle Mode Current		10 (Note 4)	20	mA	F_{OSC} = 16 MHz
I_{CC}	Operating Current		45 (Note 4)	80	mA	F_{OSC} = 16 MHz

NOTES:

1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:
   port 0 26 mA
   ports 1–3 15 mA

   Maximum Total I_{OL} for All Output Pins 71 mA

   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{CC} = 5.0, T_A = 25° C and are not guaranteed.

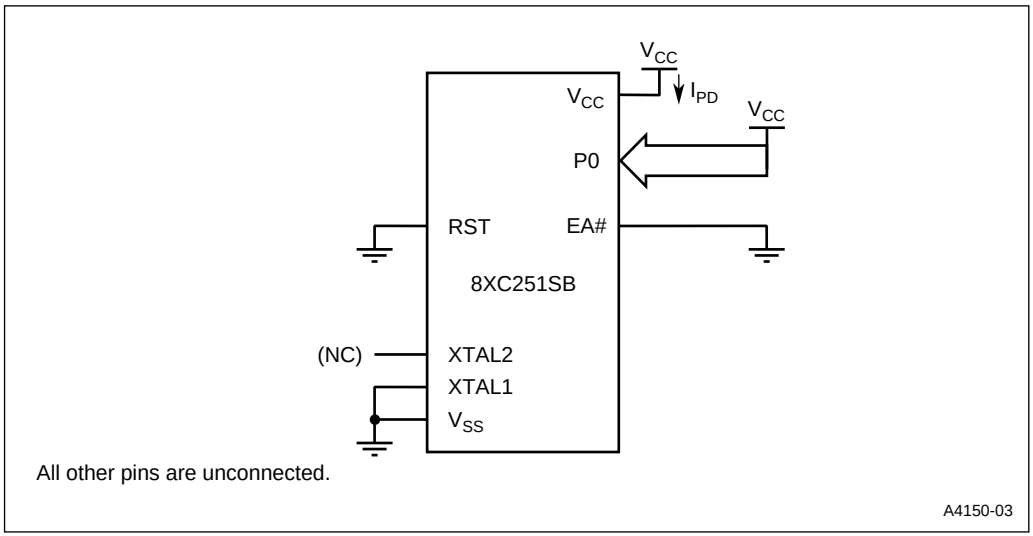


Figure 4. I_{PD} Test Condition, Powerdown Mode, V_{CC} = 2.0 – 5.5V.

AC Characteristics

Table 9 lists AC timing parameters for the 8XC251SB and 8XC251SB-16 with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and/or by extending ALE. In the table, Notes 3 and 5 mark parameters affected by an ALE wait state, and Notes 4 and 5 mark parameters affected by a PSEN#/RD#/WR# wait state.

Figures 5–10 show the bus cycles with the timing parameters.

Table 9. AC Characteristics (Capacitive Loading = 50 pF)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
F_{OSC}	XTAL1 Frequency 8XC251SB 8XC251SB-16	N/A	N/A	 0 0	 12 16	MHz
T_{OSC}	$1/F_{OSC}$ 8XC251SB 8XC251SB-16	N/A	N/A	 83.3 62.5		ns
T_{LHLL}	ALE Pulse Width 8XC251SB 8XC251SB-16	 73.3 52.5		$T_{OSC} - 10$		ns (3)
T_{AVLL}	Address Valid to ALE Low 8XC251SB 8XC251SB-16	 63.3 42.5		$T_{OSC} - 20$		ns (3)
T_{LLAX}	Address Hold after ALE Low 8XC251SB 8XC251SB-16	 63.3 42.5		$T_{OSC} - 20$		ns
T_{RLRH} (2)	RD# or PSEN# Pulse Width 8XC251SB 8XC251SB-16	 65.3 44.5		$T_{OSC} - 18$		ns (4)
T_{WLWH}	WR# Pulse Width 8XC251SB 8XC251SB-16	 65.3 44.5		$T_{OSC} - 18$		ns (4)
T_{LLRL} (2)	ALE Low to RD# or PSEN# Low 8XC251SB 8XC251SB-16	 73.3 52.5		$T_{OSC} - 10$		ns
T_{LHAX}	ALE High to Address Hold 8XC251SB 8XC251SB-16	 146.6 105		$2T_{OSC} - 20$		ns (3)
T_{RLDV} (2)	RD# or PSEN# Low to Valid Data/Instruct. In 8XC251SB 8XC251SB-16		 33.3 12.5		$T_{OSC} - 50$	ns (4)

NOTES:
1. 12 MHz for 8XC251SB and 16 MHz for 8XC251SB-16.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
5. If wait states are added as described in both Note 4 and Note 3, add a total of $4T_{OSC}$.
6. "Typical" specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{RHDX} (2)	Data/Instruct. Hold After RD# or PSEN# High	0		0		ns
T_{RLAZ} (2)	RD#/PSEN# Low to Address Float	Typ.=0 (6)	2	Typ. = 0 (6)	2	ns
T_{RHDZ} (2)	Data/Instruct. Float After RD# or PSEN# High 8XC251SB 8XC251SB-16		 63.3 42.5		T_{OSC} – 20	ns
T_{RHLH1}	RD#/PSEN# High to ALE High (Instruction) 8XC251SB 8XC251SB-16	 68.3 47.5		T_{OSC} – 15		ns
T_{RHLH2}	RD#/PSEN# High to ALE High (Data) 8XC251SB 8XC251SB-16	 234.9 172.5		$3T_{osc}$ – 15		ns
T_{WHLH}	WR# High to ALE High 8XC251SB 8XC251SB-16	 234.9 172.5		$3T_{OSC}$ – 15		ns
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In 8XC251SB (3) 8XC251SB-16 (3)		 189.9 127.5		$3T_{OSC}$ – 60	ns (3,4,5)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In 8XC251SB (3) 8XC251SB-16 (3)		 273.2 190		$4T_{OSC}$ – 60	ns (3,4,5)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In 8XC251SB 8XC251SB-16		 106.6 65		$2T_{OSC}$ – 60	ns
T_{AVRL} (2)	Address Valid to RD#/PSEN# Low 8XC251SB 8XC251SB-16	 142.6 101		$2T_{OSC}$– 24		ns (3)
T_{AVWL1}	Address (P0) Valid to WR# Low 8XC251SB 8XC251SB-16	 142.6 101		$2T_{OSC}$ – 24		ns (3)
T_{AVWL2}	Address (P2) Valid to WR# Low 8XC251SB 8XC251SB-16	 219.9 157.5		$3T_{OSC}$ – 30		ns (3)

NOTES:
1. 12 MHz for 8XC251SB and 16 MHz for 8XC251SB-16.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
5. If wait states are added as described in both Note 4 and Note 3, add a total of $4T_{OSC}$.
6. "Typical" specifications are untested and not guaranteed.

Table 9. AC Characteristics (Capacitive Loading = 50 pF) (Continued)

Symbol	Parameter	@ Max F_{osc} (1)		F_{osc} Variable		Units
		Min	Max	Min	Max	
T_{WHQX}	Data Hold after WR# High 8XC251SB 8XC251SB-16	 63.3 42.5		$T_{OSC} - 20$		ns
T_{QVWH}	Data Valid to WR# High 8XC251SB 8XC251SB-16	 58.3 37.5		$T_{OSC} - 25$		ns (4)
T_{WHAX}	WR# High to Address Hold 8XC251SB 8XC251SB-16	 146.6 105		$2T_{OSC} - 20$		ns

NOTES:
1. 12 MHz for 8XC251SB and 16 MHz for 8XC251SB-16.
2. Specifications for PSEN# are identical to those for RD#.
3. If a wait state is added by extending ALE, add $2T_{OSC}$.
4. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
5. If wait states are added as described in both Note 4 and Note 3, add a total of $4T_{OSC}$.
6. “Typical” specifications are untested and not guaranteed.

SYSTEM BUS TIMINGS

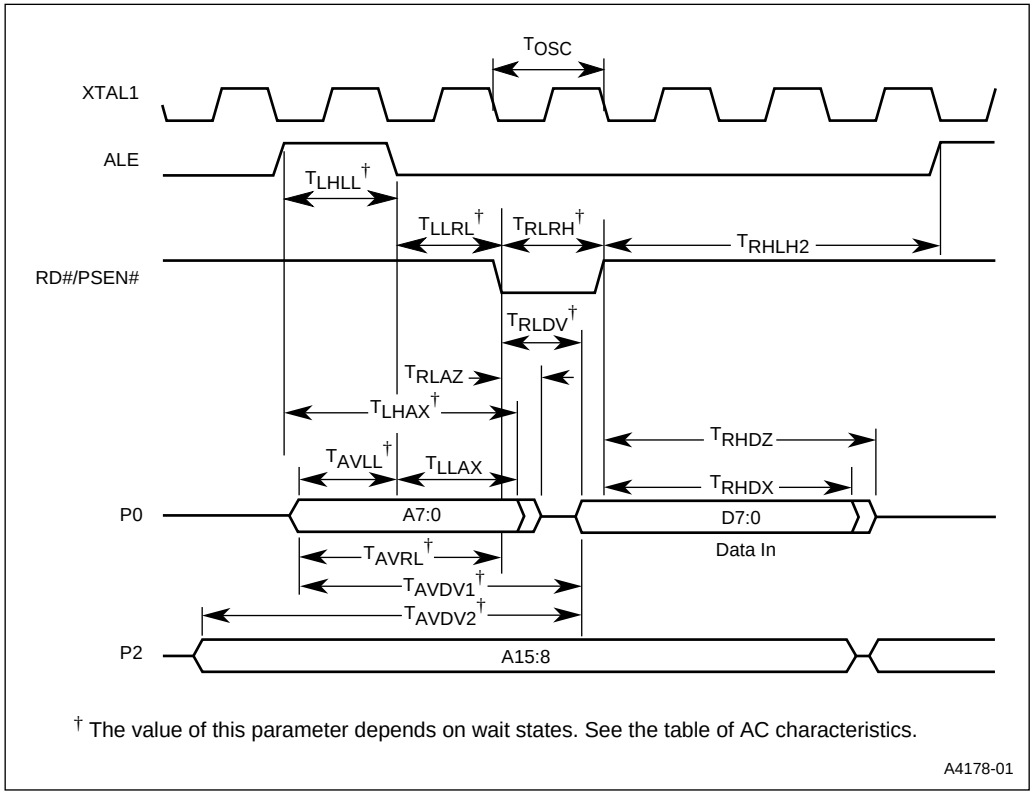
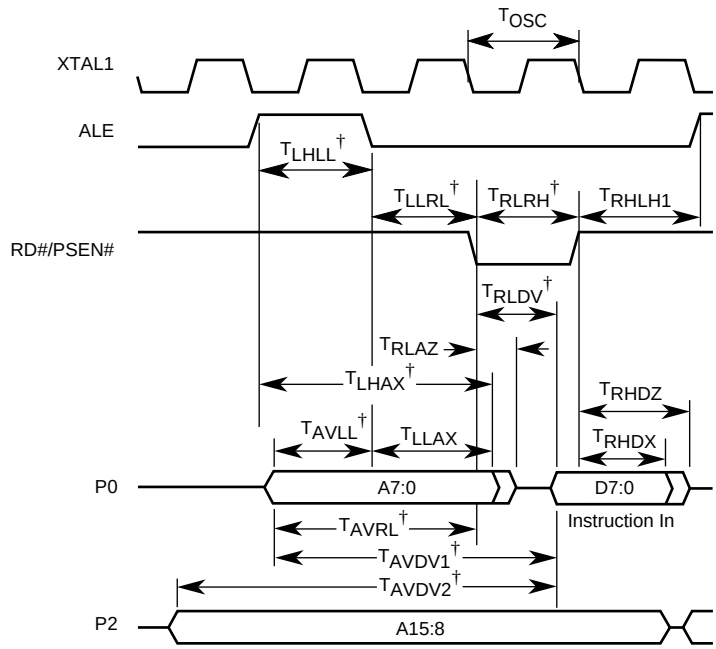


Figure 5. External Read Data Bus Cycle in Nonpage Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

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Figure 6. External Instruction Bus Cycle in Nonpage Mode

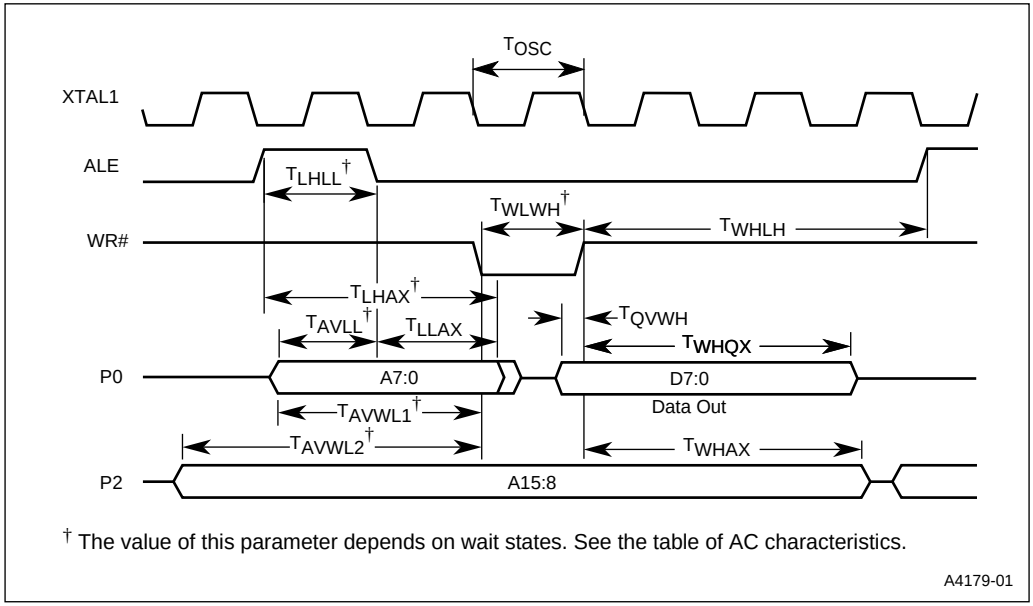


Figure 7. External Write Data Bus Cycle in Nonpage Mode

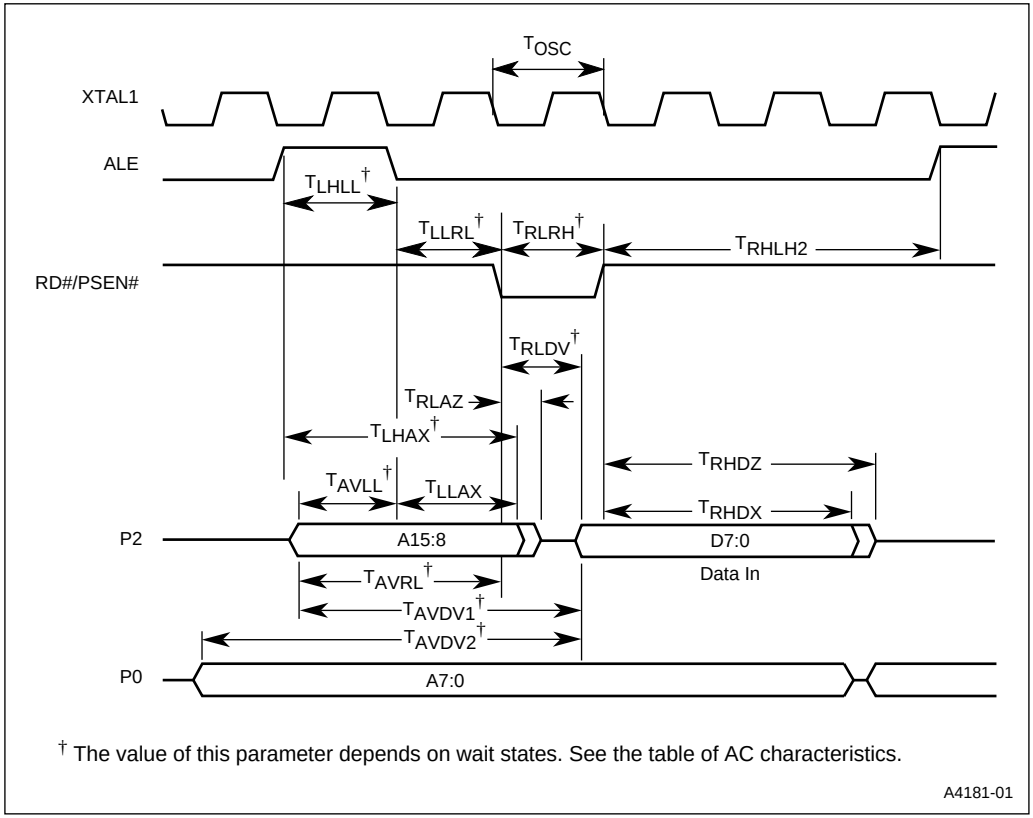


Figure 8. External Read Data Bus Cycle in Page Mode

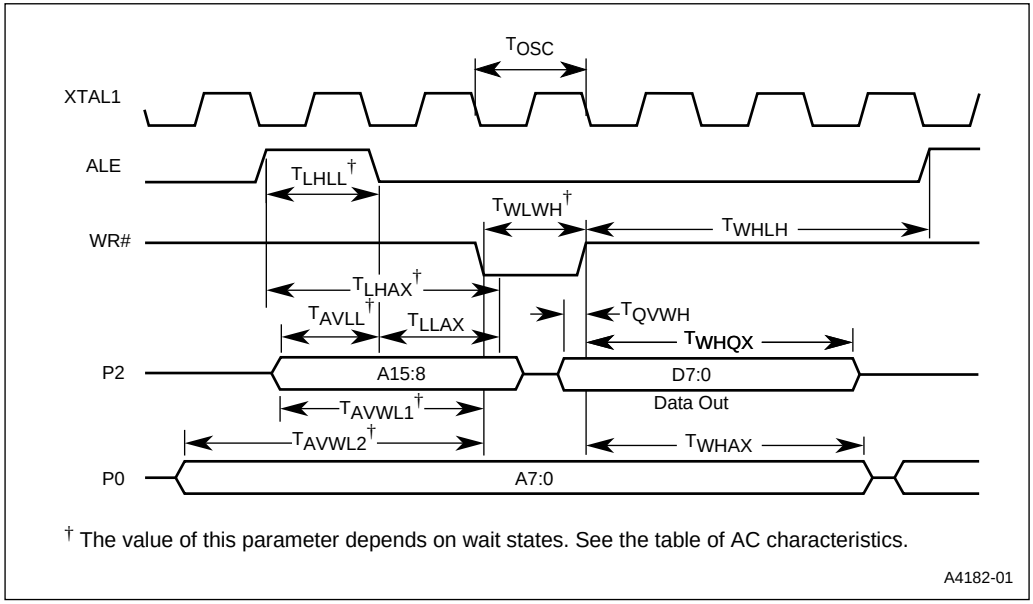
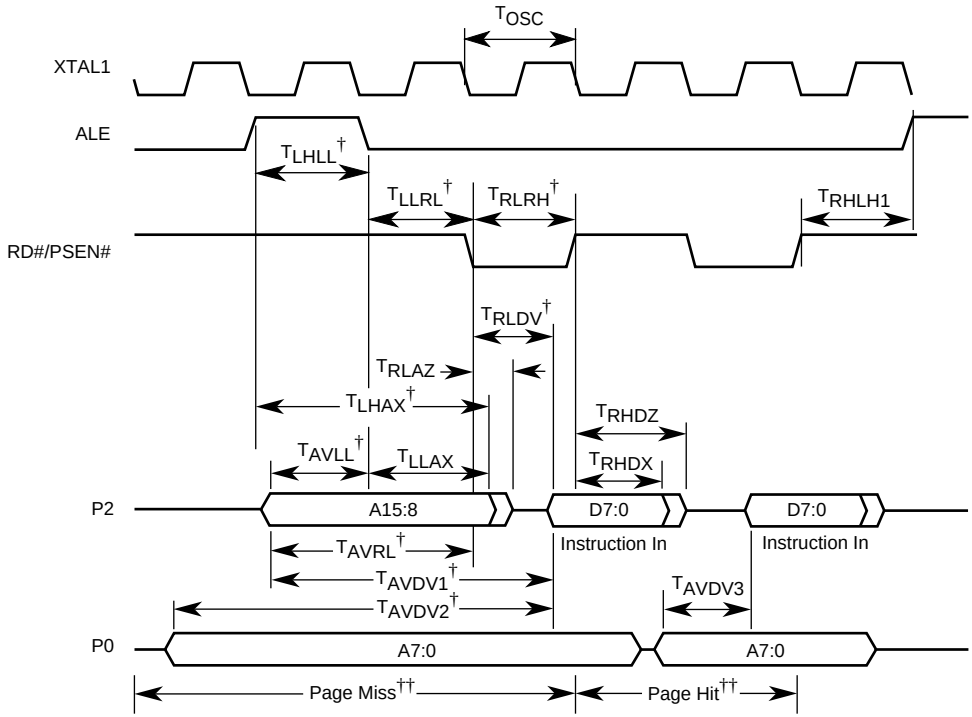


Figure 9. External Write Data Bus Cycle in Page Mode



† The value of this parameter depends on wait states. See the table of AC characteristics.

†† A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).

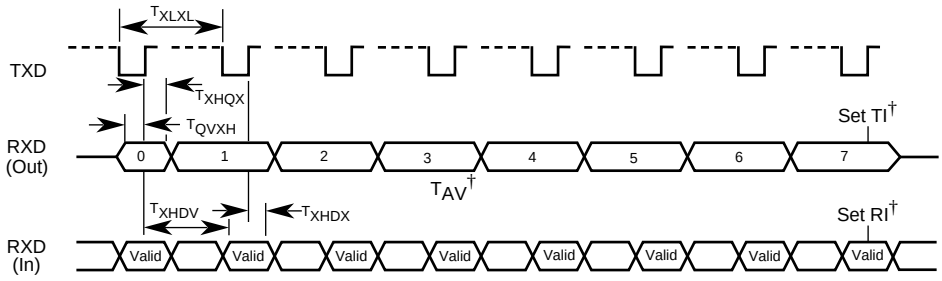
A4183-01

Figure 10. External Instruction Bus Cycle in Page Mode

AC Characteristics — Serial Port, Shift Register Mode

Table 10. Serial Port Timing — Shift Register Mode

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Cycle Time	$12T_{OSC}$		ns
T_{QVSH}	Output Data Setup to Clock Rising Edge	$10T_{OSC} - 133$		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	$2T_{OSC} - 117$		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		$10T_{OSC} - 133$	ns



†TI and RI are set during S1P1 of the peripheral cycle following the shift of the eighth bit.

A2592-02

Figure 11. Serial Port Waveform — Shift Register Mode

External Clock Drive

Table 11. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency (F_{OSC})		16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		10	ns
T_{CHCL}	Fall Time		10	ns

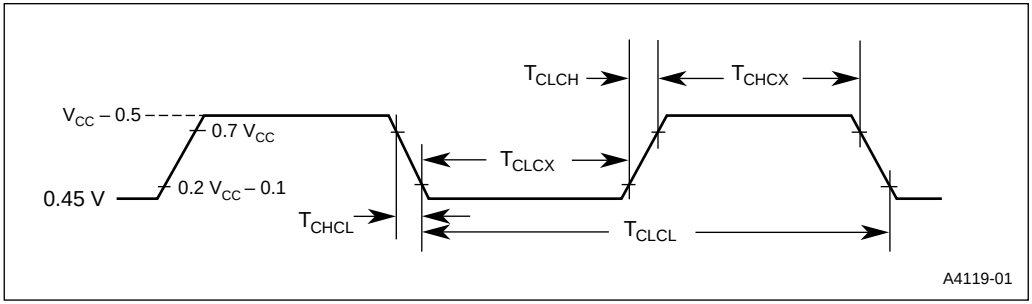


Figure 12. External Clock Drive Waveforms

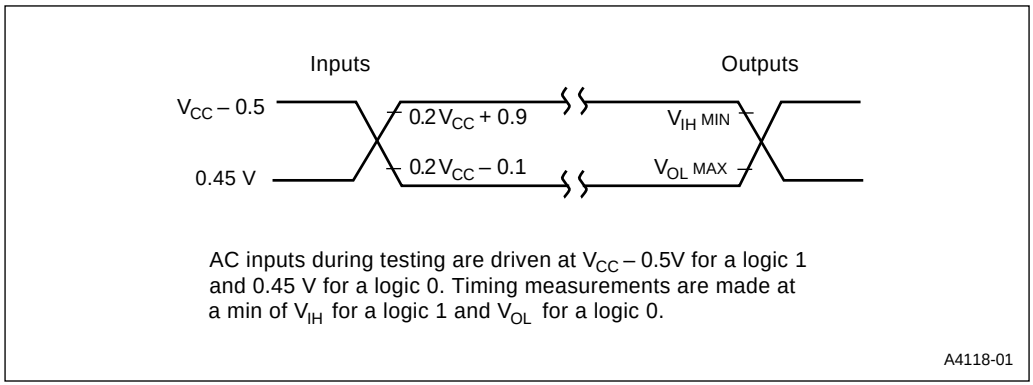
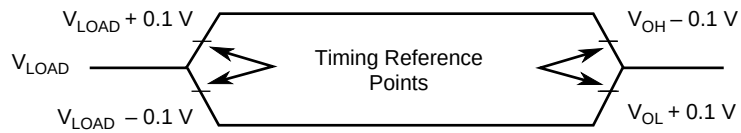


Figure 13. AC Testing Input, Output Waveforms



For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

A4117-01

Figure 14. Float Waveforms

PROGRAMMING AND VERIFYING NONVOLATILE MEMORY

The 8XC251SB has several areas of nonvolatile memory that can be programmed and/or verified: on-chip code memory (16 Kbytes), configuration bytes (2 bytes), lock bits (3 bits), encryption array (128 bytes), and signature bytes (3 bytes). The *8XC251SB User's Manual* (Order Number: 272617) provides procedures for programming and verifying the nonvolatile memory.

Figure 15 shows the setup for programming and/or verifying the nonvolatile memory. Table 12 lists the programming and verification operations and indicates which operations apply to the three versions of the 8XC251SB. It also specifies the signals on the programming input (PROG#) and the ports. The OTPROM/ROM mode (port 0) specifies the operation (program or verify) and the base address of the memory area. The addresses (ports 1 and 3) are relative to the base address. (The on-chip memory is at locations FF:0000H–FF:3FFFH of the memory address space. The other areas of the OTPROM/ROM are outside the memory address space and are accessible only during programming and verification.)

Configuration bytes CONFIG0 and CONFIG1 (Figures 16 and 17) define the configuration bits. Table 13 lists values of configuration bits for the 80C251SB.

Figure shows the waveforms for the programming and verification cycles, and Table 13 lists the timing specifications. The signature bytes of the 83C251SB and 87C251SB are factory programmed. Table 14 lists the addresses and the contents of the signature bytes.

NOTE

The V_{PP} source in Figure 15 must be well regulated and free of glitches. The voltage on the V_{PP} pin must not exceed the specified maximum, even under transient conditions.

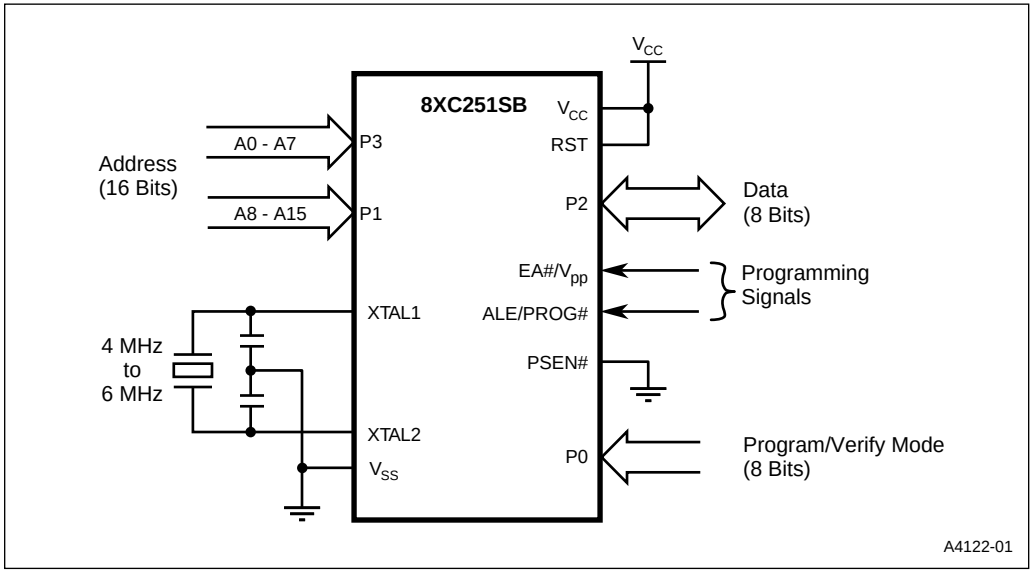


Figure 15. Setup for Programming and Verifying Nonvolatile Memory

Table 12. Programming and Verification Modes

Mode	8XC251SB			PROG#	P0	P2	Addresses P1 (high), P3 (low)	Notes
	X = 7	X = 3	X = 0					
Program on-chip code memory	Y			5 Pulses	68H	Data	0000H–3FFFH	1
Verify on-chip code memory	Y	Y		High	28H	Data	0000H–3FFFH	
Program configuration bytes	Y			5 Pulses	69H	Data	0080H–0083H	1, 2
Verify configuration bytes	Y	Y	Y	High	29H	Data	0080H–0083H	
Program lock bits	Y			25 Pulses	6BH	XX	0001H–0003H	1, 3
Verify lock bits	Y	Y		High	2BH	Data	0000H	4
Program encryption array	Y			25 Pulses	6CH	Data	0000H–007FH	1
Verify signature bytes	Y	Y		High	29H	Data	0030H, 0031H, 0060H	

NOTES:
1. The PROG# pulse waveform is shown in Figure .
2. The 8XC251SB uses only 2 bytes: 0080H and 0081H.
3. When programming the lock bits, the data bits on port 2 are don't care. Identify the lock bits with the address as follows: LB3 - 0003H, LB2 - 0002H, LB1 - 0001H
4. The three lock bits are verified in a single operation. The states of the lock bits appear simultaneously at port 2 as follows: LB3 - P2.3, LB2 - P2.2. LB1 - P2.1. High = programmed.

CONFIG0

7							0
—	—	WSA	XALE	RD1	RD0	PAGE	SRC

Bit Number	Bit Mnemonic	Function
7:6	—	Reserved; set these bits when writing to CONFIG0.
5	WSA	Wait State A: Clear this bit to generate one external wait state for memory regions 00:, FE:, and FF:. Set this bit for no wait states for these regions.
4	XALE	Extend Ale: If this bit is set, the time of the ALE pulse is T_{OSC}. Clearing this bit extends the time of the ALE pulse from T_{OSC} to $3T_{OSC}$, which adds one external wait state.
3:2	RD1, RD0	RD# and PSEN# Function Select: RD1 RD0 RD# Range PSEN# Range Features 0 0 Reserved Reserved Reserved 0 1 RD# = A16 All addresses 128-Kbyte External Address Space 1 0 P3.7 only All addresses One additional port pin 1 1 ≤ 7F:FFFFH ≥ 80:0000H Compatible with MCS 51 microcontrollers
1	PAGE	Page Mode Select: Clear this bit for page-mode (A15:8/D7:0 on P2, and A7:0 on P0). Set this bit for nonpage-mode (A15:8 on P2, and A7:0/D7:0 on P0 (compatible with 44-lead PLCC MCS 51 microcontrollers)).
0	SRC	Source Mode/Binary Mode Select: Set this bit for source mode. Clear this bit for binary mode (binary-code compatible with MCS 51 microcontrollers).

Figure 16. Configuration Byte 0

CONFIG1

7							0
—	—	—	INTR	WSB	—	—	EMAP

Bit Number	Bit Mnemonic	Function
7:5	—	Reserved; set these bits when writing to CONFIG1.
4	INTR	Interrupt Mode: If this bit is set, interrupts push 4 bytes onto the stack (the 3 bytes of the PC register and the PSW1 register). If this byte is clear, interrupts push 2 bytes onto the stack (the 2 lower bytes of the PC register).
3	WSB	Wait State B: Clear this bit to generate one external wait state for memory region 01:. Set this bit for no wait states for region 01:.
2:1		Reserved; set these bits when writing to CONFIG1.
0	EMAP	EPROM MAP: Clearing this bit maps the upper 8 Kbytes of on-chip code memory (FF:2000H–FF:3FFFH) to 00:E000H–00:FFFFH. If this bit is set, the upper 8 Kbytes of on-chip code memory are mapped only to FF:2000H–FF:3FFFH.

Figure 17. Configuration Byte 1

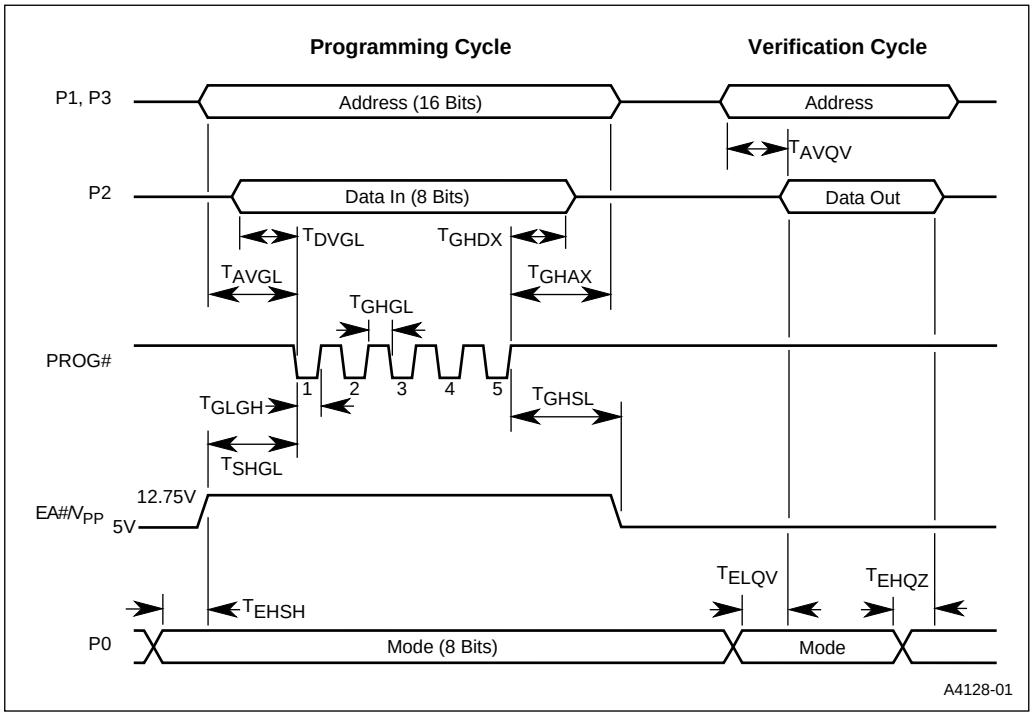


Figure 18. Timing for Programming and Verification of Nonvolatile Memory

Table 13. Nonvolatile Memory Programming and Verification Characteristics at T_A = 21 – 27 °C, V_{CC} = 5 V, and V_{SS} = 0 V

Symbol	Definition	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
F_{OSC}	Oscillator Frequency	4.0	6.0	MHz
T_{AVGL}	Address Setup to PROG# Low	$48T_{OSC}$		
T_{GHAX}	Address Hold after PROG#	$48T_{OSC}$		
T_{DVGL}	Data Setup to PROG# Low	$48T_{OSC}$		
T_{GHDX}	Data Hold after PROG#	$48T_{OSC}$		
T_{EHSH}	ENABLE High to V_{PP}	$48T_{OSC}$		
T_{SHGL}	V_{PP} Setup to PROG# Low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{GLGH}	PROG# Width	90	110	µs
T_{AVQV}	Address to Data Valid		$48T_{OSC}$	
T_{ELQV}	ENABLE Low to Data Valid		$48T_{OSC}$	
T_{EHQZ}	Data Float after ENABLE	0	$48T_{OSC}$	
T_{GHGL}	PROG# High to PROG# Low	10		µs

NOTE: Notation for timing parameters:

A = Address D = Data E = Enable G = PROG# H = High L = Low

Q = Data out S = Supply (V_{PP}) V = Valid X = No Longer Valid Z = Floating

Table 14. Contents of the Signature Bytes

Device	Address		
	30H	31H	60H
83C251SB	89H	40H	7BH
87C251SB	89H	40H	FBH

DATASHEET REVISION HISTORY

The following differences exist between the -001 revision and this -002 revision of the 8XC251SB datasheet:

1. All EXPRESS temperature information is removed.
2. The term “EC1” (PCA External Clock Input) in Table 7 is correctly stated as “ECI”.
3. The description of bits RD0 and RD1 in configuration byte CONFIG1 (Table 7) correctly identifies states for 00 and 11 and matches other datasheet and user manual information.
4. The WR# (Write) bus control signal description is added to Table 7.
5. The V_{OH2} description is included in Table 8.
6. The RST (reset) resistor is correctly stated as a “pulldown“ in Table 8.
7. The I_{PD}, I_{DL}, I_{CC}, T_{RLDV}, T_{AVDV1}, T_{AVDV2}, T_{AVDV3} Maximum specifications are revised.
8. An I_{PD} test condition replaces the I_{CC} test condition in Figure 4 and its caption.
9. T_{RLRH}, T_{WLWH}, T_{LHAX}, $T_{AVRL,}$ T_{QVWH} Minumum specifications are revised.
10. T_{LHRL}, T_{RHLH} are deleted.
11. T_{LLRL}, T_{RHLH1}, T_{RHLH2} are new.
12. T_{RLAZ} is revised.
13. T_{AVWL1} is revised.
14. All timing diagrams relative to the foregoing changes are redrawn.
15. The Serial Port Waveform — Shift Register Mode figure is redrawn to indicate Set TI and Set RI.
16. Table 13, “Configuration Bit Values for 80C251SB and 80C251SB-16,” is deleted.
17. The 12 MHz test condition for C_{IO} is now 16 MHz.

FUNCTIONAL DEVIATIONS

This section describes the functional deviations associated with the 8XC251SB -002 datasheet.

1. Certain instructions (listed below) result in register values incorrectly affecting the Negative Flag (N) of PSW1. These register values should set or clear the Negative Flag based on the value of result bit 15. The 8XC251SB ALU currently sets and clears the Negative Flag based on result bit seven when using these specific instructions. Follow affected instructions with an ANL WRj,WRj operation. This forces the ALU Negative Flag to operate on the value of result bit 15. The net impact is the additional ANL instruction time to gain correct Negative Flag results. The following Instructions are affected by this deviation:

SRL WRj
SRA WRj
SLL WRj
INC WRj,#short
DEC WRj,#short

2. WSb in the CONFIG1 configuration register controls the number of wait states for MOVX instructions in memory locations 01:0000H through 01:FFFFH. This includes both MOVX @DPTR as well as the MOVX @Ri instruction. The device currently uses WSa in the CONFIG0 configuration register for the MOVX @Ri instruction. If possible, configure both WSa and WSb to the same value. This results in identical wait-state operation for both MOVX @DPTR and MOVX @Ri. If the two CONFIGx bits must be configured differently, restrict the use of MOVX commands to the MOVX @DPTR format.

3. Use of EJMP instructions for extended jumps between 64-Kbyte regions do not result in the correct destination. Do not use the EJMP instruction.

4. Jump instructions with an address range of +127/-128 do not jump across the FF:XXXXH to FE:XXXXH 64-Kbyte region boundary. Issuing a jump instruction within range of this boundary results in a destination within the same FF:XXXXH region. Do not use jump instructions to cross this memory boundary. All +127/-128 jump instructions issued across other 64-Kbyte region boundaries operate as described. The affected instructions for the FF:XXXXH to FE:XXXXH region jump deviation are SJMP, CJNE, DJNZ, JB, JBC, JC, JE, JG, JLE, JNB, JNC, JNE, JNZ, JSG, JSGE, JSL, JSLE, and JZ.