82371FB PCI ISA IDE Xcelerator (PIIX)

Timing Specification

Datasheet Addendum

- Bridge Between the PCI Bus and the ISA Bus
- PCI and ISA Master/Slave Interface
  - —PCI from 25–33 MHz
  - —ISA from 7.5–8.33 MHz
  - —5 ISA Slots
- Fast IDE Interface
  - —Supports PIO and Bus Master IDE
  - —Supports up to Mode 4 Timings
  - —Transfer Rates to 22 Mbytes/s
  - —8 x 32-Bit Buffer for Bus Master IDE PCI Burst Transfers
- Plug-n-Play Port for Motherboard Devices
  - —1 Programmable Chip Select
- Steerable PCI Interrupts for PCI Device Plug-n-Play
- Functionality of One 82C54 Timer
  - —System Timer; Refresh Request; Speaker Tone Output
- Two 82C59 Interrupt Controller Functions
  - —14 Interrupts Supported
  - —Independently Programmable for Edge/ Level Sensitivity
- Enhanced DMA Functions
  - —Two 8237 DMA Controllers
  - —Fast Type F DMA
  - —Compatible DMA Transfers
  - —7 Independently Programmable Channels
- X-Bus Peripheral Support
  - —Chip Select Decode
  - —Controls Lower X-Bus Data Byte Transceiver
- System Power Management (Intel SMM Support)
  - —Programmable System Management Interrupt (SMI)—Hardware Events, Software Events, EXTSMI#
  - —Programmable CPU Clock Control (STPCLK#)
  - —Fast On/Off Mode
- Non-Maskable Interrupts (NMI)
  - —PCI System Error Reporting
- NAND Tree for Board-Level ATE Testing
- 208-Pin QFP

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 430FX PCIset. Please refer to the standard 430FX datasheet (order number 290550) for 82371FB (PIIX) product information and specifications not found in this document.

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Datasheet Addendum

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1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Maximum Rating
Case Temperature under Bias	0° C to + 85° C
Storage Temperature	– 55° C to + 150° C
Voltage on Any Pin with Respect to Ground	– 0.3 V to V_{CC} + 0.3 V
Supply Voltage with Respect to V_{SS}	– 0.3 V to + 6.5 V
Maximum Power Dissipation	1.0 W

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operating beyond the Operating Conditions is not recommended and extended exposure beyond Operating Conditions may affect reliability.

1.2 Thermal Characteristics

The 82371FB PIIX is designed for operation at case temperatures between 0° C and 85° C. The thermal resistances of the package are given in Table 1.

Table 1. Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{JA} (°C/Watt)	34.5	26.1
θ_{JC} (°C/Watt)	12.0	

1.3 DC Characteristics

Table 2. 82371FB DC Characteristics

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	– 0.3	0.8	V	
V_{IH1}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{T1-}	Schmitt Trigger Threshold Voltage, Falling Edge	0.7	1.35	V	V_{CC}=5 V
V_{T1+}	Schmitt Trigger Threshold Voltage, Rising Edge	1.4	2.2	V	1, V_{CC}=5 V
V_{H1}	Hysteresis Voltage	0.3	1.2	V	1, V_{CC}=5 V
V_{OL1}	Output Low Voltage		0.5	V	2,3,4,5
V_{OH1}	Output High Voltage	V_{CC} – 0.7		V	2,3,4,5
I_{OL1}	Output Low Current		2	mA	2
I_{OH1}	Output High Current	– 1		mA	2
I_{OL2}	Output Low Current		12	mA	3
I_{OH2}	Output High Current	– 3		mA	3
I_{OL3}	Output Low Current		3	mA	4
I_{OH3}	Output High Current	– 2		mA	4
I_{OL4}	Output Low Current		6	mA	5
I_{OH4}	Output High Current	– 2		mA	5
I_{LI1}	Input Leakage Current		± 1	µA	All, except I_{LI2} and I_{LI3}
I_{LI2}	Input Leakage Current		± 300	µA	6, T_C
I_{LI3}	Input Leakage Current		± 250	µA	6, EXTSMI#, TESTIN#
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz
I_{CC}	V_{CC} Supply Current		250	mA	V_{CC} = 5 V

NOTES:

1. V_{T1-}, V_{T1+} and VH1 apply to the following signals: IRQx, IOCHK#, ZEROWS#, PWROK.
2. I_{OL1}, I_{OH1} apply to the following signals (V_{OL1}, pertains to the I_{OL1}, condition and V_{OH1} pertains to the I_{OH1} condition): DD[15:0], PHOLD#, DIOW#, DIOR#,DDAK[1:0]#, SPKR, IGNNE#, INTR, SMI#, STPCLK#, CPURST#,INIT, NMI,TC, DREQ[7:5,3:0], DACK[7:5,3:0]#, REFRESH#, DDRQ[1:0], SDIR, SOE#, BIOSCS#, RTCCS#, KBCS#, XOE#, XDIR, MDRQ[1:0], MDAK[1:0], MIRQ[1:0], RTCALE, PIRQ[A:D].
3. I_{OL2}, I_{OH2} apply to the following signals (V_{OL1}, pertains to the I_{OL2}, condition and V_{OH1} pertains to the I_{OH2} condition): SYSCLK, SD[15:0], IOCHRDY, SMEMR#, AEN, SMEMW#, IOR#, IOW#, RSTDRV, SA[7:0], BALE, MEMCS16#, LA[23:17], MEMR#, MEMW#,
4. I_{OL3}, I_{OH3} apply to the following signals (V_{OL1}, pertains to the I_{OL2}, condition and V_{OH1} pertains to the I_{OH2} condition): AD[31:0], C/BE[3:0]#, PCIRST#
5. I_{OL4}, I_{OH4} apply to the following signals (V_{OL1}, pertains to the I_{OL2}, condition and V_{OH1} pertains to the I_{OH2} condition): FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR.
6. These signals have weak internal pull-up resistors.

1.4 AC Characteristics

This section provides the AC parameters. Unless otherwise specified, the units for timing parameters are nanoseconds.

Table 3. Clock/Reset Timings

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
PCI Clock Timings						
	PCICLK					
t1a	Period	30	40	ns		1
t1b	High Time	12		ns		1
t1c	Low Time	12		ns		1
t1c	Rise Time		3	ns		1
tt1d	Fall Time		3	ns		1
ISA Clock Timings						
	SYSCLK					
t1f	Period	120	125	ns		1
t1g	High Time	56		ns		1
t1h	Low time	56		ns		1
t1i	Rise Time		4	ns		1
t1j	Fall time		4	ns		1
Oscillator Clock Timings						
	OSC					
t1l	OSC Period	67	70	ns		1
t1m	High Time	20		ns		1
t1n	Low time	20		ns		1
Reset Timings						
t2a	CPURST, PCIRST#, RSTDRV Driven Inactive After PWROK is Driven Active High.	2		PCICLK		3
t2b	CPURST, PCIRST#, RSTDRV Active Pulse Width. Initiated via the RC Register.	1		ms		4
t2c	CPURST Valid Delay from PCICLK Rising	3	25	ns		30

Table 4. System Power Management Timings

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
	SMI#					
t3a	Valid Delay from PCICLK	2	30	ns		7
t3b	Active Pulse Width	3		PCLKIN		5
t3c	Inactive Pulse Width	4		PCLKIN		5
	EXTSMI#					
t3d	Active Pulse Width	2		PCLKIN		5
t3e	Inactive Pulse Width	4		PCLKIN		5
t3f	Valid Setup to PCICLK	10		ns		6
t3g	Valid Hold from PCICLK	2		ns		6
	STPCLK#					
t3h	Valid Delay from PCICLK	2	30	ns		30
t3i	STPCLK# Inactive Pulse Width	5		PCLKIN		5

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 1 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
PIIX as Master Timings								
	BALE							
t4a	BALE Pulse Width	50		ns	M,I/O	8,16		8, 9, 10, 11
t4b	BALE Driven Active from MEMx#, IOx# Inactive	44		ns	M,I/O	8,16		8, 9, 10, 11
	LA[23:17]							
t5a	LA[23:17] Valid Setup to BALE Inactive	150		ns	M	8,16	7	8, 9
t5b	LA[23:17] Valid Hold from BALE Inactive	26		ns	M	8,16		8, 9
t5c	LA[23:17] Valid Setup to MEMx# Active	150		ns	M	16		9
t5d	LA[23:17] Valid Setup to MEMx# Active	173		ns	M	8		8
t5e	LA[23:17] Invalid from MEMx# Active	39		ns	M	16		9
t5f	LA[23:17] Invalid from MEMx# Active	39		ns	M	8		8
	SA[19:0], SBHE#							
t6a	SA[19:0], SBHE# Valid Setup to MEMx# Active	34		ns	M	16	13,15	9
t6b	SA[19:0], SBHE# Valid Setup to IOx# Active	100		ns	I/O	16		11

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 2 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t6c	SA[19:0], SBHE# Setup to MEMx#, IOx# Active	100		ns	M,I/O	8		8
t6d	SA[19:0], SBHE# Valid Setup to BALE Inactive	37		ns	M,I/O	8,16	13,15	8, 9, 10, 11
t6e	SA[19:0], SBHE# Valid Hold from MEMx#, IOx# Inactive	46		ns	M,I/O	8,16		8, 9, 10, 11
	MEMR#, MEMW#, IOR# AND IOW#							
t7a	MEMx# Active Pulse Width (std)	225		ns	M	16		9
t7b	IOx# Active Pulse Width (std)	160		ns	I/O	16		11
t7c	MEMx# Active Pulse Width (nws)	105		ns	M	16	1	9
t7d	MEMx# or IOx# Active Pulse Width (std)	520		ns	M,I/O	8		8, 10
t7e	MEMx# or IOx# Active Pulse Width (nws)	160		ns	M,I/O	8	1	8, 10
t7f	MEMx# Inactive Pulse Width	103		ns	M	16		9
t7g	MEMx# Inactive Pulse Width	163		ns	M	8		8
t7h	IOx# Inactive Pulse Width	163		ns	I/O	8,16		10, 11
t7i	MEMx#, IOx# Driven Inactive from IOCHRDY Active	120		ns	M,I/O	8,16		8, 9, 10, 11
	SMEMR# and SMEMW#							
t8a	SMEMR# & SMEMW# Propagation Delay from MEMR# and MEMW#		16	ns	M	8,16		8, 9
	Read Data							
t9a	Read Data Driven from MEMR#, IOR# Active	0		ns	M,I/O	8,16		8, 9, 10, 11
t9b	Read Data Valid Setup to MEMR#, IOR#	24		ns	M,I/O	8,16		8, 9, 10, 11
t9c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		8, 9, 10, 11
t9d	Read Data three-stated from MEMR# and IOR# Inactive		41	ns	M,I/O	8,16		8, 9, 10, 11
	Write Data							
t10a	Write Data Valid Setup to MEMW# Active Write Data Valid Setup to IOW# Active Write Data Valid Setup to IOW# Active	– 40 – 40 +23		ns ns ns	M, I/O M, I/O M, I/O	8,16 8 16		8, 9, 10, 11
t10b	Write Data Valid Hold from MEMW#, IOW# Inactive	45		ns	M,I/O	8,16		8, 9, 10, 11
t10c	Write Data three-Stated from MEMW#, IOW# Inactive		105	ns	M,I/O	8,16		8, 9, 10, 11
t10d	Write Data Driven Valid after Read MEMR#, IOR# Inactive	41		ns	M,I/O	8,16		8, 9, 10, 11

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 3 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
	MEMCS16#							
t11a	MEMCS16# Driven Active from LA[23:17] Valid		94	ns	M	16		9
t11b	MEMCS16# Inactive from LA[23:17] Valid		91	ns	M	8		8, 9
t11c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		9
t11d	MEMCS16# Driven Active from SA[19:2] Valid		35	ns	M	16		9
	IOCS16#							
t12a	IOCS16# Driven Active from Valid SA[19:0]		123	ns	I/O	16		11
t12b	IOCS16# Inactive from Valid SA[19:0]		91	ns	I/O	8		10, 11
t12c	IOCS16# Valid Hold from SA[19:0] Invalid	0		ns	I/O	16		11
t12d	IOCS16# Driven Active from IOx Active		80	ns	I/O	16		11
	ZEROWS#							
t13a	ZEROWS# Driven Active from MEMx# Active		16	ns	M	16		9
t13b	ZEROWS# Driven Active from MEMx#, IOx# Active		80	ns	M,I/O	8		8
t13c	ZEROWS# Driven Active from LA[23:17] Valid		180	ns	M	16		9
t13d	ZEROWS# Driven Active from LA[23:17] Valid		300	ns	M	8		8
	ZEROWS#							
t13e	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		80	ns	M	16		9
t13f	ZEROWS# Driven Active from SA[19:0], SBHE# Valid		200	ns	M,I/O	8		8, 10
	AEN							
t14a	AEN Valid Setup to IOx# Driven Active	111		ns	I/O	8,16		10, 11
t14b	AEN Valid Setup to BALE Driven Inactive	111		ns	I/O	8,16		10, 11
t14c	AEN Valid Hold from IOx# Driven Inactive	41		ns	I/O	8,16		10, 11
	IOCHRDY							
t15a	IOCHRDY Driven Valid from MEMx#, IOx# Active		78	ns	M,I/O	16		9, 11
t15b	IOCHRDY Driven Valid from MEMx#, IOx# Active		366	ns	M,I/O	8		10

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 4 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t15e	IOCHRDY Inactive Pulse Width	120	15.6	µs	M,I/O	8,16		8, 10, 11
PIIX as Slave Timings								
	LA[23:17]							
t16a	LA[23:17] Valid Setup to MEMx# Active	23		ns	M	16		12
	SA[19:0],SBHE#							
t17a	SA[19:0],SBHE# Setup to MEMx# Active	23		ns	M	16		12
t17b	SA[19:0],SBHE# Setup to IOx# Active	89		ns	I/O	8		13
t17c	SA[19:0],SBHE# Valid Hold from MEMx#, IOx# Inactive	30		ns	M,I/O	8,16		12, 13
	MEMR#, MEMW#, IOR#, IOW#							
t18a	MEMx# Active Pulse Width	214		ns	M	16		12
t18b	IOx# Active Pulse Width	509		ns	I/O	8		13
t18c	MEMx# Inactive Pulse Width	92		ns	M	16		12
t18d	IOx# Inactive Pulse Width	152		ns	I/O	8		13
	Read Data							
t19a	Read Data Valid from IOCHRDY Active		69	ns	M,I/O	8,16		12, 13
t19b	Read Data Valid from IOR# Active		69	ns	I/O	8	11	13
t19c	Read Data Valid Hold from MEMR#, IOR# Inactive	0		ns	M,I/O	8,16		12, 13
t19d	Read Data three-State from MEMR#, IOR# Inactive		55	ns	M,I/O	8,16		12, 13
	Write Data							
t20a	Write Data Valid Setup to MEMW#, IOW# Active	-54		ns	M,I/O	8,16		12, 13
t20b	Write Data Valid Hold from MEMW#, IOW# Inactive	14		ns	M,I/O	8,16		12, 13
	MEMCS16#							
t21a	MEMCS16# Driven Active from Valid LA[23:17]		65	ns	M	16		12
t21b	MEMCS16# Float from Valid LA[23:17]		31	ns	M	16		12
t21c	MEMCS16# Valid Hold from LA[23:17] Invalid	0		ns	M	16		12
	IOCHRDY							
t22a	IOCHRDY Inactive from MEMx#, IOx# Active		50	ns	M,I/O	8,16		12, 13

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 5 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t22b	IOCHRDY Float from IOCHRDY Rising		85	ns	M,I/O	8,16	4	12, 13
t22c	IOCHRDY Inactive Pulse Width	120	2.5	µs	M,I/O	8,16		12, 13
Interrupt and NMI Timings								
	NMI Timing							
t23a	SERR#, IOCHK# Active to NMI Driven Active		200	ns				14
	Interrupt Timing							
t24a	IRQx, MIRQx Inactive Pulse Width	100		ns				15
ISA Bus Master Timings								
	DACK#							
t26a	DACK#, MDAKx# Inactive from DREQ Inactive	240		ns				16
	Three-Stating and Driving the Bus							
t27a	PIIX Three-States Address, Data, and Control Signals from DACK#, MDAKx# Active		30	ns				16
t27b	PIIX Drives Address, Data, and Control Signals from DACK#, MDAKx# Inactive	71		ns				16
	SMEMR# and SMEMW#							
t28a	SMEMR# and SMEMW# Active (falling edge) from MEMR# and MEMW# Active (falling edge)		25	ns				16
t28b	SMEMR# and SMEMW# Inactive (rising edge) from MEMR# and MEMW# Inactive (rising edge)		35					16
Data Swap Logic Timing (ISA Master to ISA Slave)								
t29a	SD[7:0] to SD[15:8] Propagation Delay		26	ns				17
t29b	SD[15:8] to SD[7:0] Propagation Delay		26	ns				17
t29c	PIIX Drives Data Bus from IOR#, IOW#, MEMR# or MEMW# Active		26	ns			2	17
t29d	PIIX Three-States Bus from IOR#, MEMR#, or SMEMR# Inactive	2	55	ns			2,3	17
t29e	PIIX Three-States Bus from IOW#, MEMW#, or SMEMW# Inactive	2	60	ns			2,3	17
DMA Compatible Timings								
	DREQ, MDRQ							
t30a	DREQ, MDRQx Active Hold from IOR# Active		558	ns			5	19

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 6 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t30b	DREQ, MDRQ, Active Hold from IOW# Active		315	ns			5	18
	DACK#, MDAK#							
t31a	DACK#, MDAK# Active to IOR# Active	73		ns				19
t31b	DACK#, MDAK# Active to IOW# Active	312		ns				18
t31c	DACK#, MDAK# Active Hold from IOR# Inactive	100		ns				19
t31d	DACK#, MDAK# Active Hold from IOW# Inactive	155		ns				18
	AEN and BALE							
t32a	AEN Active to IOx# Active	111		ns				18, 19
t32b	AEN and BALE Inactive from IOx# Inactive	41		ns				18, 19
	LA[23:19], SA[19:0], SBHE#							
t33a	LA[23:19],SA[19:0], SBHE# Valid Setup to MEMx# Active	99		ns				18, 19
t33b	LA[23:19],SA[19:0], SBHE# Valid Hold from MEMx# Inactive	51		ns				18, 19
	MEMR#, MEMW#, IOR#, IOW#							
t34a	IOW# and MEMW# Active Pulse Width	465		ns				18, 19
t34b	MEMR# Active Pulse Width	495		ns				18
t34c	IOR# Active Pulse Width	760		ns				19
t34d	IOW# Inactive Pulse Width (continuous)	465		ns				18
t34e	IOR# Inactive Pulse Width (continuous)	160		ns				19
t34f	IOR# Active to MEMW# Active	230		ns				19
t34g	MEMR# Active to IOW# Active	-26		ns				18
t34h	MEMR# Active Hold from IOW# Inactive	40		ns				18
t34i	IOR# Active Hold from MEMW# Inactive	40		ns				19
t34j	MEMx# Active Hold from IOCHRDY Active	120		ns				18, 19
	SMEMR# & SMEMW#							
t35a	SMEMR# & SMEMW# Valid from MEMR# and MEMW# Valid		15	ns				18, 19
	Read Data							
t36a	Read Data Valid from IOR# Active		237	ns				19

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 7 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t36b	Read Data Valid Hold from IOR# Inactive	0		ns				19
t36c	Read Data Float from IOR# Inactive		61	ns				19
	Write Data							
t37a	Write Data Valid Setup to IOW# Inactive	225		ns				18
t37b	Write Data Valid Hold from IOW# Inactive	36		ns				18
Data Swap Logic Timing (ISA to ISA Transaction)								
t38a	SD[7:0] to SD[15:8] Propagation Delay		26	ns				20
t38b	SD[15:8] to SD[7:0] Propagation Delay		26	ns				20
t38c	PIIX Drives Data Bus from IOR# or MEMR# Active		26	ns			2	20
t38d	PIIX Three-States Bus from IOR# or MEMR# Inactive		55	ns			2	20
	TC							
t39a	TC Active Setup to IOx# Inactive	511		ns			6	18, 19
t39b	TC Active Hold from IOx# Inactive	71		ns			6	18, 19
t39h	TC Pulse Width	700		ns				18, 19
	IOCHRDY							
t40b	IOCHRDY Valid from MEMx# Active		315	ns				18, 19
t40c	IOCHRDY Inactive Pulse Width	125		ns				18, 19
DMA Type "F" Timings								
	DREQ, MDRQx							
t55a	DREQ, MDRQx Active Hold from IOR# Active		82	ns			5, 16	21
t55b	DREQ, MDRQx Active Hold from IOW# Active		82	ns			5, 16	21
	DACK#, MDAKx#							
t56a	DACK#, MDAKx# Active to IOR# Active	77		ns			16	21
t56b	DACK#, MDAKx# Active to IOW# Active	77		ns			16	21
t56c	DACK#, MDAKx# Active Hold from IOR# Inactive	30		ns			16	21
t56d	DACK#, MDAKx# Active Hold from IOW# Inactive	30		ns			16	21
	AEN and BALE							
t57a	AEN Active to IOx# Active	111		ns				21

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 8 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t57b	AEN and BALE Inactive from IOx# Inactive	41		ns				21
	IOR# and IOW#							
t58a	IOR# Active Pulse Width	110		ns				21
t58b	IOW# Active Pulse Width	110		ns				21
t58c	IOR# Inactive Pulse Width (Continuous)	115		ns				21
t58d	IOW# Inactive Pulse Width (Continuous)	115		ns				21
	Read Data							
t59a	Read Data Valid from IOR# Active		96	ns				21
t59b	Read Data Valid Hold from IOR# Inactive	2		ns				21
t59c	Read Data Float from IOR# Inactive		61	ns				21
	Write Data							
t60a	Write Data Valid Setup to IOW# Inactive	73		ns				21
t60b	Write Data Valid Hold from IOW# Inactive	31		ns				21
	TC							
t61a	TC Active Setup to IOR# Inactive	40		ns			6	21
t61b	TC Active Setup to IOW# Inactive	40		ns			6	21
t61c	TC Active Hold from IOx# Inactive	0		ns			6	21
ISA Refresh Timings								
	REFRESH#							
t62a	REFRESH# Active Setup to MEMR# Active	120		ns				22, 23
t62b	REFRESH# Active Hold from MEMR# Inactive	31	218	ns				22, 23
t62c	REFRESH# Driven Active to SA[15:0] Valid	11		ns				22, 23
t62d	REFRESH# Active Hold from SA[15:0] Invalid	11		ns				22, 23
	AEN							
t63a	AEN Driven Active to MEMR# Active	11		ns				22, 23
t63b	AEN Hold from MEMR# Inactive	11		ns				22, 23
	SA[15:0]							
t64a	SA[15:0] Valid Setup to MEMR# Active	72		ns				22, 23

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 9 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
t64b	SA[15:0] Valid Hold from MEMR# Inactive	35		ns				22, 23
t64c	SA[15:0] Valid Float from MEMR# Inactive	46	120	ns			8	23
	MEMR#, SMEMR#							
t65a	MEMR# Active Pulse Width	225		ns				22, 23
t65b	MEMR# Three-state from MEMR# Inactive	36	120	ns				22, 23
t65c	MEMR# Driven Inactive from IOCHRDY Active	120		ns				22, 23
t65d	SMEMR# Propagation Delay from MEMR#		25	ns				22, 23
	IOCHRDY							
t66a	IOCHRDY Inactive from MEMR# Active		76	ns				22, 23
t66b	IOCHRDY Valid from MEMR# Active		76	ns				22, 23
t66c	IOCHRDY Active to Inactive	120		ns				22, 23
	PIIX Driving Bus From REFRESH#							
t67a	PIIX Drives Control and Address from REFRESH# Active	5		ns			8	23
PIIX and ISA Master Accesses to the X-Bus								
	BIOSCS#, KBCCS#, RTCCS#, AND PCS#							
t68a	CS# Driven Active from SA[19:0], LA[23:17] Valid		35	ns				24
t68b	CS# Driven Inactive from SA[16:0], LA[23:17] Invalid		35	ns				24
	XDIR# and XOE#							
t69a	XDIR# Active from IOR#, MEMR# Active - PCI-Initiated Access - ISA-Initiated Access		 25 30	 ns ns				24
t69c	XDIR# Active Setup to XOE# Active	0	8	ns				24
t69d	XOE# Inactive from IOx#, MEMx# Inactive	35	62	ns			9	24
t69e	XDIR# Inactive from IOR#, MEMR# Inactive	45	100	ns			9	24
t69f	XOE# Setup to XDIR# Inactive	10	45	ns			9	24
t69g	XOE# Inactive from SA[16:0] and LA[23:17]		25	ns			10	24
t69h	XDIR# Inactive from IOR#, MEMR# Inactive	15	60	ns			10	24

Table 5. ISA BUS AND X-BUS TIMINGS (Sheet 10 of 10)

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Type	Size	Notes	Fig
DMA Accesses to X-Bus								
	XDIR#							
t70a	XDIR# Active from DACKx#, MDAKx# Active		25	ns			12,14	25
t70b	XDIR# Inactive from DACKx#, MDAKx# Inactive	8	65	ns			12	25
Miscellaneous X-Bus Timings								
	Mouse Timing Support							
t71a	IRQ12/M and IRQ1 Minimum Active Pulse Width (for Mouse Function and Keyboard)	180		ns				26
	Coprocessor Error Support							
t73a	IGNNE# Active from IOW# Active from Port F0H Access		220	ns				26
t73b	IGNNE# Inactive from FERR# Inactive		230	ns				26
	Real Time Clock Timing (RTCALE)							
t75a	RTCALE Pulse Width	200	300	ns				27
t75b	RTCALE Active from IOW# Active - PCI-Initiated Access - ISA-Initiated Access		 85 156	 ns ns				27
	Speaker Timing							
t76a	SPKR Valid Delay from OSC Rising		200	ns				28

NOTES:
1. No-wait-state (ZEROWS#) asserted.
2. This applies to the byte lane that the data has been swapped to.
3. Data is three-stated from the standard memory commands (SMEMR# or SMEMW#), when they are generated.
4. This specification includes both the time the PIIX drives IOCHRDY active and the time it takes the PIIX to float IOCHRDY.
5. This applies to the last cycle of a demand mode DMA transfer.
6. Output from PIIX.
7. 36 ns has been added to the ISA specification to meet ZEROWS# setup requirements.
8. This applies to ISA Master initiated refresh only.
9. PIIX as a master cycles only.
10. ISA master cycles only.
11. This applies to the PIIX cycles that IOCHRDY is not driven low.
12. This applies to all DACK# signals.
13. 56 ns has been added to the ISA specification to meet MEMCS16# setup requirements. ISA devices are not suppose to use the SA address as part of their MEMCS16# decode. However, some devices do use SA as part of MEMCS16# decode.
14. X-Bus read
15. For back-to-back “sub cycles” generated as a result of byte assembly or disassembly, this specification is 34 ns.
16. Type F transfers are selected via the MBDMAX Register

Table 6. PCI Interface Timing

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

Sym	Parameter	Min	Max	Units	Notes	Fig
t77	AD[31:0] Valid Delay	2	11	ns	Min: 0 pF Max: 50 pF	30
t78	AD[31:0] Setup Time	7		ns		31
t79	AD[31:0] Hold Time	0		ns		31
t80	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Valid Delay from PCLKIN Rising	2	11	ns	Min: 0 pF Max: 50 pF	30
t81	C/BEs[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Output Enable Delay from PCLKIN Rising	2		ns		34
t82	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Float Delay from PCLKIN Rising	2	28	ns		32
t83	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Setup Time to PCLKIN Rising	7		ns		31
t84	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, SERR#, IDSEL, DEVSEL# Hold Time from PCLKIN Rising	0		ns		31
t85	PHLD# Valid Delay from PCICLK Rising	2	12	ns	0 pF	30
t86	PHLDA# Setup Time to PCICLK Rising	10		ns		31
t87	PHLDA# Hold Time from PCICLK Rising	0		ns		31
t91	PIRQ[A:D]# Setup Time to PCICLK Rising				1	31
t92	PIRQ[A:D]# Hold Time From PCICLK Rising				1	31
t96	RST# Low Pulse Width	1		ms		33

NOTE:
1. This signal is internally synchronized.

Table 7. PCI Bus IDE Timing

Functional Operating Range (V_{CC} = 5 V ±5%, T_{CASE} = 0° C to +85° C)

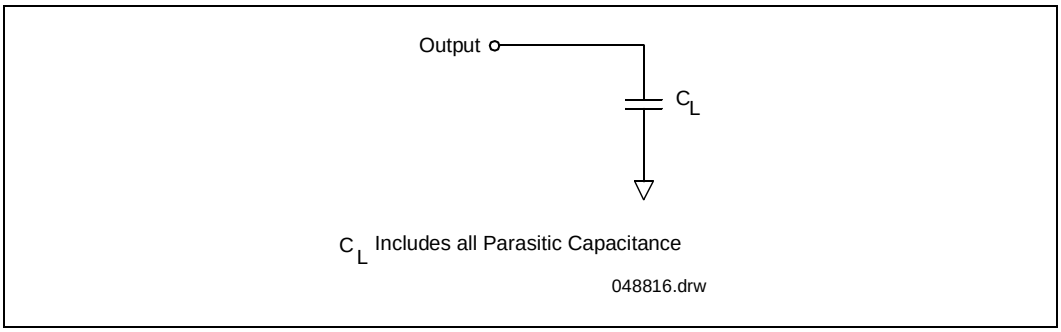
Sym	Parameter	Min	Max	Units	Notes	Fig
t102	DIOW# Active From PCICLK Rising	2	20	ns		35,36
t103	DIOW# Inactive From PCICLK Rising	2	20	ns		35,36
t104	DIOR# Active From PCICLK Rising	2	20	ns		35,36
t105	DIOR# Inactive From PCICLK Rising	2	20	ns		35,36
t106	DA[2:0] Valid Delay From PCICLK Rising	2	30	ns		35
t107	CSxx Active From PCICLK Rising	2	30	ns		35
t108	CSxx Inactive From PCICLK Rising	2	30	ns		35
t109	SOE# Active From PCICLK Rising	2	25	ns		35,36
t110	SOE# Inactive From PCICLK Rising	2	25	ns		
t113	DDAKx# Active From PCICLK Rising	2	20	ns		36
t114	DDAKx# Inactive From PCICLK Rising	2	20	ns		36
t114a	DREQx Setup to PCICLK Rising	7			2	36
t114b	DREQx Hold From PCICLK Rising	7			2	36
t115	DD[15:0] Valid Delay From PCICLK Rising	2	30	PCICLK		35,36
t115a	DD[15:0] Setup to PCICLK Rising	10				35,36
t115b	DD[15:0] Hold From PCICLK Rising	8				35,36
t116	IORDY Setup to PCICLK Rising	7		ns	2	35
t117	IORDY Hold From PCICLK Rising	7		ns	2	35
t118	IORDY Sample Point From DIOx# Assertion			ns	1	35
t119	DIOx# Active Pulse Width	ISP Setting		PCICLK	3	35,36
t120	DIOx# Inactive Pulse Width	RTC Setting		PCICLK	4	

NOTES:
1. This parameter is programmable in the IDE Timing Register.
2. DREQx, IORDY are internally synchronized. This timing is to guarantee recognition on the next clock.
3. ISP represents the setting of the IORDY Sample Point field in the IDE Timing Register (2 to 5 PCICLKs).
4. RTC represents the setting of the Recovery Time field in the IDE Timing Register (1 to 4 PCICLKs).

Table 8. AC Test Loads

Capacitive Load	Signals
120pf	REFRESH#, TC, SD[15:0], SA[7:0], SBHE#, LA[23:17], I0CS16#, MEMCS16#, MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW#, AEN, BALE, IOCHRDY, ZEROWS#, RSTDRV, SYSCLK, DD[15:0]
50pf	DACK#[7:5,3:0], SPKR, INTR, NMI, BIOSCS#, KBCCS#, RTCCS#, RTCALE, XDIR#, XOE#, IGNNE#, SOE#, SDIR#, MDAKx#, DIOR#, DIOW#, DDAK[1:0]#

Figure 1. Test Load



1.5 Clock, Reset, ISA Bus, X-Bus, and Host Timing Diagrams

Figure 2. Clock Timing

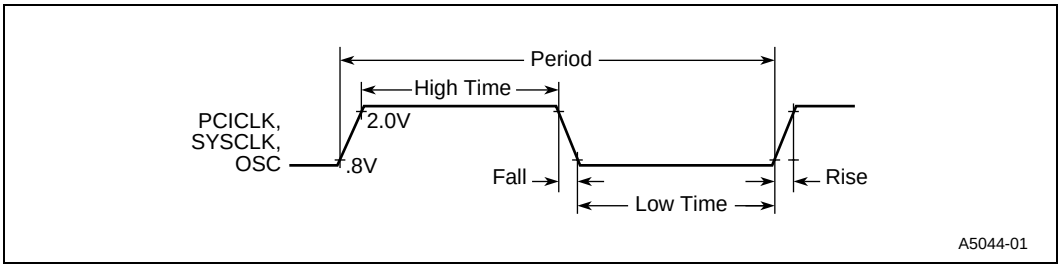


Figure 3. Reset Inactive After PWROK

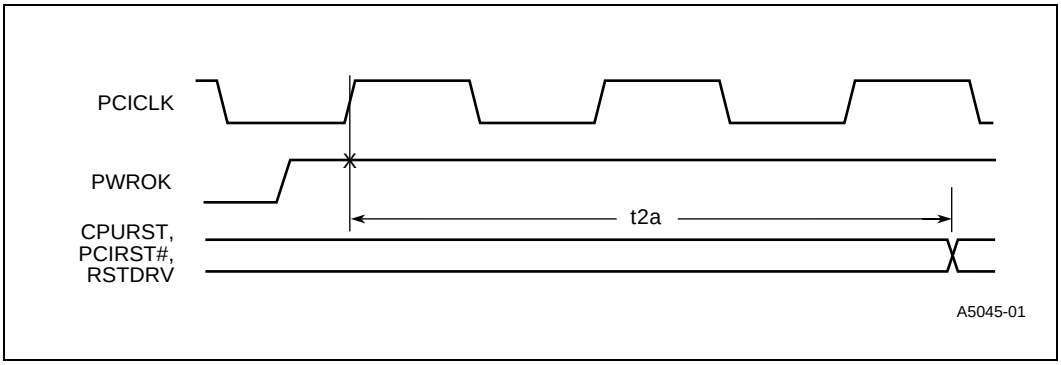


Figure 4. Reset Active Pulse Width

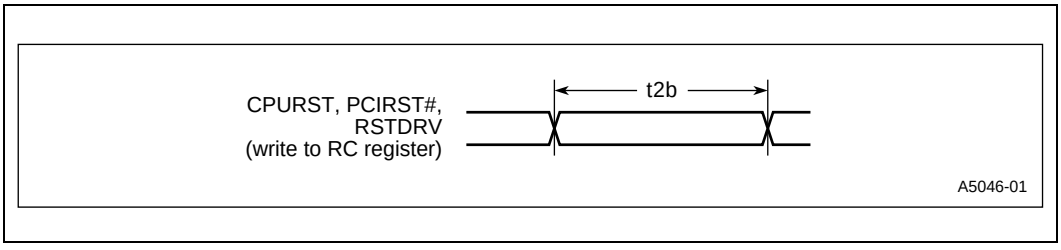


Figure 5. SMI#, EXTSMI#, and STPCLK# Timing

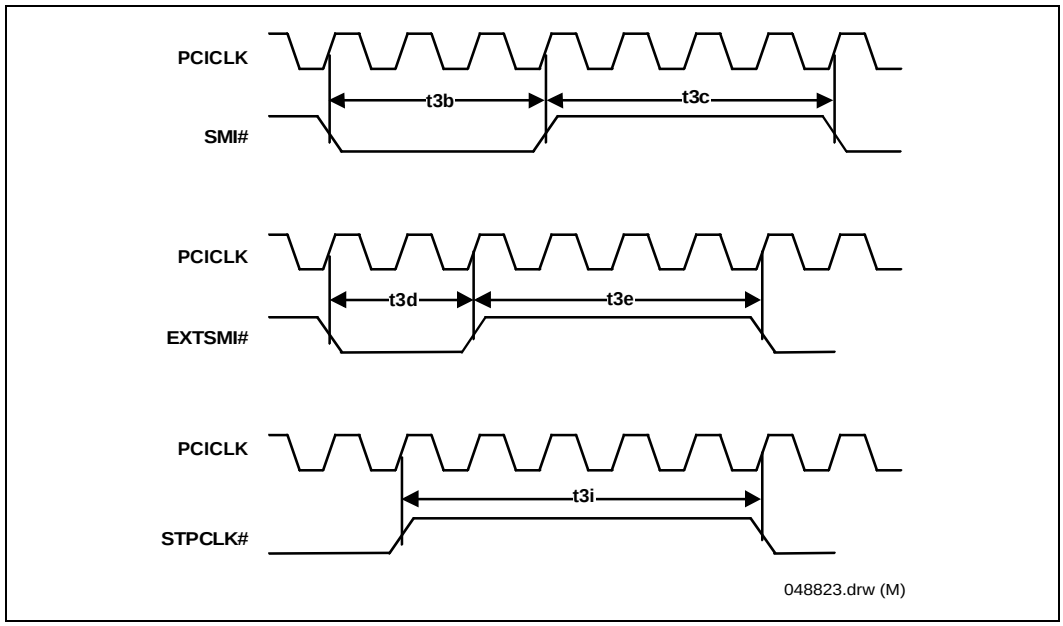


Figure 6. Input to PCICLK Setup/Hold Times

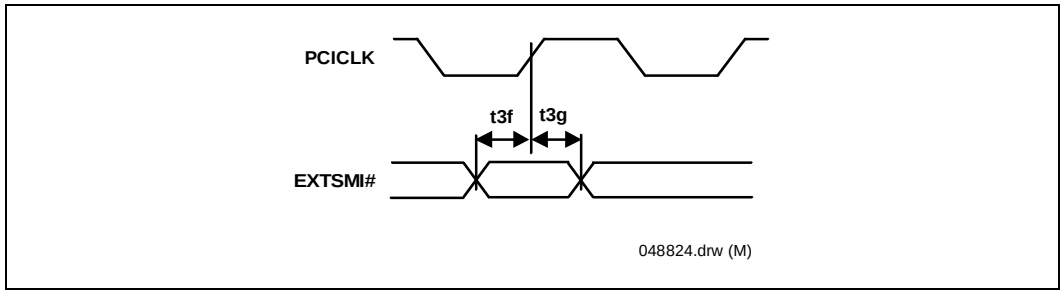


Figure 7. HCLKIN to Output Valid Delay

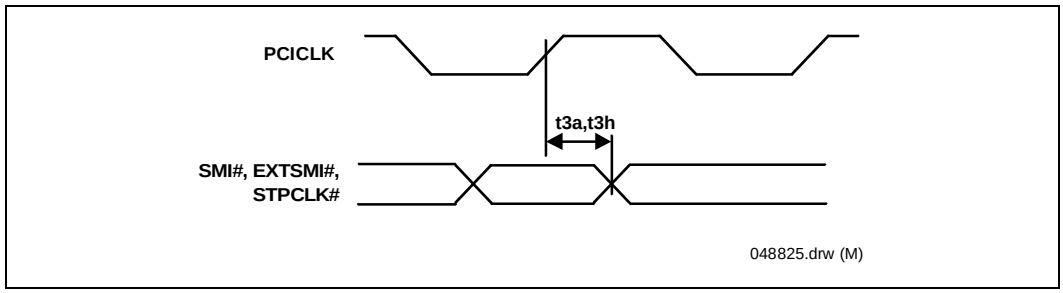


Figure 8. 8-Bit ISA Memory Slave Timing (PIIX as Master)

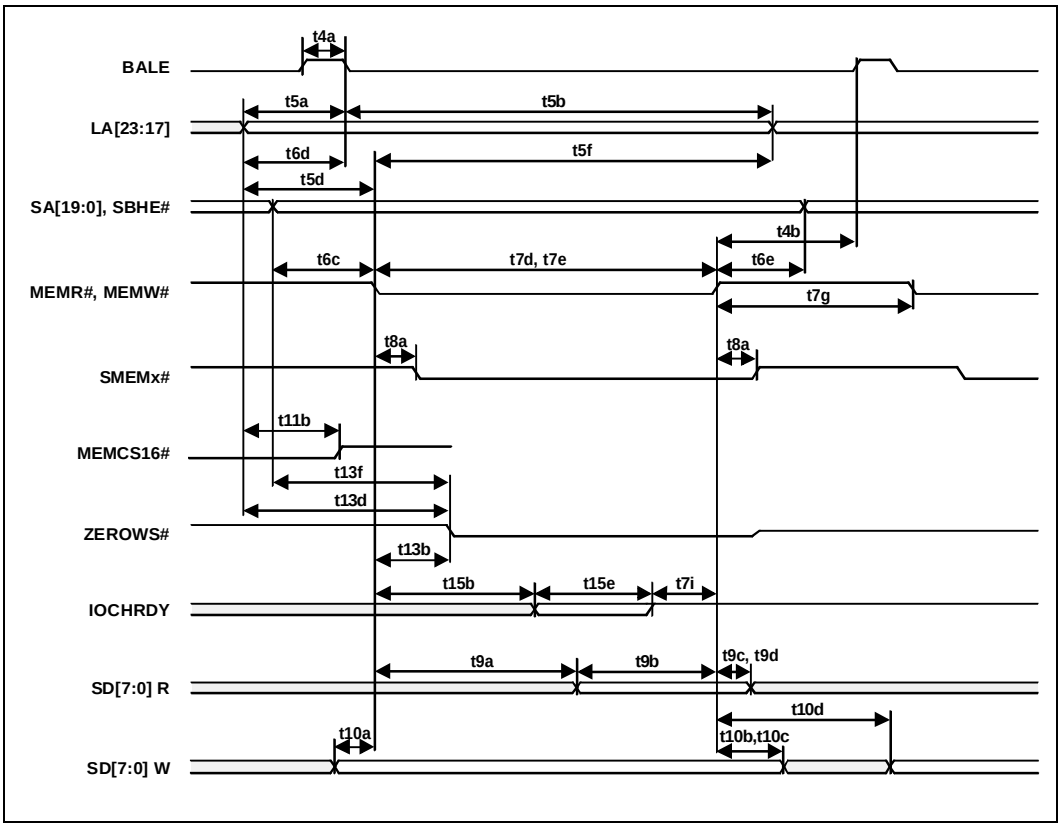


Figure 9. 16-Bit ISA Memory Slave Timing (PIIX as Master)

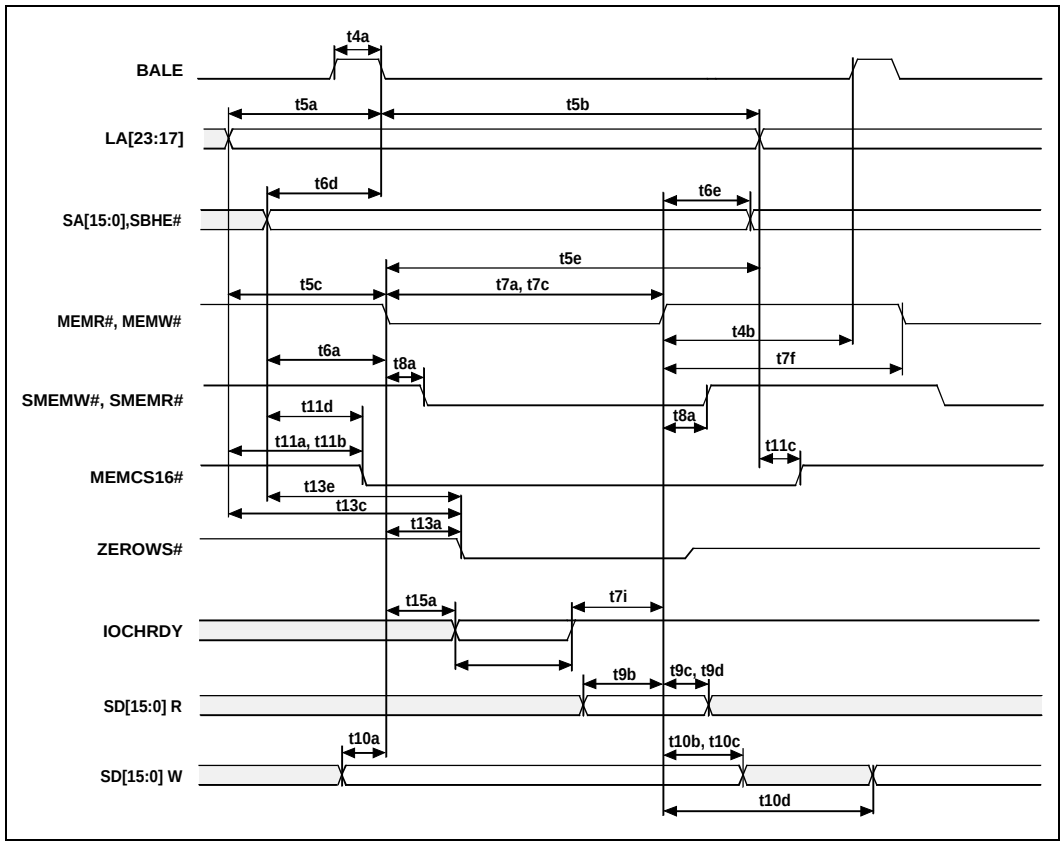


Figure 10. 8-Bit ISA I/O Slave Timing (PIIX as Master)

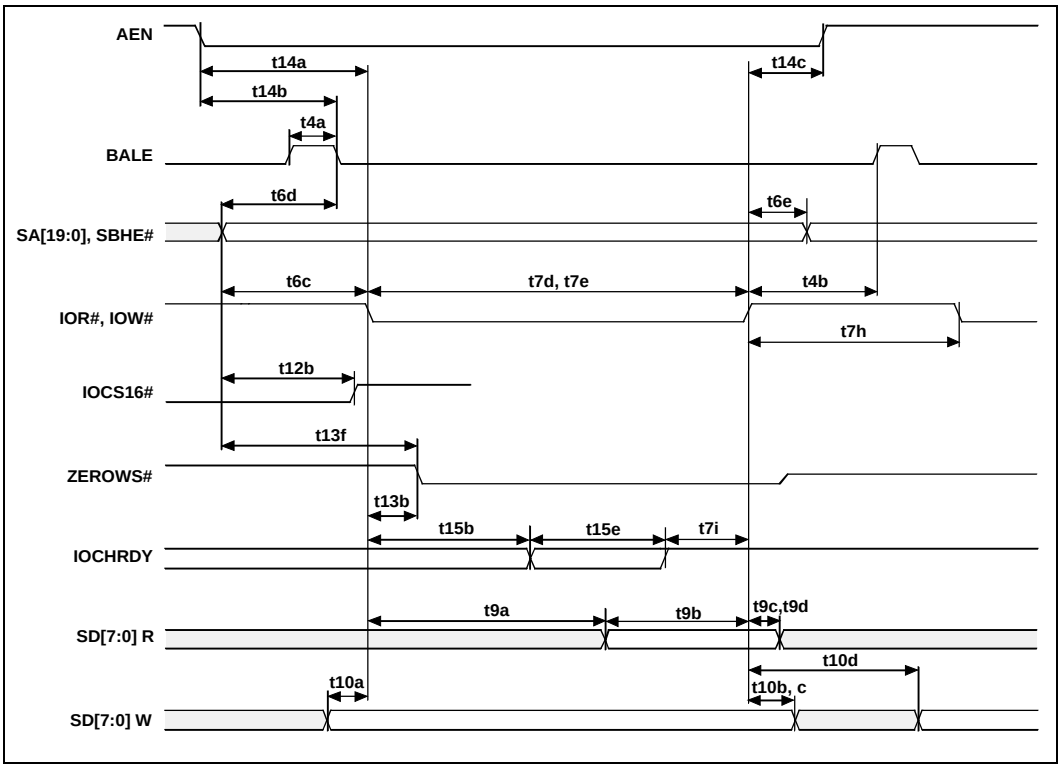


Figure 11. 16-Bit I/O Slave Timing (PIIX as Master)

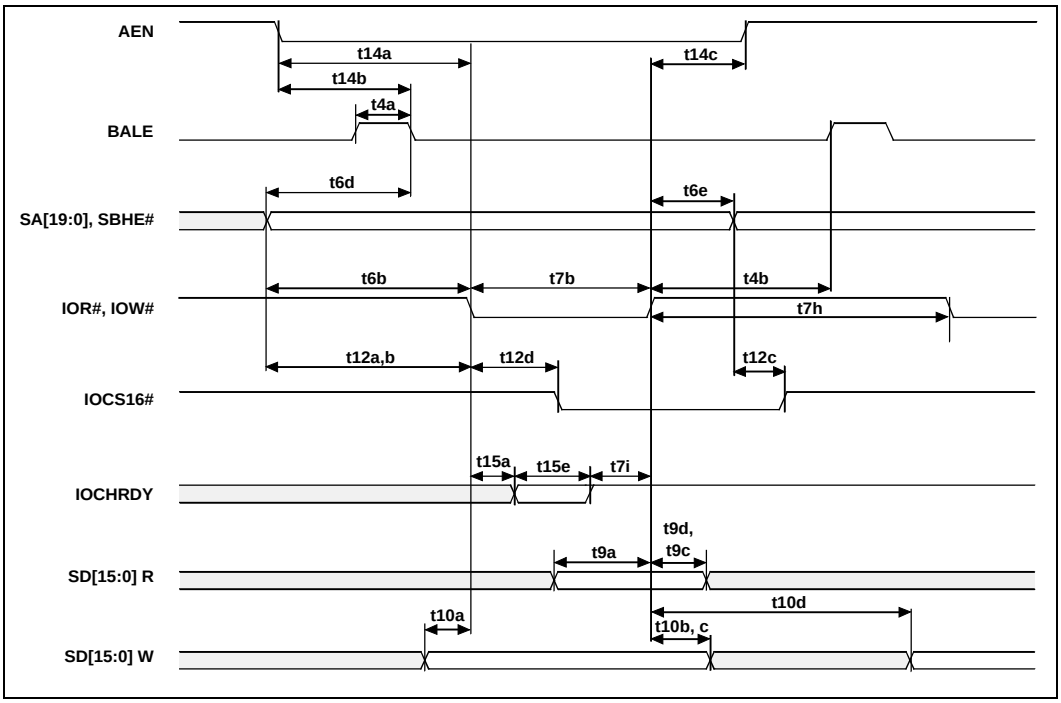


Figure 12. ISA Master Accessing PCI Memory Timing

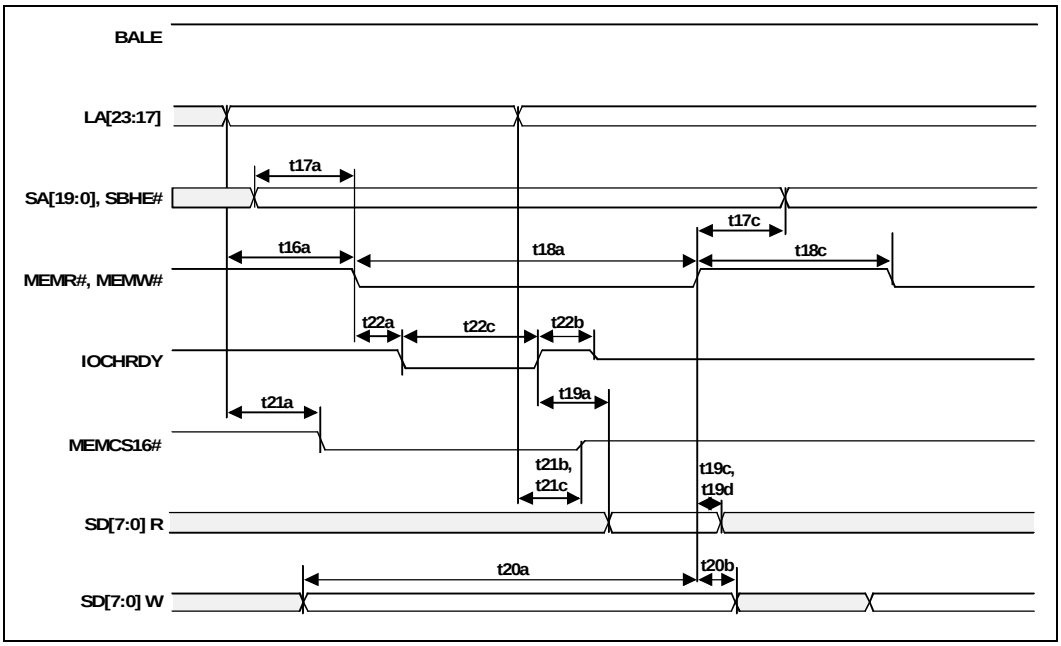


Figure 13. ISA Master Accessing PIIX Register Timing

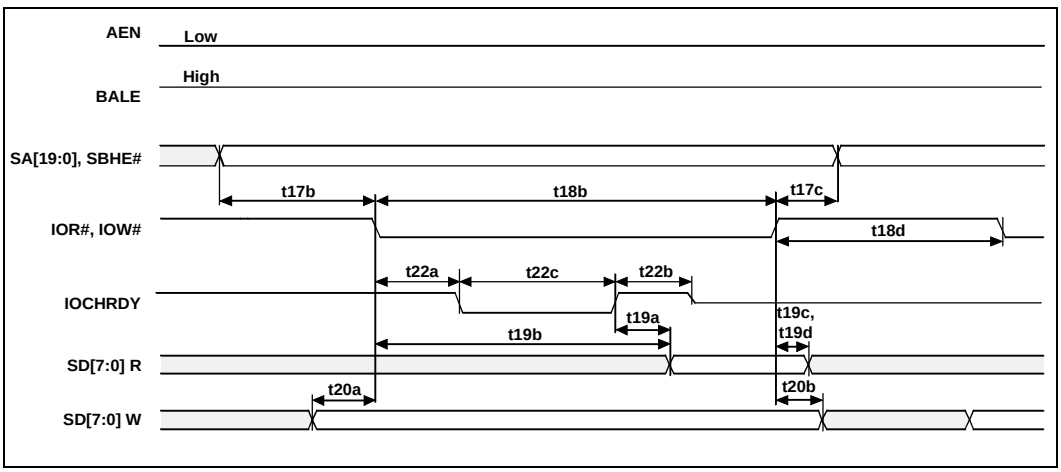


Figure 14. NMI Timing

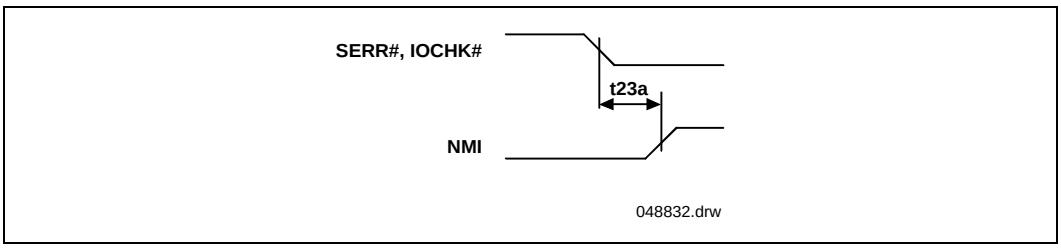


Figure 15. Interrupt Timing

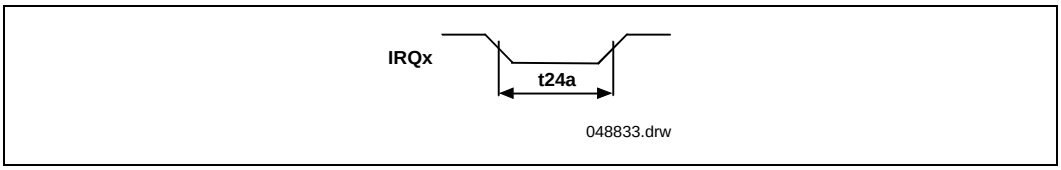


Figure 16. ISA Master Miscellaneous Timing

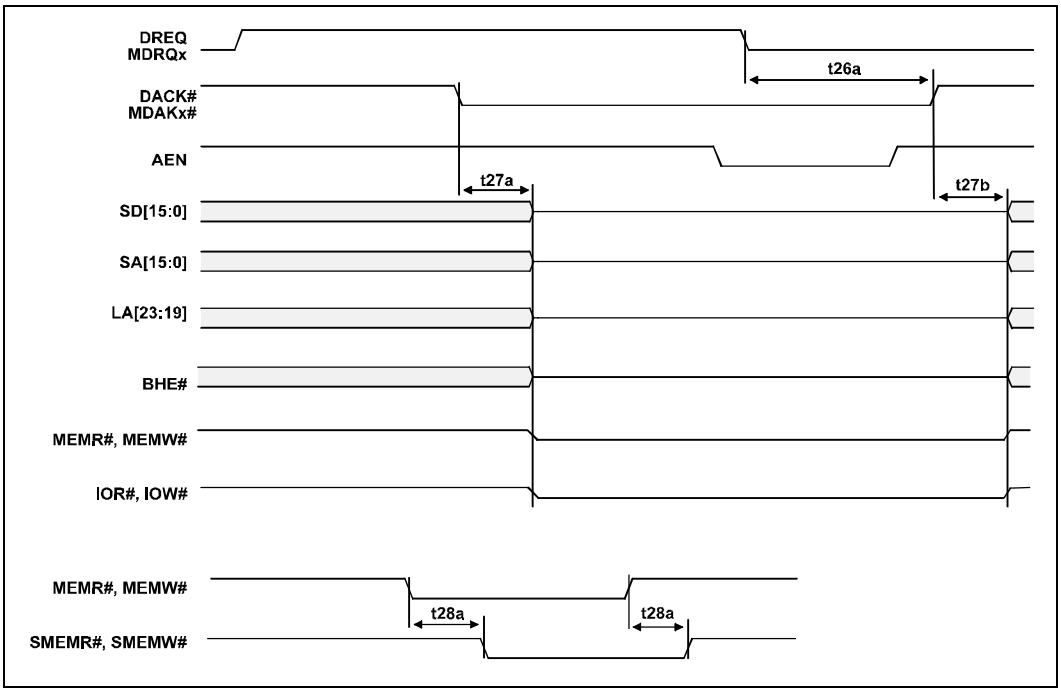


Figure 17. ISA Master Data Swap Timing

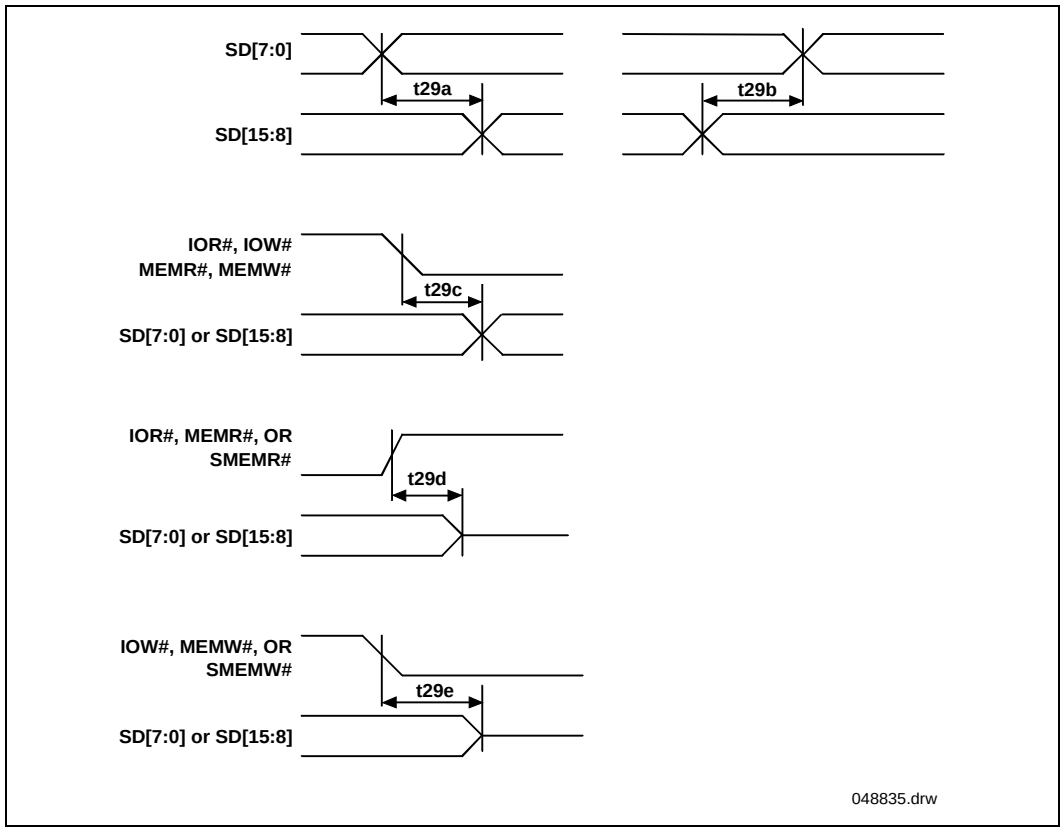


Figure 18. DMA Compatible Timing (Memory Read)

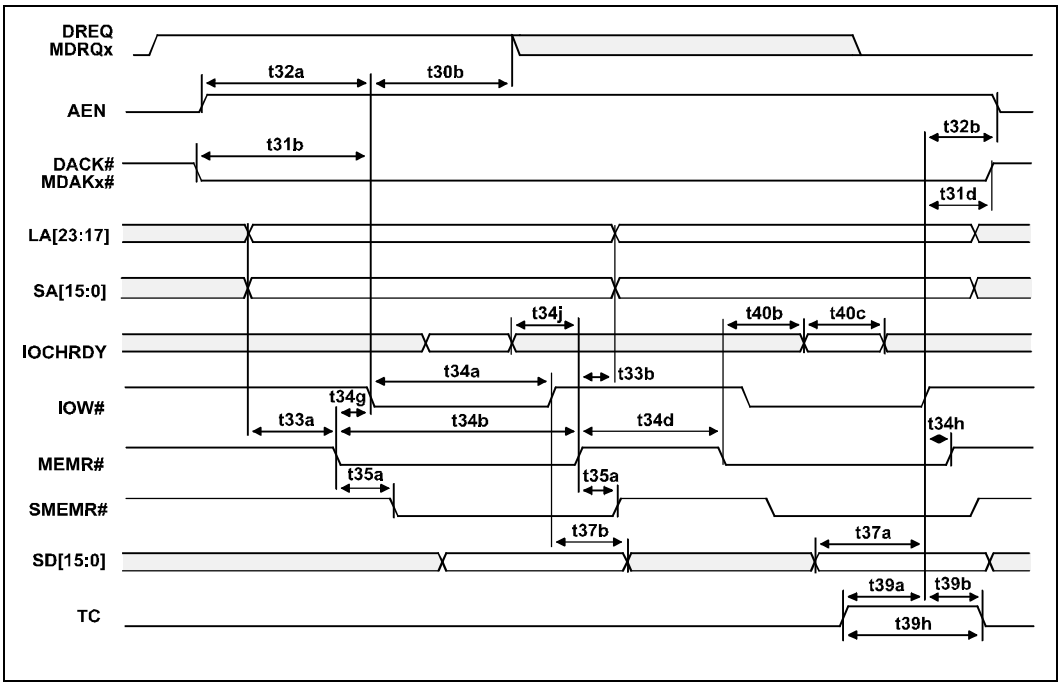


Figure 19. DMA Compatible Timing (Memory Write)

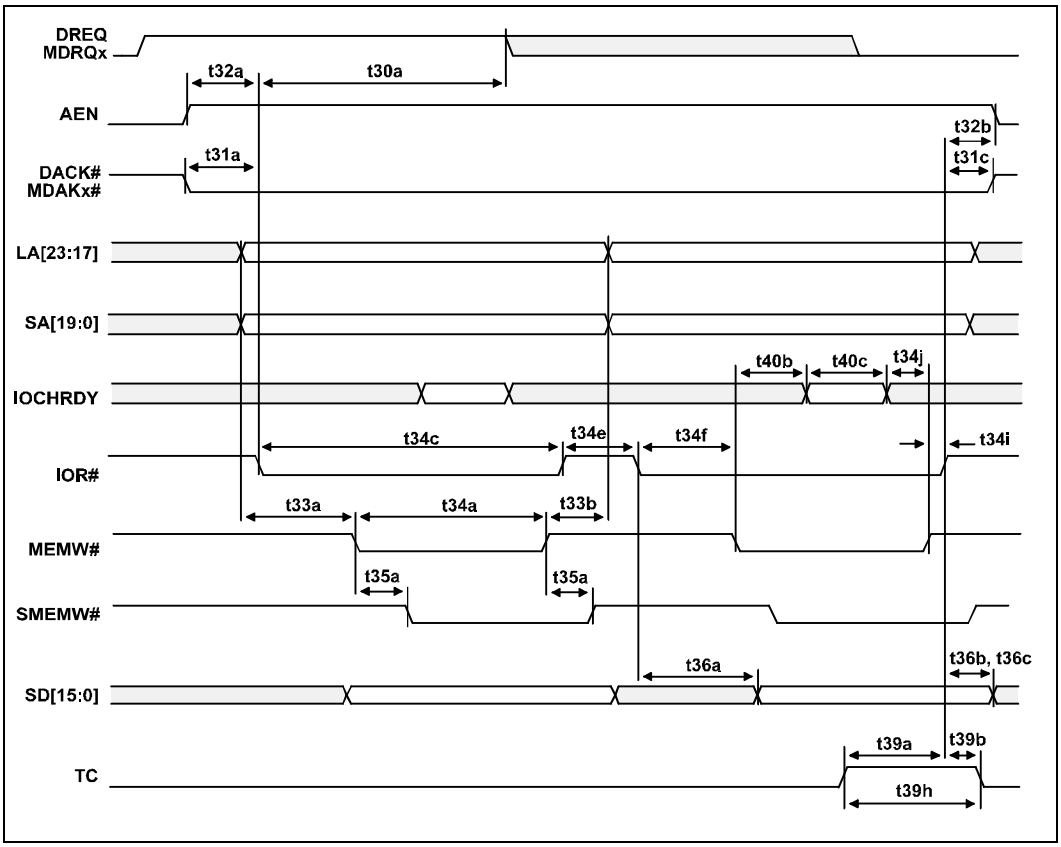


Figure 20. DMA Compatible Timing (Data Swap)

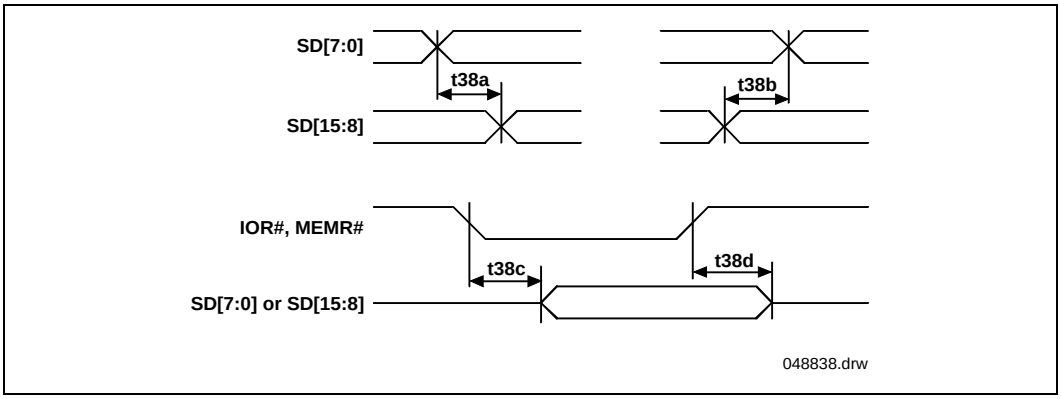


Figure 21. DMA Type F Timing

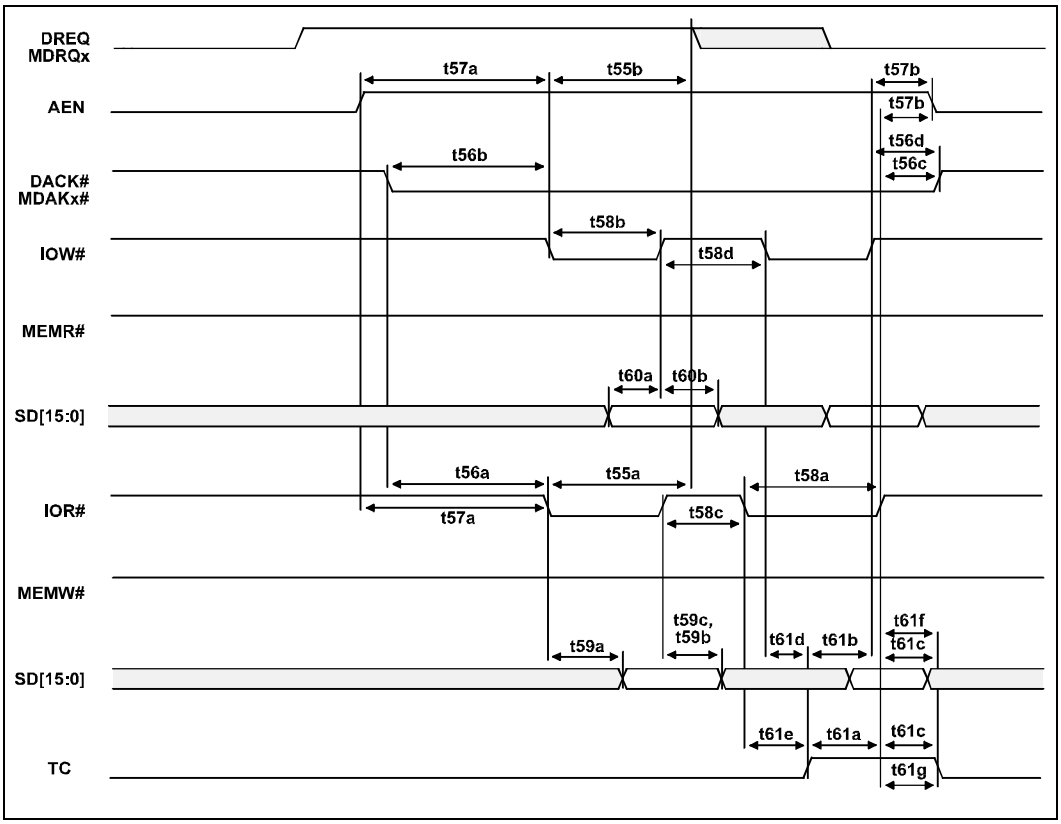


Figure 22. PIIX-Initiated Refresh Timing

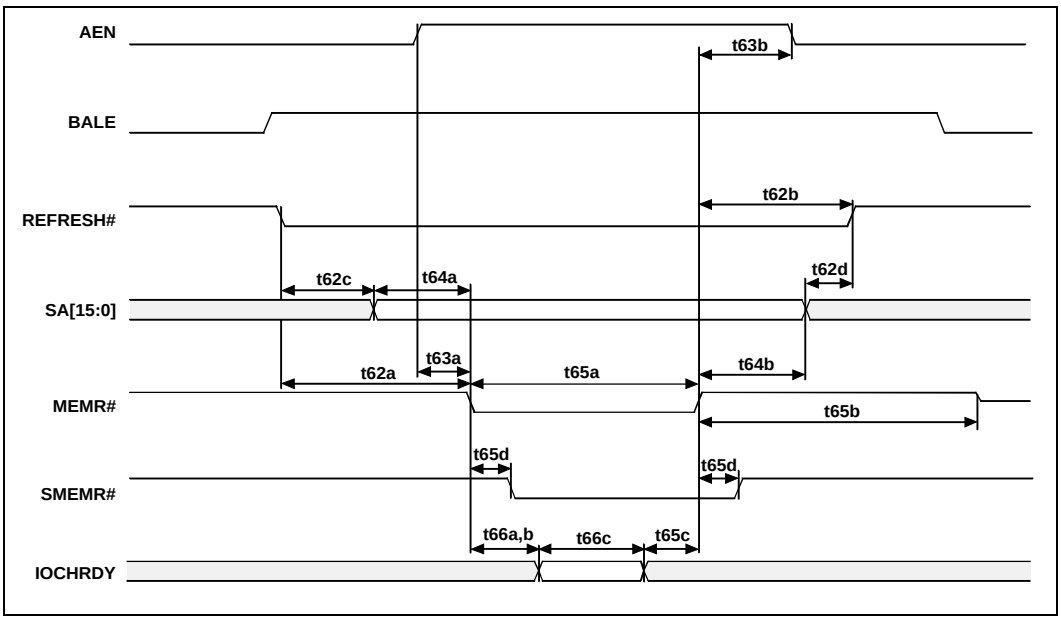


Figure 23. ISA Master-Initiated Refresh Timing

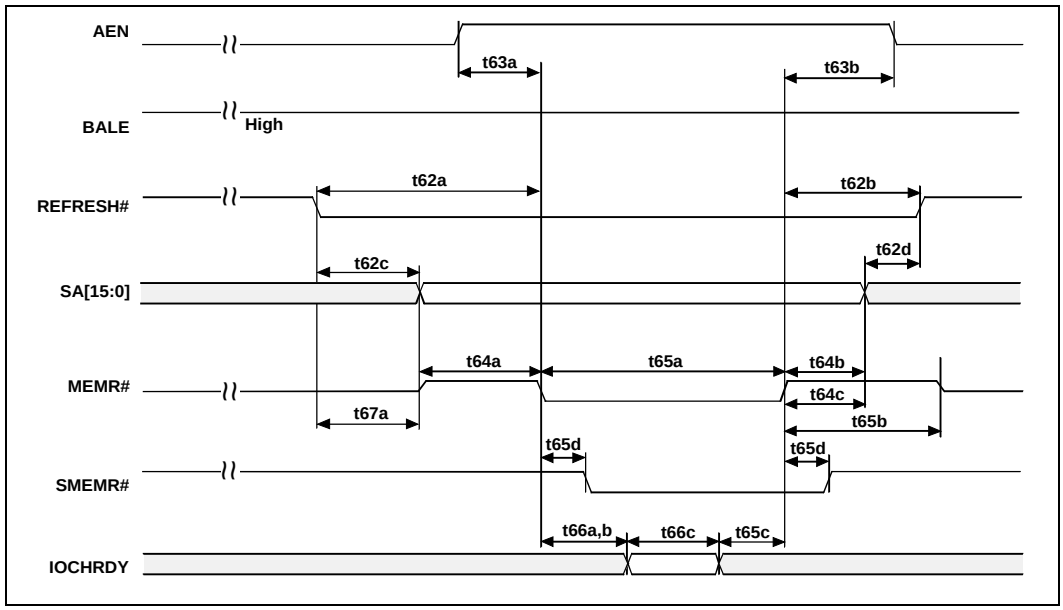


Figure 24. PIIX and ISA Master Access to X-Bus Timing

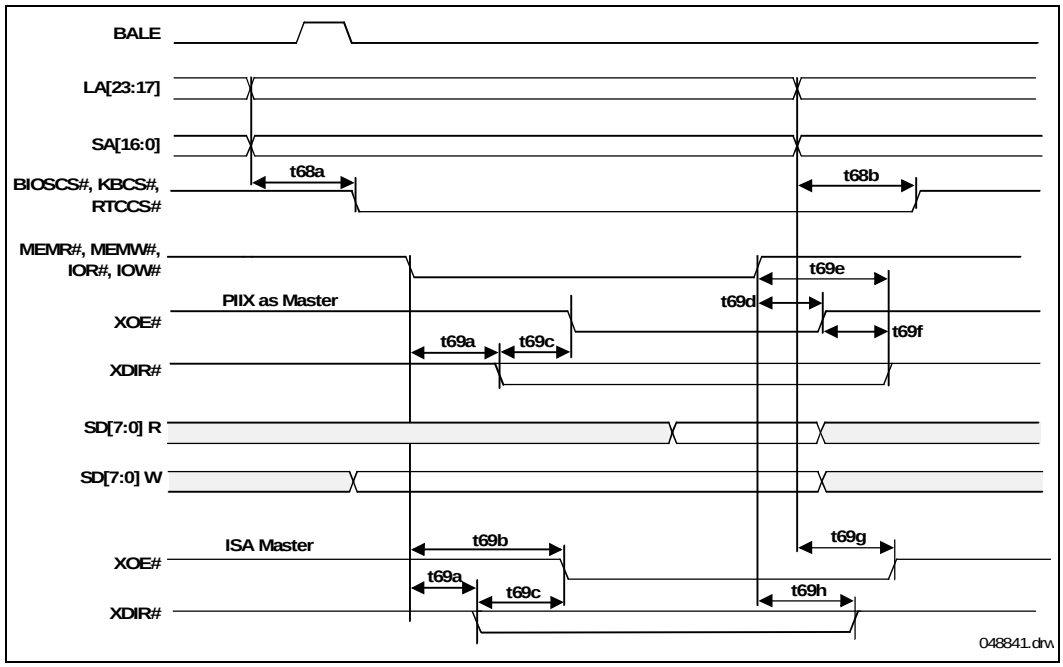


Figure 25. DMA Access to X-Bus Timing

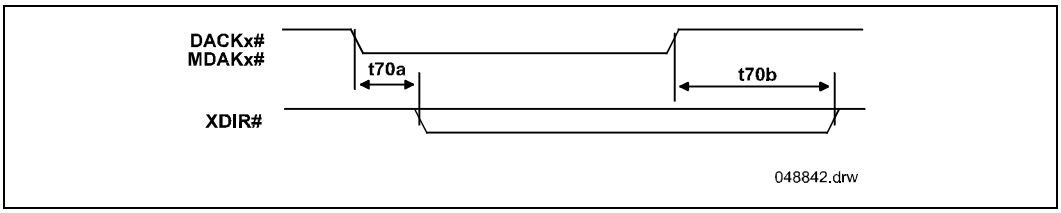


Figure 26. Coprocessor Error and Mouse Support Timing

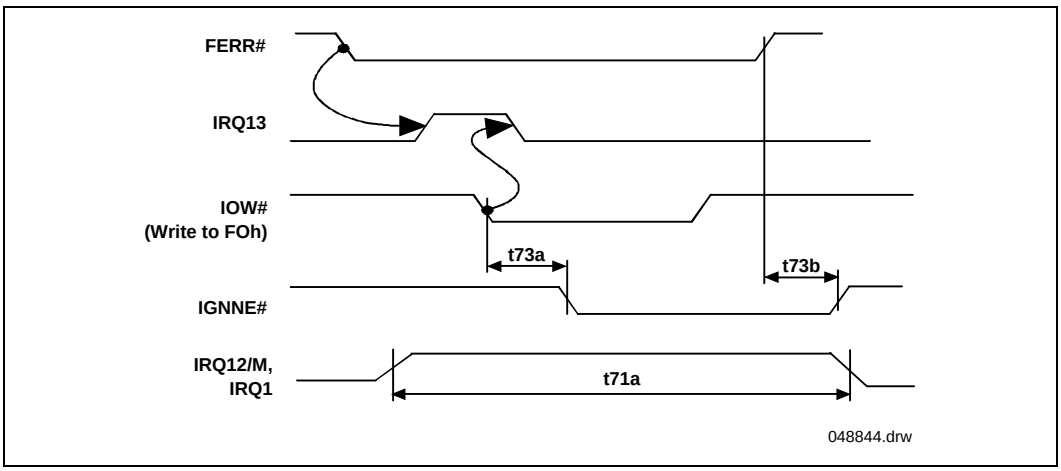


Figure 27. Real Time Clock Timing (RTCALE Generation)

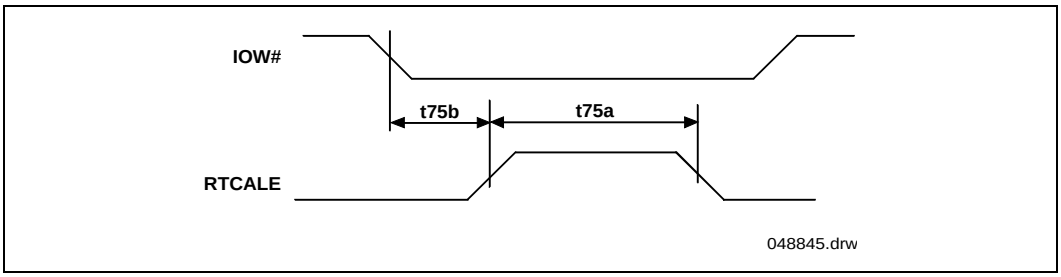
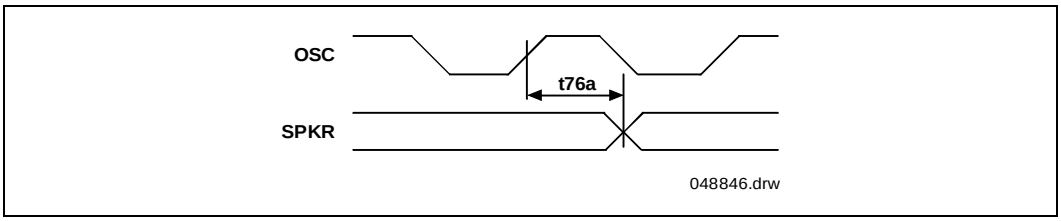


Figure 28. Speaker Timing



1.6 PCI Timing Diagrams

Figure 29. Propagation Delay

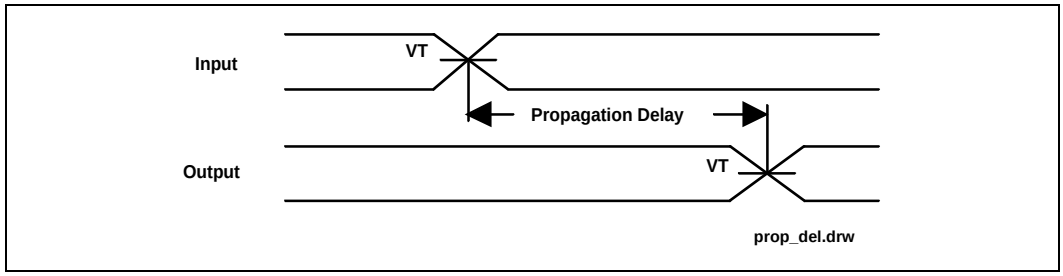


Figure 30. Valid Delay From Rising Clock Edge

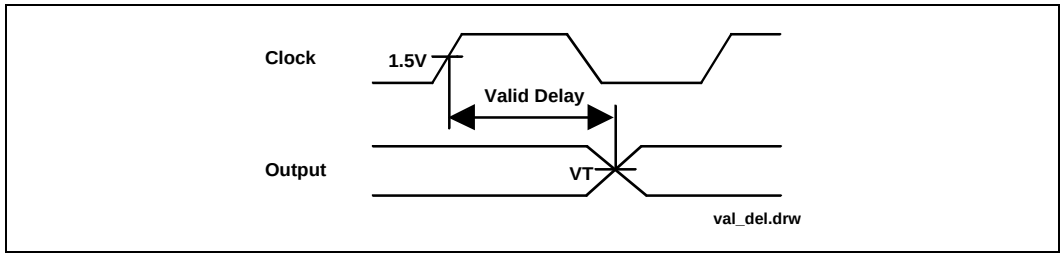


Figure 31. Setup and Hold Times

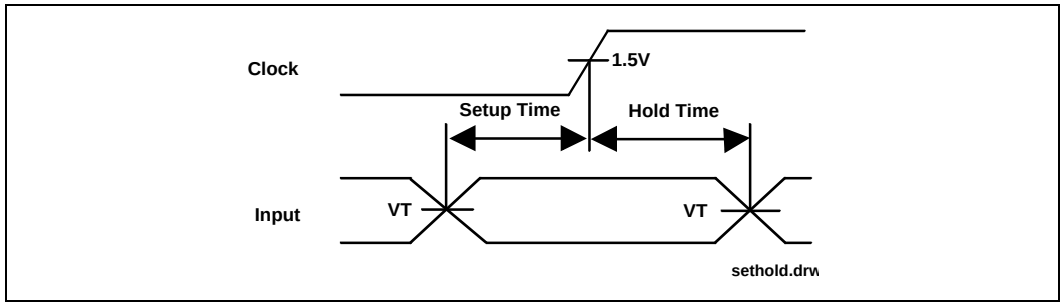


Figure 32. Float Delay

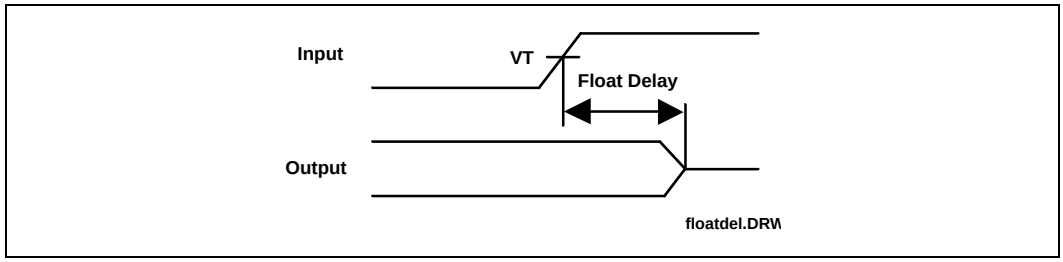


Figure 33. Pulse Width

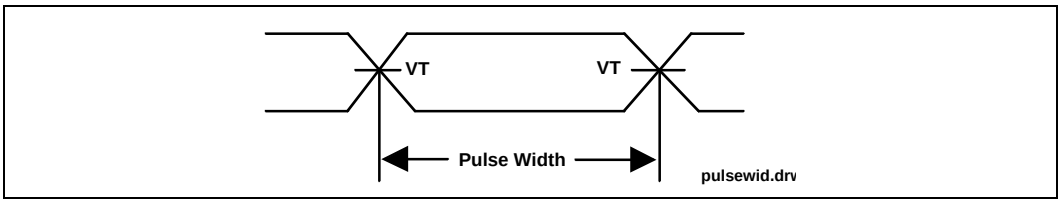
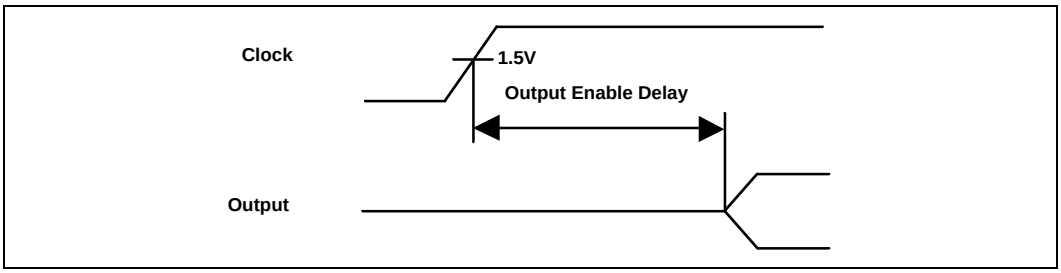


Figure 34. Output Enable Delay



1.7 IDE Timing Diagrams

Figure 35. IDE PIO Mode

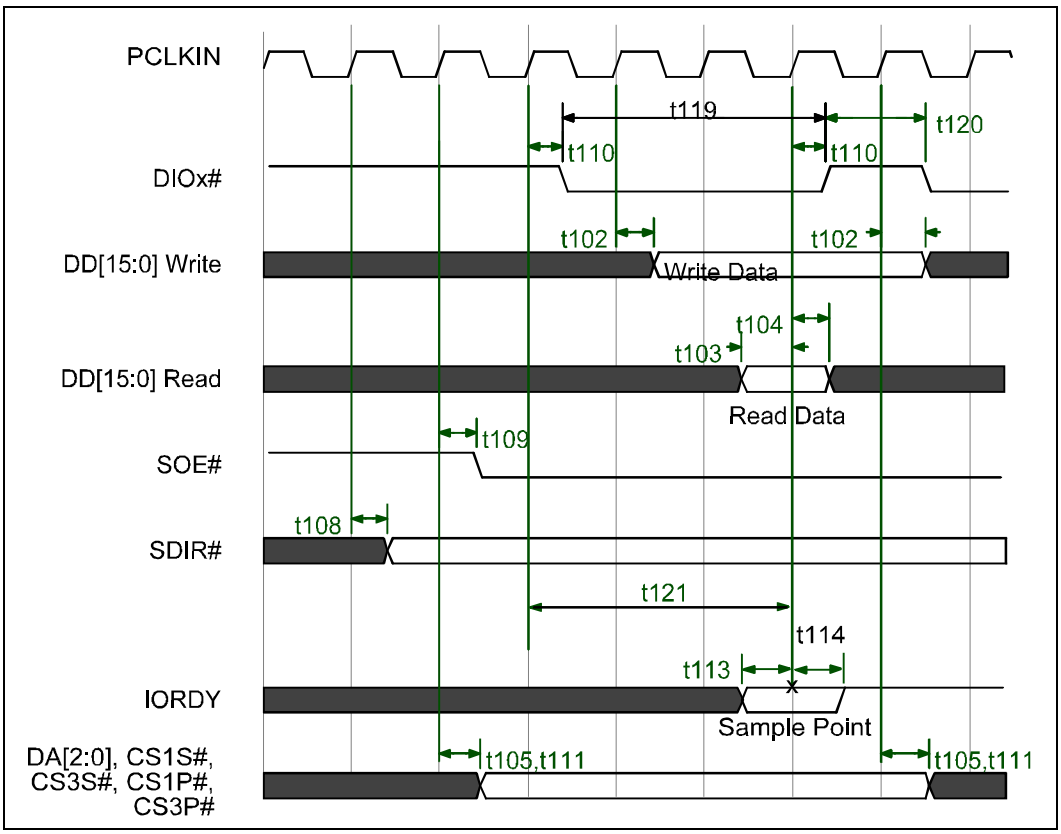
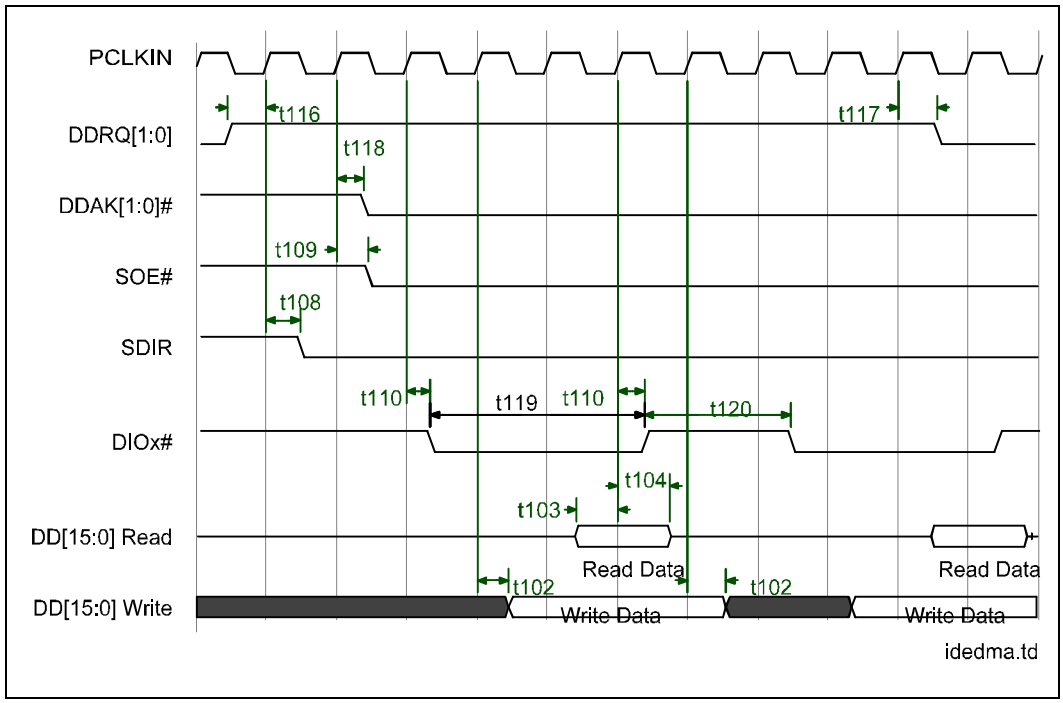


Figure 36. IDE Multiword DMA Mode

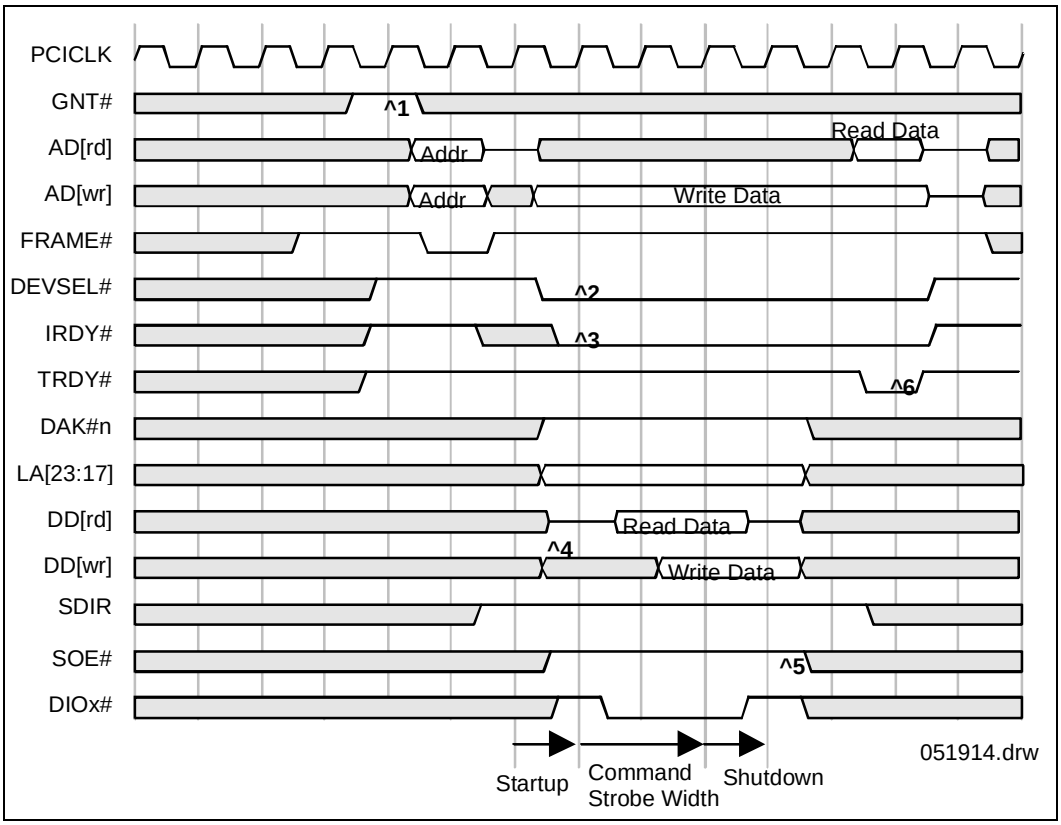


2.0 Timing Relationship Diagrams

2.1 PCI to IDE AT Compatible Transaction Timing

This diagram illustrates the generic case of a PCI master reading from or writing to and IDE I/O port. Note that the latency to start up (setup of the address and chip selects with respect to the command strobe) and shut down (hold time of the address and chip selects with respect to the command strobe) the IDE cycle are shown as one clock. In reality, different values are used for different types of transactions. The command strobe assertion width is shown as two PCI clocks. This is the minimum value for the fast timing modes. The 8- and 16-bit compatible timing modes are slower. The values for the start-up, shutdown, and command strobe width are given in the Table 9.

Figure 37. PCI Master Access to IDE Device



NOTES:
1. The PHLDA# signal will always be negated at least one clock prior to FRAME# assertion.
2. DEVSEL# is asserted by the PIIX in medium time.
3. The IRDY# signal must be sampled asserted for writes by this point in order not to delay the assertion of the DIOW# signal.
4. The DD[15:0] signals are three-stated on this clock in the case of reads from the IDE ports. Therefore, the earliest that the DIOR# signal (which enables data to be driven onto the DD[15:0] lines by the IDE slave device) can be driven is the following clock. (Therefore, the start-up latency is at least one clock)
5. The SOE# signal is reasserted when no more IDE transactions are pending.
6. TRDY# is asserted here with respect to the negation edge of the DIOR# and DIOW# signals.

Table 9. Command Strobe Width For IDE Transaction Type

IDE transaction type	Start-up Latency	Shutdown Latency	ISP	RCT
Non data port (8-bit) ¾ 25 MHz	4	1	9	17
Data port (16-bit)¾ 25 MHz	3	1	5	11
Non data port (8-bit)¾ 30/33 MHz	4	1	11	22
Data port (16-bit) ¾ 30/33 MHz	3	1	6	14
Enhanced timing data port (MAX)	2	1	5	4
Enhanced timing data port (MIN)	2	1	2	1

NOTE: Start-up and Shutdown latency will be incurred for all IDE PIO transactions, except enhanced timing data port transactions. Further, the IDE chip selects are negated for at least two clocks after the Shutdown latency of the last transaction and before the Start-up latency of the next.