1.0 Electrical Specifications: 80L960JA/JF Processor

Note: This section contains preliminary information on new products in production. The specifications are subject to change without notice.

1.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 1. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Case Temperature Under Bias	–65°C to +110°C
Supply Voltage wrt. V_{SS}	–0.5 V to + 4.6 V
Voltage on Other Pins wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

1.2 Operating Conditions

Warning: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 2. 80L960JA/JF Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage 80L960JA/JF-25 80L960JA/JF-16	 3.0 3.0	 3.6 3.6	V	
f_{CLKIN}	Input Clock Frequency 80L960JA/JF-25 80L960JA/JF-16	 8 8	 25 16.67	MHz	
T_C	Operating Case Temperature A80L960JA/JF-25 (132 PGA) A80L960JA/JF-16 (132 PGA) NG80L960JA/JF-25 (132 PQFP) NG80L960JA/JF-16 (132 PQFP)	 0 0 0 0	 100 100 100 100	°C	

1.3 Connection Recommendations

For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960Jx processor power and ground pins. On the circuit board, every V_{CC} pin should connect to a power plane and every V_{SS} pin should connect to a ground plane. Place liberal decoupling capacitance near the processor, since the processor can cause transient power surges.

Pay special attention to the Test Reset (TRST#) pin. It is essential that the JTAG Boundary Scan Test Access Port (TAP) controller initializes to a known state whether it will be used or not. If the JTAG Boundary Scan function will be used, connect a pulldown resistor between the TRST# pin and V_{SS}. If the JTAG Boundary Scan function will not be used (even for board-level testing), connect the TRST# pin to V_{SS}. Also, do not connect the TDI, TDO, and TCK pins if the TAP Controller will not be used.

Pins identified as NC must not be connected in the system.

1.4 DC Specifications

Table 3. 80L960JA/JF DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage			0.4 0.2		I_{OL} = 3 mA I_{OL} = 100 µA
V_{OH}	Output High Voltage	2.4 V_{CC} - 0.2		V	V	I_{OH} = -3 mA I_{OH} = -100 µA
V_{OLP}	Output Ground Bounce		< 0.8		V	(1,2)
C_{IN}	Input Capacitance PGA PQFP			 12 10	pF	$f_{CLKIN} = f_{MIN}$ (2)
C_{OUT}	I/O or Output Capacitance PGA PQFP			 12 10	pF	$f_{CLKIN} = f_{MIN}$ (2)
C_{CLK}	CLKIN Capacitance PGA PQFP			 12 10	pF	$f_{CLKIN} = f_{MIN}$ (2)

NOTES:
1. Typical is measured with V_{CC} = 3.3V and temperature = 25 °C.
2. Not tested.

Table 4. 80L960JA/JF I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
I_{LI1}	Input Leakage Current for each pin except TCK, TDI, TRST# and TMS		± 1	µA	$0 \le V_{IN} \le V_{CC}$
I_{LI2}	Input Leakage Current for TCK, TDI, TRST# and TMS	-140	-250	µA	V_{IN} = 0.45V (1)
I_{LO}	Output Leakage Current		± 1	µA	$0.4 \le V_{OUT} \le V_{CC}$
I_{CC} Active (Power Supply)	80960JA/JF-25 80960JA/JF-16		284 184	mA	(1,2) (2,3)
I_{CC} Active (Thermal)	80960JA/JF-25 80960JA/JF-16	225 165		mA	(2,4) (2,4)
I_{CC} Test Reset mode	80960JA/JF-25 80960JA/JF-16		200 150	mA	(5) (5)
I_{CC} Test Halt mode	80960JA/JF-25 80960JA/JF-16		26 16	mA	(5) (5)
I_{CC} Test ONCE mode			10	mA	(5)

1. These pins have internal pullup devices. Typical leakage current is not tested.
2. Measured with device operating and outputs loaded to the test condition in Figure 1 “AC Test Load”.
3. I_{CC} Active (Power Supply) value is provided for selecting your system’s power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.6V. This parameter is characterized but not tested.
4. I_{CC} Active (Thermal) value is provided for your system’s thermal management. Typical I_{CC} is measured with V_{CC} = 3.3V and temperature = 25° C. This parameter is characterized but not tested.
5. I_{CC} Test (Power modes) refers to the I_{CC} values that are tested when the 80960JA/JF is in Reset mode, Halt mode or ONCE mode with V_{CC} = 3.6V.

1.5 AC Specifications

The 80960Jx AC timings are based upon device characterization.

Table 5. 80L960JA/JF AC Characteristics (25 MHz) (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK TIMINGS					
T_F	CLKIN Frequency	8	25	MHz	
T_C	CLKIN Period	40	125	ns	
T_{CS}	CLKIN Period Stability		± 250	ps	(1,2)
T_{CH}	CLKIN High Time	12		ns	Measured at 1.5 V (1)
T_{CL}	CLKIN Low Time	12		ns	Measured at 1.5 V (1)
T_{CR}	CLKIN Rise Time		4	ns	0.8 V to 2.0 V (1)
T_{CF}	CLKIN Fall Time		4	ns	2.0 V to 0.8 V (1)
SYNCHRONOUS OUTPUT TIMINGS					
T_{OV1}	Output Valid Delay, Except ALE/ ALE# Inactive and DT/R#	4.0	18	ns	(3)
T_{OV2}	Output Valid Delay, DT/R#	0.5 T_C + 4.0	0.5 T_C +18	ns	
T_{OF}	Output Float Delay	4.0	16	ns	(4)
SYNCHRONOUS INPUT TIMINGS					
T_{IS1}	Input Setup to CLKIN — AD[31:0], NMI#, XINT[7:0]#	9		ns	(5)
T_{IH1}	Input Hold from CLKIN — AD[31:0], NMI#, XINT[7:0]#	1		ns	(5)
T_{IS2}	Input Setup to CLKIN — RDYRCV# and HOLD	10		ns	(6)
T_{IH2}	Input Hold from CLKIN — RDYRCV# and HOLD	1		ns	(6)
T_{IS3}	Input Setup to CLKIN — RESET#	8		ns	(7)
T_{IH3}	Input Hold from CLKIN — RESET#	1		ns	(7)
T_{IS4}	Input Setup to RESET# — ONCE#, STEST#	8		ns	(8)
T_{IH4}	Input Hold from RESET# — ONCE#, STEST#	1		ns	(8)

NOTE: Refer to Table 6 for note definitions for this table.

Table 5. 80L960JA/JF AC Characteristics (25 MHz) (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
RELATIVE OUTPUT TIMINGS					
T_{LXL}	ALE/ALE# Width	$0.5T_C$ - 7.5		ns	(9)
T_{LXA}	Address Hold from ALE/ALE# Inactive	$0.5T_C$ - 7.5		ns	Equal Loading (9)
T_{DXD}	DT/R# Valid to DEN# Active	$0.5T_C$ - 7.5		ns	Equal Loading (9)
BOUNDARY SCAN TEST SIGNAL TIMINGS					
T_{BSF}	TCK Frequency		0.5 T_F	MHz	
T_{BSCH}	TCK High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	4		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	6		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	(1, 10)
T_{BSOF1}	TDO Float Delay	3	36	ns	(1, 10)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	35	ns	(1, 10)
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	36	ns	(1, 10)
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	4		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	6		ns	

NOTE: Refer to Table 6 for note definitions for this table.

Table 6. Note Definitions for Table 5 “80L960JA/JF AC Characteristics (25 MHz)”

1. Not tested.
2. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal clock, the jitter frequency spectrum should not have any power peaking between 500 KHz and 1/3 of the CLKIN frequency.
3. Inactive ALE/ALE# refers to the falling edge of ALE and the rising edge of ALE#. For inactive ALE/ALE# timings, refer to Relative Output Timings in Table 5.
4. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested, but is designed to be no longer than the valid delay.
5. AD[31:0] are synchronous inputs. Setup and hold times must be met for proper processor operation. NMI# and XINT[7:0]# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, NMI# and XINT[7:0]# must be asserted for a minimum of two CLKIN periods to guarantee recognition.
6. RDYRCV# and HOLD are synchronous inputs. Setup and hold times must be met for proper processor operation.
7. RESET# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
8. ONCE# and STEST must be stable at the rising edge of RESET# for proper operation.
9. Guaranteed by design. May not be 100% tested.
10. Relative to falling edge of TCK.

Table 7. 80L960JA/JF AC Characteristics (16 MHz) (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK TIMINGS					
T_F	CLKIN Frequency	8	16.67	MHz	
T_C	CLKIN Period	60	125	ns	
T_{CS}	CLKIN Period Stability		± 250	ps	(1,2)
T_{CH}	CLKIN High Time	18		ns	Measured at 1.5 V (1)
T_{CL}	CLKIN Low Time	18		ns	Measured at 1.5 V (1)
T_{CR}	CLKIN Rise Time		6	ns	0.8 V to 2.0 V (1)
T_{CF}	CLKIN Fall Time		6	ns	2.0 V to 0.8 V (1)
SYNCHRONOUS OUTPUT TIMINGS					
T_{OV1}	Output Valid Delay, Except ALE/ALE# Inactive and DT/R#	4.0	21	ns	(3)
T_{OV2}	Output Valid Delay, DT/R#	0.5 T_C + 4.0	0.5 T_C +21	ns	
T_{OF}	Output Float Delay	4.0	19	ns	(4)
SYNCHRONOUS INPUT TIMINGS					
T_{IS1}	Input Setup to CLKIN — AD[31:0], NMI#, XINT[7:0]#	10		ns	(5)
T_{IH1}	Input Hold from CLKIN — AD[31:0], NMI# XINT[7:0]#	1		ns	(5)
T_{IS2}	Input Setup to CLKIN — RDYRCV# and HOLD	11		ns	(6)
T_{IH2}	Input Hold from CLKIN — RDYRCV# and HOLD	1		ns	(6)
T_{IS3}	Input Setup to CLKIN — RESET#	8		ns	(7)
T_{IH3}	Input Hold from CLKIN — RESET#	1		ns	(7)
T_{IS4}	Input Setup to RESET# — ONCE#, STEST	8		ns	(8)
T_{IH4}	Input Hold from RESET# — ONCE#, STEST	1		ns	(8)
RELATIVE OUTPUT TIMINGS					
T_{LXL}	ALE/ALE# Width	0.5T_C - 8		ns	(9)
T_{LXA}	Address Hold from ALE/ALE# Inactive	0.5T_C - 8		ns	Equal Loading (9)
T_{DXD}	DT/R# Valid to DEN# Active	0.5T_C - 8		ns	Equal Loading (9)

NOTE: Refer to Table 8 for note definitions for this table.

Table 7. 80L960JA/JF AC Characteristics (16 MHz) (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
BOUNDARY SCAN TEST SIGNAL TIMINGS					
T_{BSF}	TCK Frequency		0.5 T_F	MHz	
T_{BSCH}	TCK High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	4		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	6		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	(1, 10)
T_{BSOF1}	TDO Float Delay	3	36	ns	(1, 10)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	35	ns	(1, 10)
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	36	ns	(1, 10)
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	4		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	6		ns	

NOTE: Refer to Table 8 for note definitions for this table.

Table 8. Note Definitions for Table 7 “80L960JA/JF AC Characteristics (16 MHz)”

1. Not tested.
2. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal clock, the jitter frequency spectrum should not have any power peaking between 500 KHz and 1/3 of the CLKIN frequency.
3. Inactive ALE/ALE# refers to the falling edge of ALE and the rising edge of ALE#. For inactive ALE/ALE# timings, see Relative Output Timings in Table 7.
4. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested, but is designed to be no longer than the valid delay.
5. AD[31:0] are synchronous inputs. Setup and hold times must be met for proper processor operation. NMI# and XINT[7:0]# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, NMI# and XINT[7:0]# must be asserted for a minimum of two CLKIN periods to guarantee recognition.
6. RDYRCV# and HOLD are synchronous inputs. Setup and hold times must be met for proper processor operation.
7. RESET# may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
8. ONCE# and STEST must be stable at the rising edge of RESET# for proper operation.
9. Guaranteed by design. May not be 100% tested.
10. Relative to falling edge of TCK.

1.5.1 AC Test Conditions and Derating Curves

The AC Specifications in Section 1.5, “AC Specifications are tested with the 50 pF load indicated in Figure 1. Figure 2 shows how timings vary with load capacitance; Figure 3 shows how output rise and fall times vary with load capacitance.

Figure 1. AC Test Load

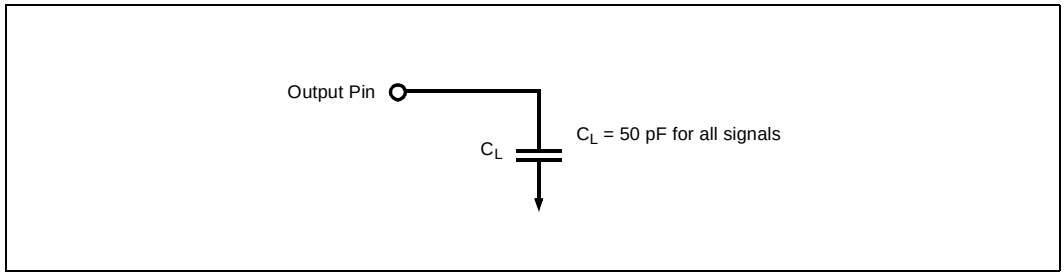


Figure 2. Output Delay or Hold vs. Load Capacitance

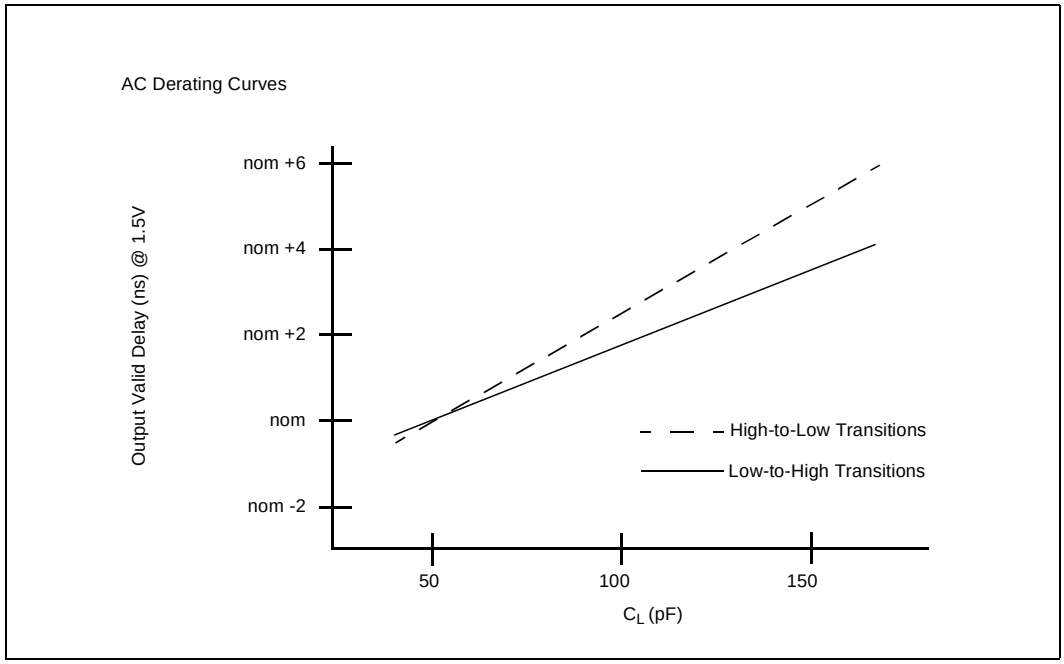
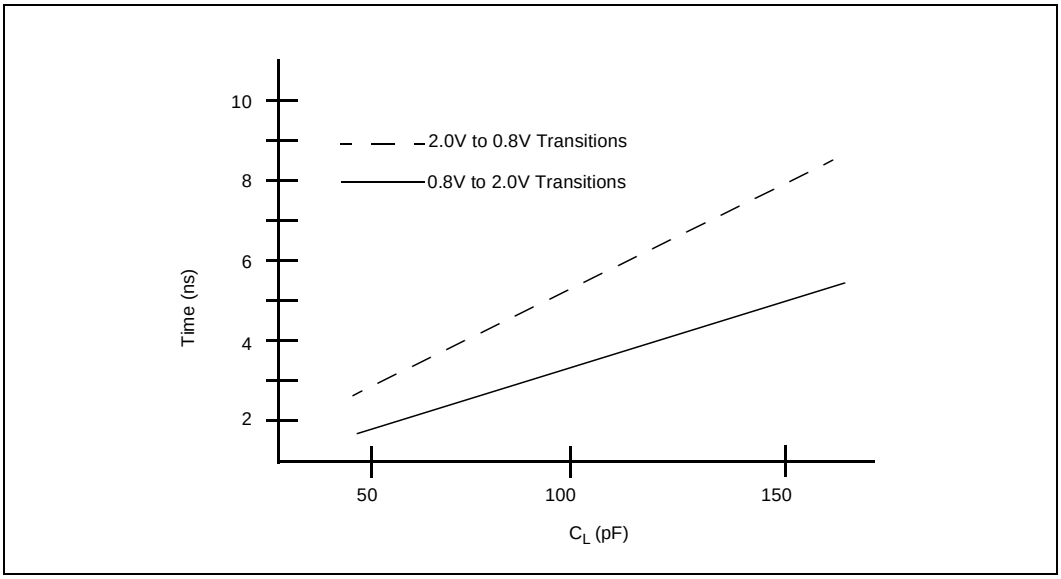


Figure 3. Rise and Fall Time Derating



1.5.2 AC Timing Waveforms

Figure 4. CLKIN Waveform

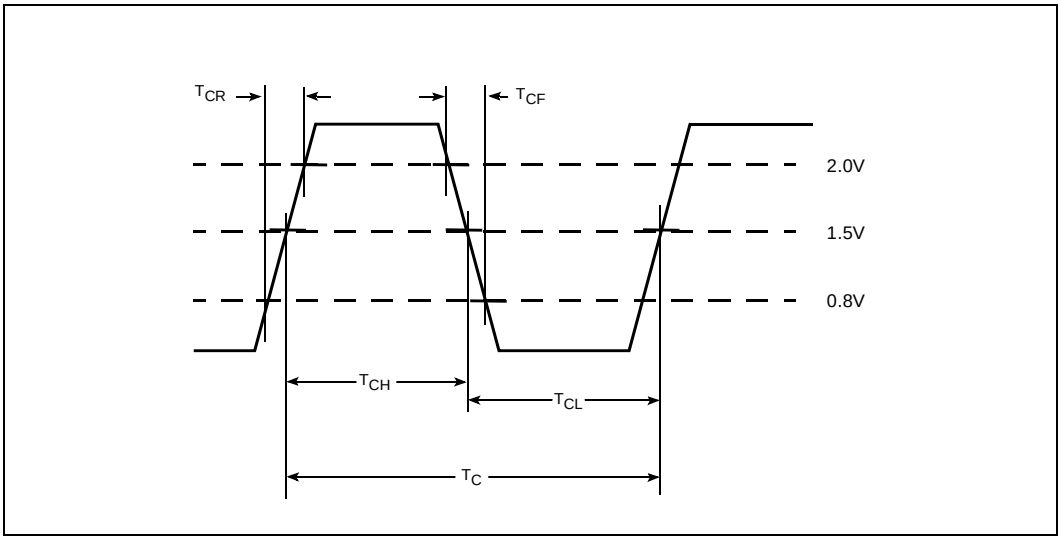


Figure 5. Output Delay Waveform for T_{OV1}

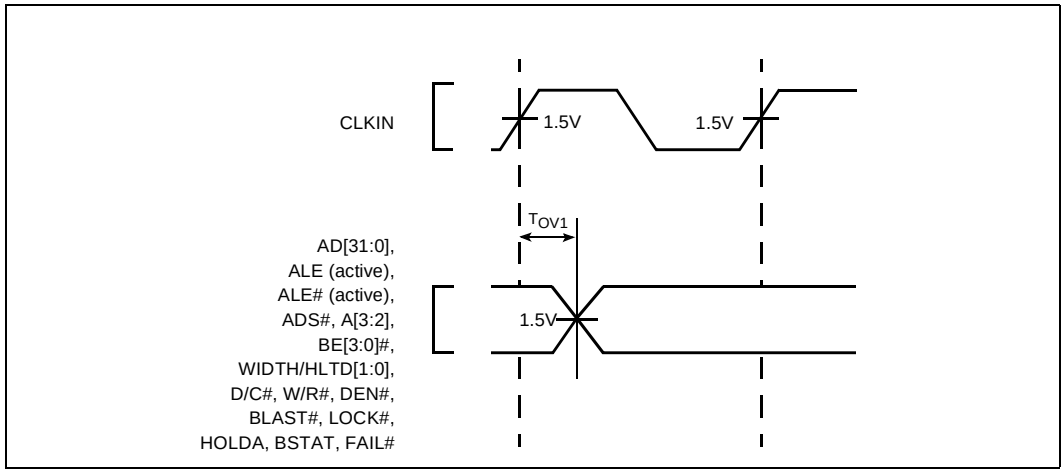


Figure 6. Output Float Waveform for T_{OF}

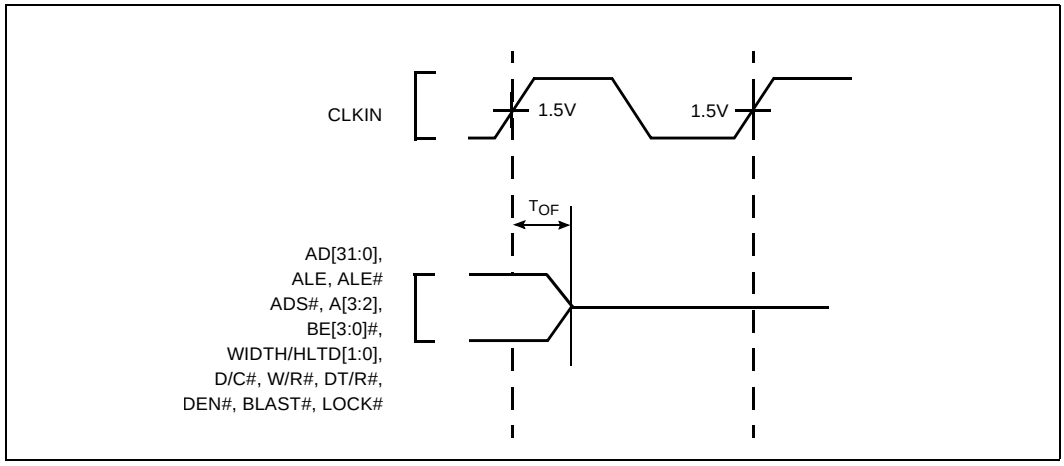


Figure 7. Input Setup and Hold Waveform for T_{IS1} and T_{IH1}

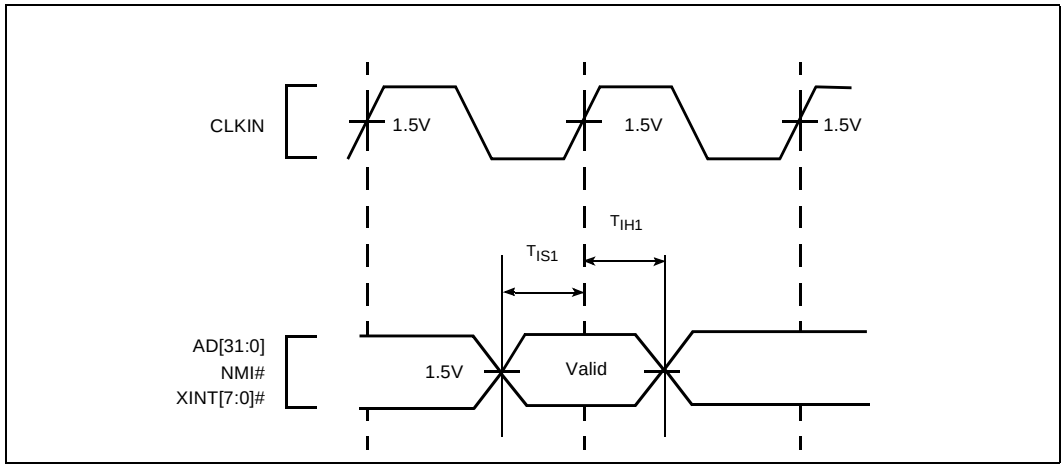


Figure 8. Input Setup and Hold Waveform for T_{IS2} and T_{IH2}

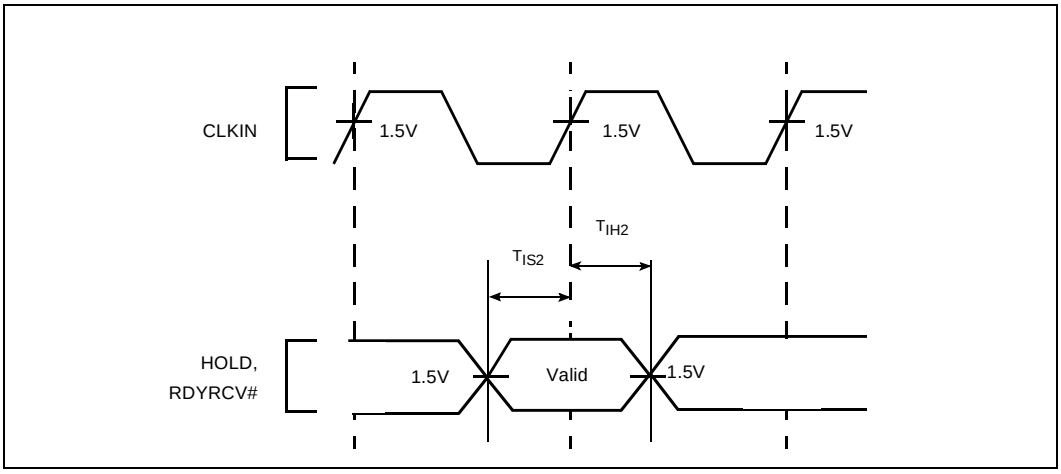


Figure 9. Input Setup and Hold Waveform for T_{IS3} and T_{IH3}

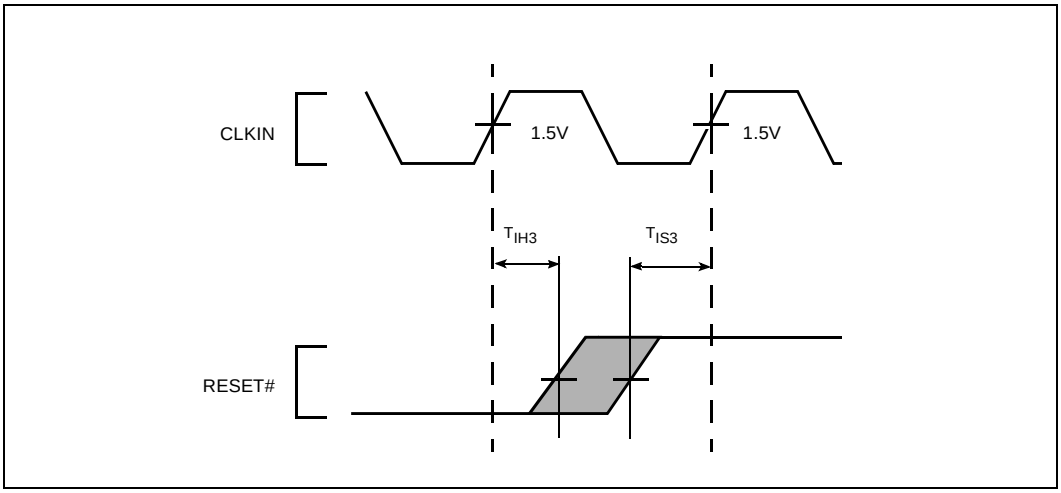


Figure 10. Input Setup and Hold Waveform for T_{IS4} and T_{IH4}

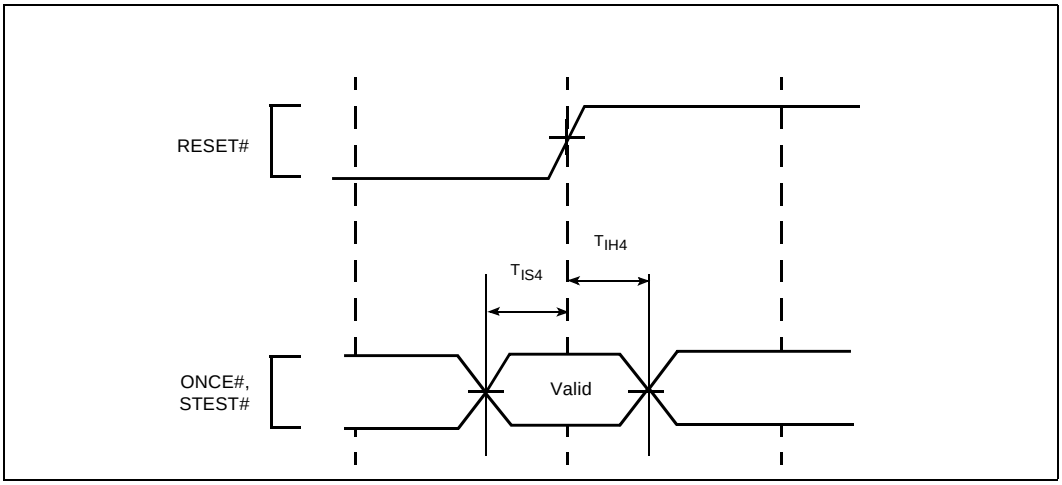


Figure 11. Relative Timings Waveform for T_{LXL} and T_{LXA}

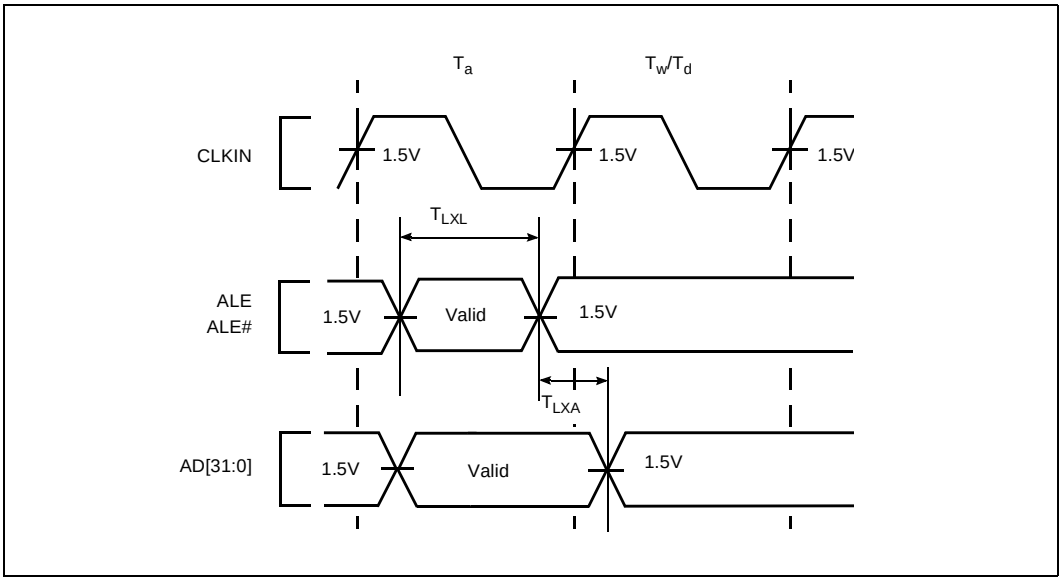


Figure 12. DT/R# and DEN# Timings Waveform

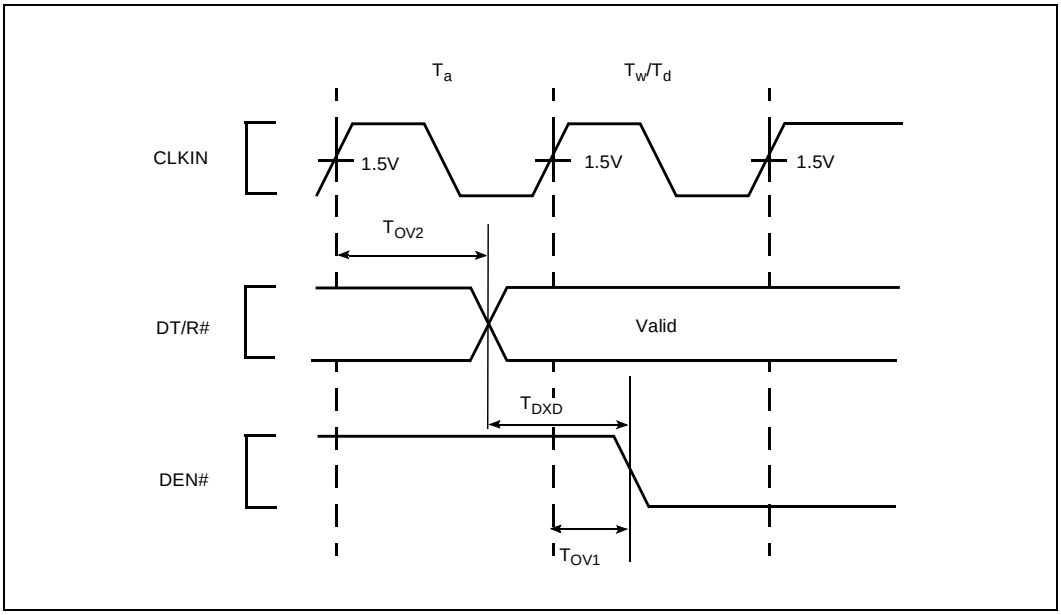


Figure 13. TCK Waveform

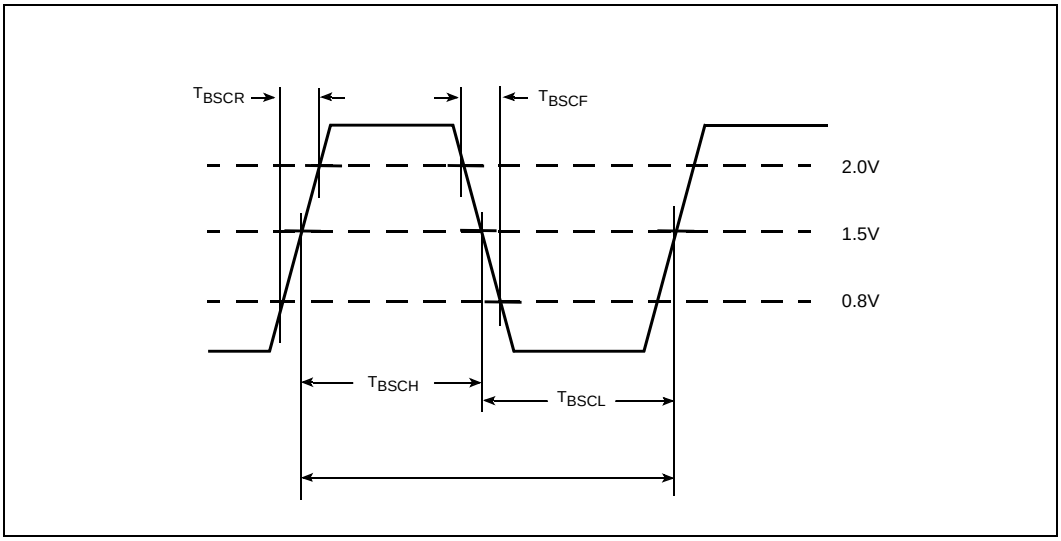


Figure 14. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}

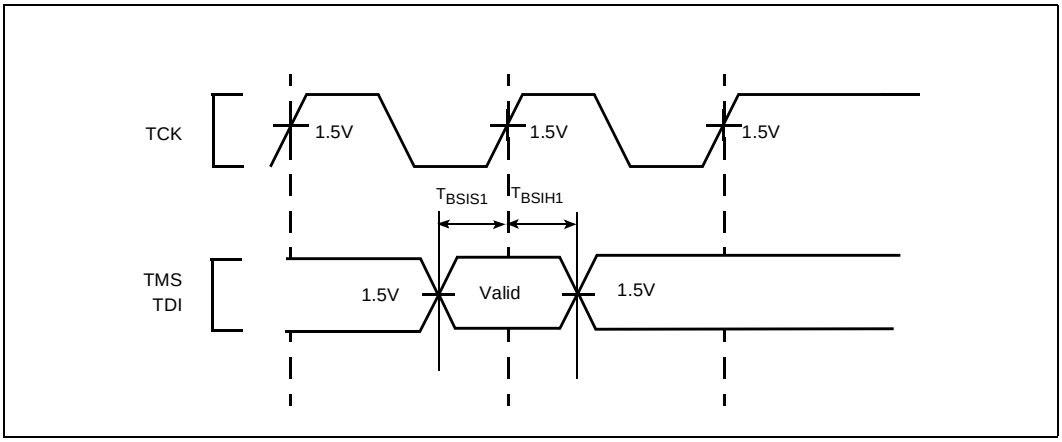


Figure 15. Output Delay and Output Float Waveform for T_{BSOV1} AND T_{BSOF1}

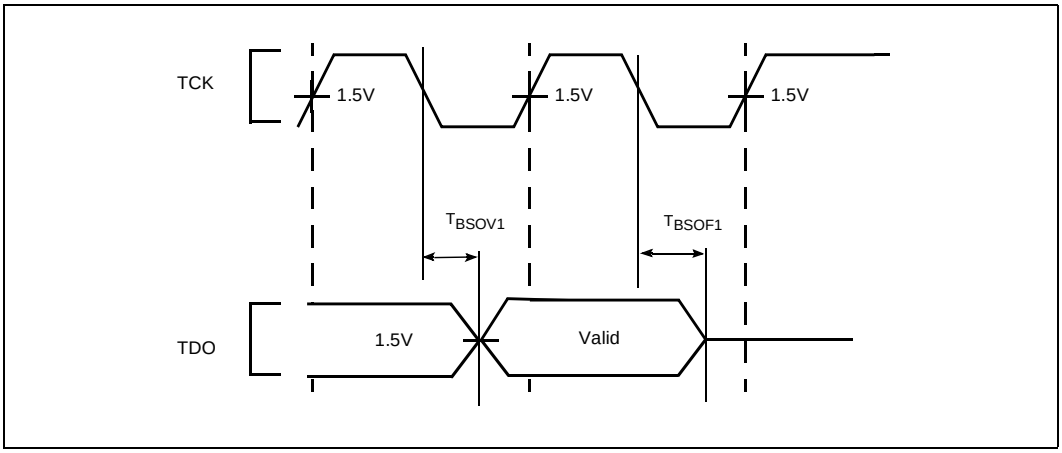


Figure 16. Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2}

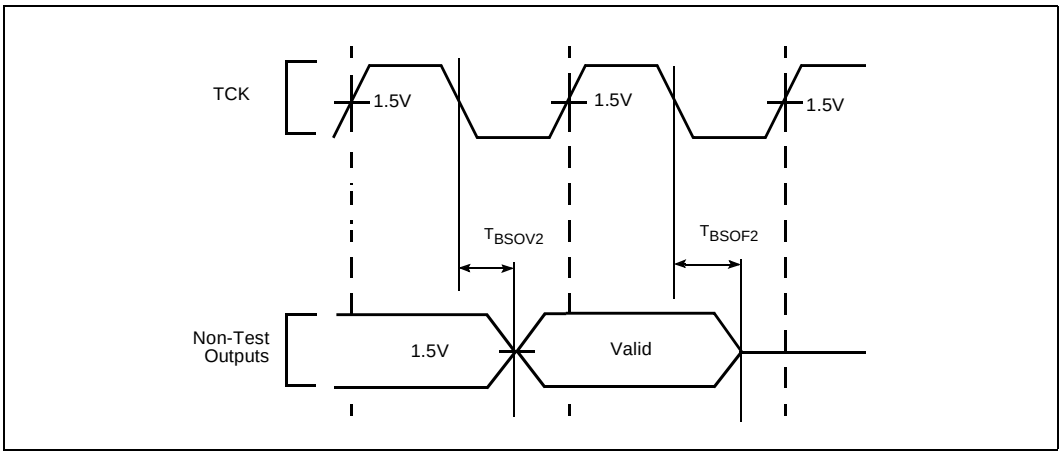


Figure 17. Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2}