8101/8104 Gigabit Ethernet Controller

Datasheet

The 8101/8104 Gigabit Ethernet Controller is a complete media access controller (MAC sublayer) with integrated coding logic for fiber and short haul copper media (8-bit/10-bit Physical Coding Sublayer) (8B/10B PCS) for 1000 Mbit/s Gigabit Ethernet systems.

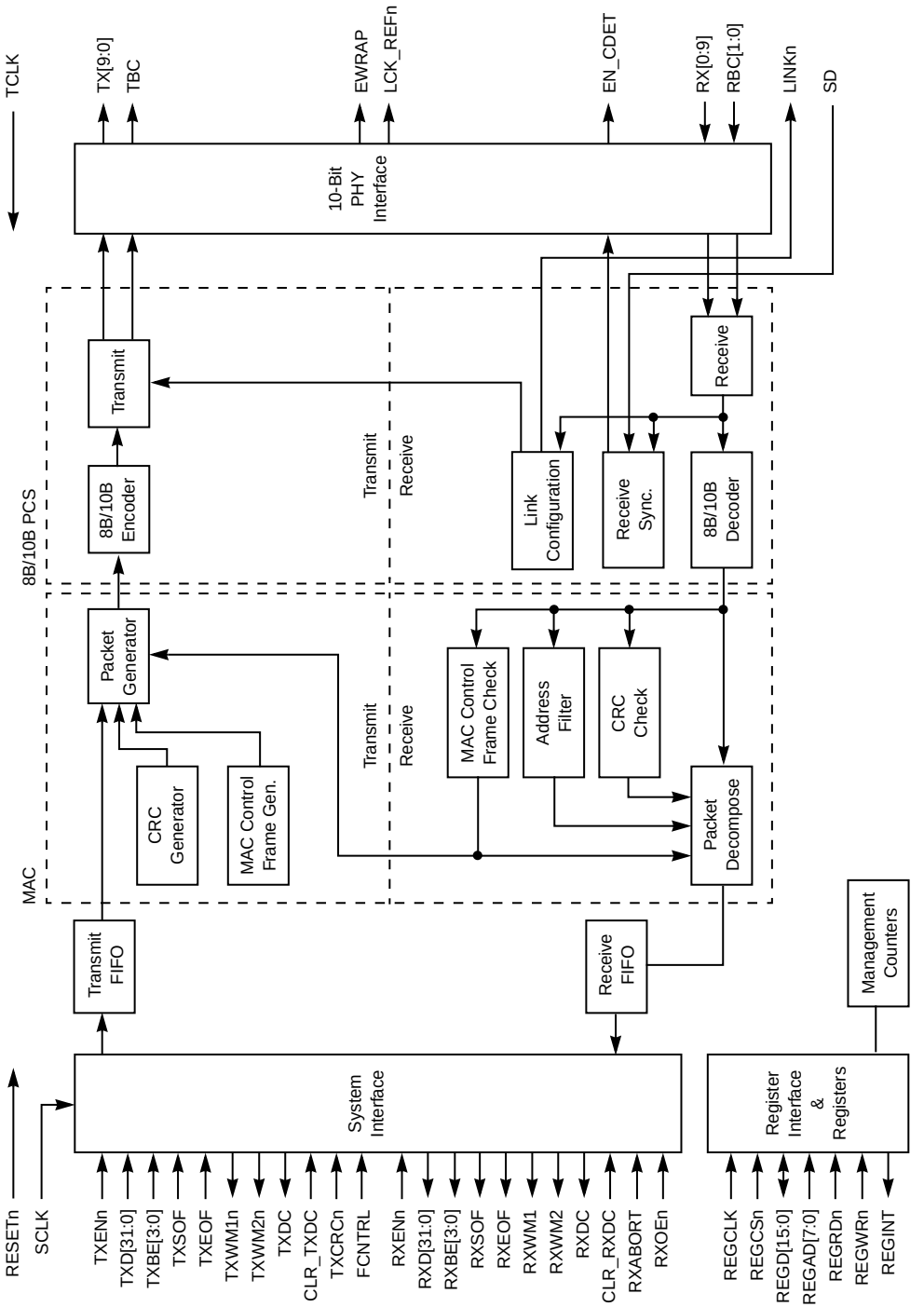
The 8104 is functionally the same as the 8101 except that the 8104 is in a 208-pin Ball Grid Array (BGA) package and the 8101 is in a 208-pin Plastic Quad Flat Pack (PQFP) package.

The Controller consists of a 32-bit system interface, receive/transmit First In First Out (FIFO) buffers, a full-duplex Ethernet Media Access Controller (MAC), an 8B/10B PCS, a 10-bit Physical Layer Device (PHY) interface, and a 16-bit register interface. The controller also contains all the necessary circuitry to implement the IEEE 802.3x Flow Control Algorithm. Flow control messages can be sent automatically without host intervention. Figure 1 is a block diagram of the controller.

The controller contains 53 counters which satisfy the management objectives of the Remote Monitoring (RMON) Statistics Group MIB, (RFC 1757), Simple Network Management Protocol (SNMP) Interfaces Group (RFC 1213 and 1573), Ethernet-like Group MIB (RFC 1643), and Ethernet MIB (IEEE 802.3z Clause 30). The controller also contains 136 internal 16-bit registers that can be accessed through the register interface. These registers contain configuration inputs, status outputs, and management counter results.

The 8101/8104 is ideal as an Ethernet controller for Gigabit Ethernet switch ports, uplinks, backbones, and adapter cards.

Figure 1 8101/8104 Block Diagram



Features

The 8101/8104 provides the following features.

- Combined Ethernet MAC and 8B/10B PCS
- 1000 Mbits/s data rate
- 64-bit, 66 MHz external bus interface (4 Gbits/s bandwidth)
- 10-bit interface to external SERDES chip
- 16-bit interface to internal registers and management counters
- Full RMON, SNMP, and Ethernet management counter support
- Independent receive and transmit FIFOs with programmable watermarks
  - 16 Kbyte receive FIFO size
  - 4 Kbyte Transmit FIFO size
- AutoNegotiation algorithm on chip
- Full duplex only
- Flow control per IEEE 802.3x
- Automatic CRC generation and checking
- Automatic packet error discarding
- Programmable transmit start threshold
- Interrupt capability
- Supports fiber and short haul copper media
- 3.3 V power supply, 5 V tolerant inputs
- Meets all applicable IEEE 802.3 and 802.3z specifications

Transmit Data Path

Data is input to the system from an external bus. The data is then sent to the transmit FIFO. The transmit FIFO provides temporary storage of the data until it is sent to the MAC transmit section. The transmit MAC formats the data into an Ethernet packet according to IEEE 802.3

specification. The transmit MAC also generates MAC control frames and includes logic for AutoNegotiation. The Ethernet frame packet is then sent to the 8B/10B PCS.

The 8B/10B PCS encodes the data and adds appropriate framing delimiters to create 10-bit symbols as specified in IEEE 802.3. The 10-bit symbols are then sent to the 10-bit PHY interface for transmission to an external PHY device.

Receive Data Path

The 10-bit PHY interface receives incoming encoded data from an external PHY device. The incoming encoded data must be encoded in the 10-bit PHY format specified in IEEE 802.3z. The incoming encoded data is then sent to the receive 8B/10B PCS, which strips off the framing delimiters, decodes the data, and converts the encoded data into an Ethernet packet according to the IEEE 802.3 specifications. The Ethernet packet data is then sent to the receive MAC section.

The receive MAC section disassembles the packet, checks the validity of the packet against certain error criteria and address filters, and checks for MAC control frames. The receive MAC then sends valid packets to the receive FIFO. The receive FIFO provides temporary storage of data until it is demanded by the system interface. The system interface outputs the data to an external bus.

Register Structure

The controller has 136 internal 16-bit registers. Twenty-two registers are available for setting configuration inputs and reading status outputs. The remaining 114 registers are associated with the management counters.

The register interface is a separate internal register bidirectional 16-bit data bus to set configuration inputs, read status outputs, and access management counters.

Ethernet Frame Format

Information in an Ethernet network is transmitted and received in packets or frames. The basic function of the controller is to process Ethernet frames. An Ethernet frame is defined in IEEE 802.3 and consists of a preamble, start of frame delimiter (SFD), destination address (DA), source address (SA), length/type field (L/T), data, frame check sequence (FCS), and interpacket gap (IPG).

An Ethernet frame is specified by IEEE 802.3 to have a minimum length of 64 bytes and a maximum length of 1518 bytes, exclusive of the preamble and SFD. Packets that are less than 64 bytes or greater than 1518 bytes are referred to as undersize and oversize packets, respectively.

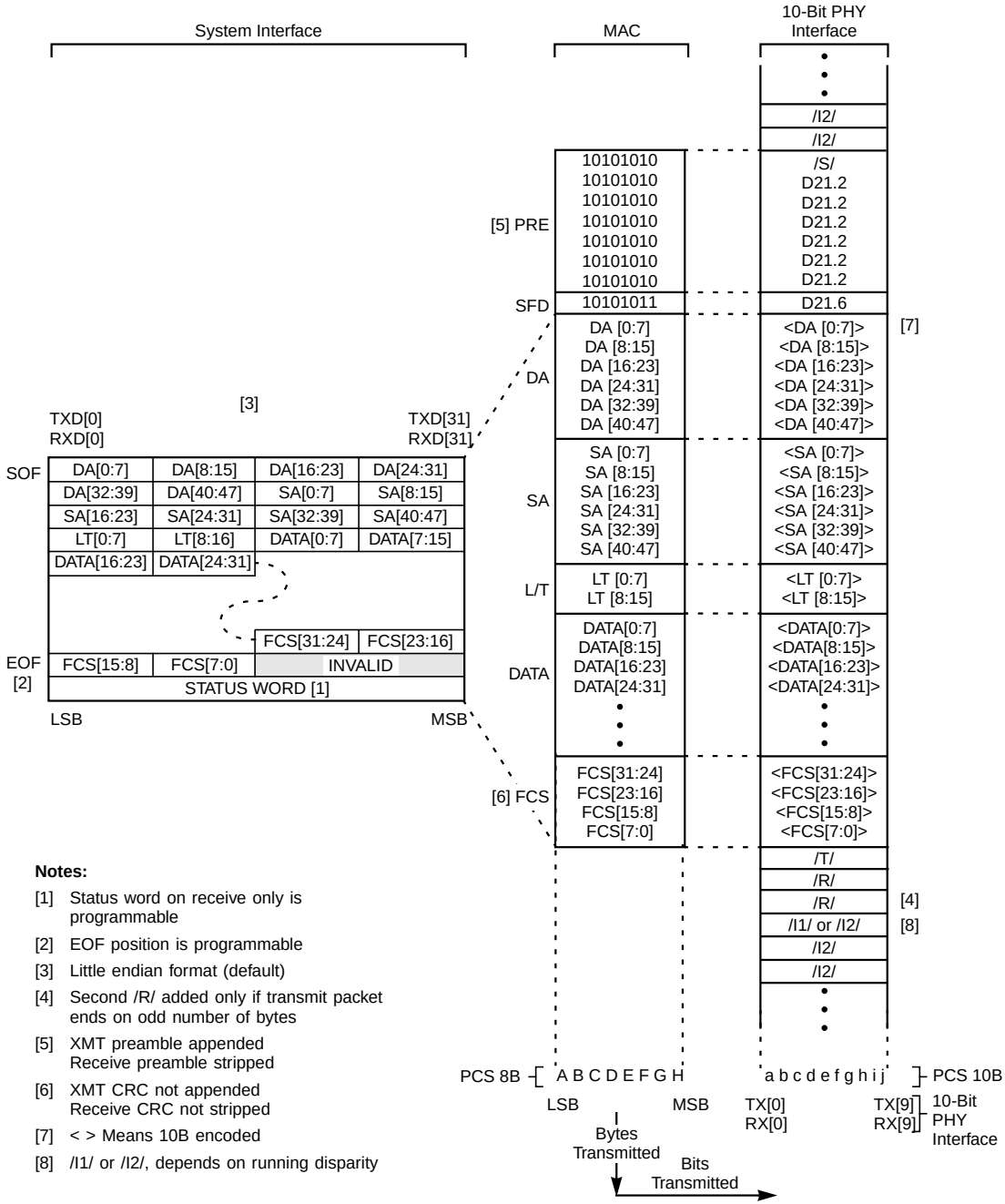
System Interface

The system interface is a 64-bit wide data interface consisting of separate 32-bit data buses for transmit and receive.

Data Format and Bit Order

The format of the data word on TXD[31:0] and RXD[31:0] and its relationship to the MAC frame format and 10-bit PHY interface format is shown in Figure 2. Note that the controller can be programmed to append an additional 32-bit status word to the end of the receive packet.

Figure 2 Frame Formats and Bit Ordering



Notes:

[1] Status word on receive only is programmable

[2] EOF position is programmable

[3] Little endian format (default)

[4] Second /R/ added only if transmit packet ends on odd number of bytes

[5] XMT preamble appended
Receive preamble stripped

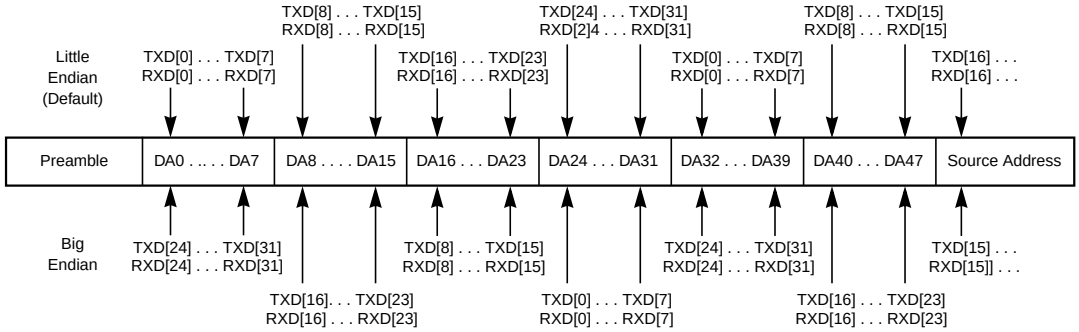
[6] XMT CRC not appended
Receive CRC not stripped

[7] < > Means 10B encoded

[8] /I1/ or /I2/, depends on running disparity

The byte order is little endian format mode (default). If the controller is placed in big endian format, the byte order shown in Figure 3 is reversed, DA[0:7] occurs on pins RXD[24:31], DA[24:31] occurs on pins RXD[0:7]and so on. The endian bit affects all bytes in the frame including the receive status word (if appended). The difference between little endian and big endian format is illustrated in Figure 3.

Figure 3 Little Endian vs. Big Endian Format



Transmit

The transmit portion of the system interface consists of 45 signals:

- 32 transmit data input bits (TXD[31:0])
- One transmit enable (TXENn)
- Four transmit byte enable inputs (TXBE[3:0])
- Two transmit start of frame and end of frame inputs (TXSOFn and TXEOFn)
- Two transmit FIFO watermark outputs (TXWM1n and TXWM2n)
- One transmit discard output (TXDC)
- One transmit discard clear input (CLR_TXDC)
- One transmit CRC enable input (TXCRCn)
- One flow control enable input (FCNTRL)

All receive and transmit data is clocked in and out on the rising edge of the system clock, SCLK. SCLK must operate between 33–66 MHz.

Receive

The receive portion of the system interface consists of 45 signals:

- 32 receive output data bits (RXD[31:0])
- One receive enable input (RXENn)
- Four receive byte enable outputs (RXBE[3:0])
- Two receive start of frame and end of frame outputs (RXSOF and RXEOF)
- Two receive FIFO watermark outputs (RXWM1 and RXWM2)
- One receive discard output (RXDC)
- One receive discard clear input (CLR_RXDC)
- One receive packet abort input (RXABORT)
- One receive output enable (RXOEn)

All receive and transmit data is clocked in and out with the system clock, SCLK, which must operate between 33–66 MHz.

Transmit MAC

To generate an Ethernet MAC frame from the transmit FIFO packet, the transmit MAC section:

- generates preamble and SFD
- pads undersize packets with zeros to meet minimum packet size requirements
- calculates and appends a CRC value to the packet
- maintains a minimum interpacket gap

Each of the above four operations can be individually disabled and altered if desired. The transmit MAC then sends the fully formed Ethernet packet to the 8B/10B PCS block for encoding. The transmit MAC section also generates MAC control frames.

Receive MAC

The receive MAC section performs the following operations to disassemble Ethernet packets received from the receive 8B/10B PCS section:

- strips off the preamble and SFD
- strips off the CRC
- checks the destination address against the address filters to determine packet validity
- checks frame validity against the discard conditions
- checks the length/type field for MAC control frames

Each of the above operations can be individually disabled and altered, if desired. The receive MAC then sends valid packets to the receive FIFO for storage.

Transmit FIFO

The transmit FIFO acts as a temporary buffer between the system interface and transmit MAC section. The transmit FIFO size is 4 Kbytes. Data is clocked into the transmit FIFO with the 33–66 MHz system interface clock, SCLK. Data is automatically clocked out of the transmit FIFO with the 125 MHz 8B/10B PCS clock whenever a full packet has been loaded into the FIFO (an EOF is written into the FIFO on the system interface), or the FIFO data exceeds the transmit FIFO AutoSend threshold. There are two programmable watermark outputs, TXWM1n and TXWM2n, which aid in managing the data flow into the transmit FIFO.

Receive FIFO

The receive FIFO acts as a temporary buffer between the receive MAC section and system interface. The receive FIFO size is 16 kbytes. Data is clocked into the receive FIFO with the 125 MHz 8B/10B PCS clock. Data is clocked out of the receive FIFO with the 33–66 MHz system

interface clock, SCLK. There are two programmable watermark outputs, RXWM1 and RXWM2, which aid in managing the data flow out of the receive FIFO.

8B/10B PCS

The 8B/10B PCS encodes the data and adds approiate framing delimiters to create 10-bit symbols as specified in IEEE 802.3.

Transmit

The transmit 8B/10B PCS section accepts Ethernet formatted packet data from the transmit MAC and:

- Encodes the data with the 8B/10B encoder
- Adds the start of packet delimiter
- Adds the end of packet delimiter
- Adds the idle code stream
- Formats the packet according to the 10-bit PHY format defined in IEEE 802.3z

The 8B/10B encoded data stream is then sent to the transmit 10-bit PHY interface for transmission.

The transmit 8B/10B PCS section also generates the AutoNegotation code stream when the controller is in the AutoNegotation process.

Receive

The receive 8B/10B PCS section takes the 8B/10B encoded packet data from the incoming 10-bit PHY interface and:

- Acquires and maintains word synchronization
- Strips off the start of packet delimiter
- Strips off the end of packet delimiter
- Strips off the idle code stream
- Decodes the data with the 8B/10B decoder
- Converts the packet to the Ethernet packet format

The Ethernet packet is then sent to the receive MAC for processing.

The receive 8B/10B PCS section also decodes the AutoNegotation code stream when the controller is in the AutoNegotation process.

8B/10B Encoder

The 8B/10B encoder converts each data byte of a packet into a unique 10-bit word as defined in IEEE 802.3z

The encoder also converts the start of packet delimiter, end of packet delimiter, idle code streams, and AutoNegotation code streams into unique 10B code words. These unique 10B code words are referred to as ordered sets.

The 8B/10B encoder also keeps the running disparity of the outgoing 10B word as close as possible to zero. Running disparity is the difference between the number of ones and zeros transmitted on the outgoing bitstream. The algorithm for calculating running disparity is defined in IEEE 802.3z.

10-Bit PHY Interface

The 10-bit PHY interface is a standardized interface between the 8B/10B PCS section and an external physical layer device. The 10-bit PHY interface meets all the requirements outlined in IEEE 802.3z. The controller can directly connect, without any external logic, to any physical layer device that also complies with the IEEE 802.3z 10-bit interface specifications.

The 10-bit PHY interface consists of 26 signals as follows:

- 10-bit transmit data output bits (TX[9:0])
- Transmit clock output (TBC)
- 10-bit receive data input bits (RX[9:0])
- Two receive clock inputs (RBC0 and RBC1)
- Comma detect enable output (EN_CDET)
- Loopback output (EWRAP)
- Receiver lock output (LCK_REFn)

Packet Discard

The controller can be programmed to discard receive and transmit packets when certain error conditions are detected. The detection of these error conditions can occur in the MAC, FIFO, or 8B/10B PCS sections.

Transmit Discards

Transmit packets are automatically discarded if certain error conditions are detected. These error conditions are described in Table 1. When a discard error is detected for a transmit packet, any remaining data for that packet being input from the system interface is ignored, a /V/ code is appended to the end of the packet to indicate an error to a remote station, and TXDC is asserted if the packet was being input from the system interface when the discard occurred.

Table 1 Transmit Discard Conditions

Discard Condition	Description
Transmit FIFO Underflow	TX FIFO empty. Packet transmission to 8B/10B PCS halted. Partially transmitted packet is terminated with a /V/ code, followed by normal /I/ codes.
Transmit FIFO Overflow	TX FIFO full. No more data accepted from the system interface. Partially transmitted packet is terminated with a /V/ code, followed by normal /I/ codes.

Receive Discards

Receive packets can be discarded if the error conditions listed in Table 2 are detected. The discard behavior is dependent on whether or not the packet is being output on the system interface when the discard condition is detected. If the packet containing the error is not being output on the system interface when the discard condition is detected (an internal discard) the packet is discarded, (all data from the packet containing the error is flushed from the receive FIFO). If the packet containing the error is being output on the system interface when the discard condition is detected (an external discard) the packet is

automatically discarded. For both internal and external discarded packets, the appended status word is updated to reflect the discard error condition.

Table 2 Receive Discard Conditions

Discard Condition	Description
Receive FIFO overflow	Receive FIFO full. No more data accepted from the 8B/10B PCS.
CRC error	Receive packet has a CRC error.
Undersize packet	Receive packet is less than 64 bytes, exclusive of preamble and SFD.
Oversize packet	Receive packet is greater than maximum packet size, exclusive of preamble and SFD.
PCS codeword error	Receive packet contains at least one word with an 8B/10BPCS coding error.

Counters

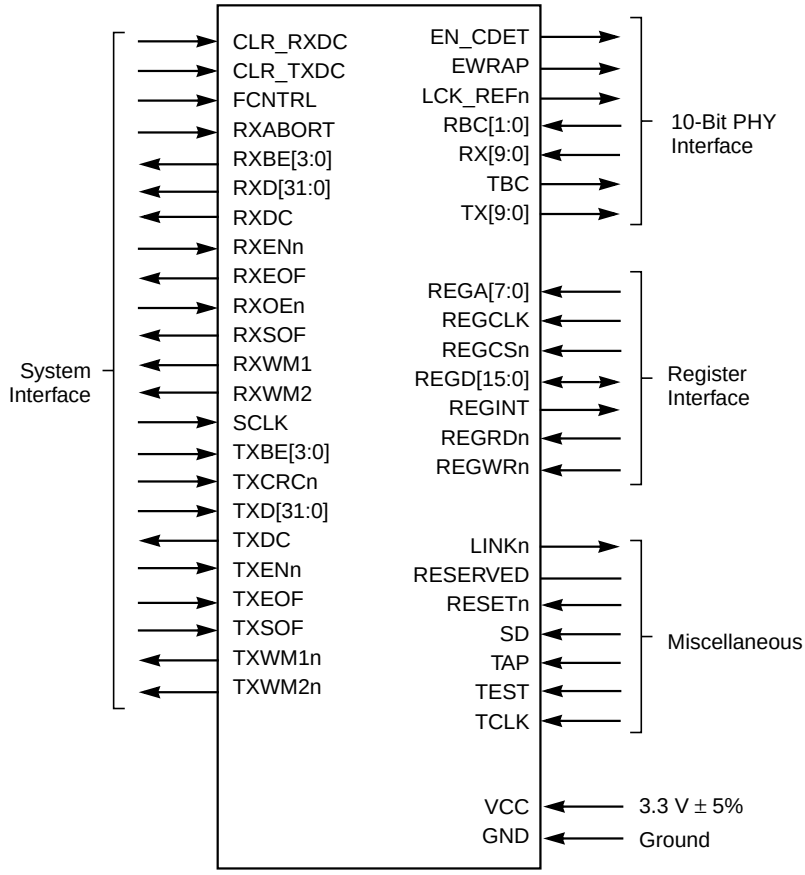
The controller has a set of 53 management counters. Each counter tabulates the number of times a specific event occurs. These counters provide the necessary statistics to completely support the following specifications:

- RMON Statistics Group (IETF RFC 1757)
- SNMP Interfaces Group (IETF RFC 1213 and 1573)
- Ethernet-Like MIB (IETF RFC 1643)
- Ethernet MIB (IEEE 802.3z, clause 30)

Signal Descriptions

This section describes the controller interfaces and the signals used in each interface. Figure 4 is a diagram of the 8101/8104 signals.

Figure 4 8101/8104 Interface Diagram



System Interface Signals

This section describes the 8101/8104 system interface signals.

CLR_RXDC **Clear RXDC** **Input**

When CLR_RXDC is asserted, the RXDC pin is cleared. When CLR_RXDC is LOW, the RXDC pin is not cleared. CLR_RXDC is clocked in on the rising edge of the system clock, SCLK.

This pin only clears RXDC when AutoClear mode is disabled. When AutoClear mode is enabled, this pin is ignored and RXDC is automatically cleared two clock cycles after RXEOF is asserted.

CLR_TXDC **Clear TXDC** **Input**

When CLR_TXDC is HIGH, the TXDC pin is cleared. When CLR_TXDC is LOW, the TXDC pin is not cleared. TXDC is clocked in on the rising edge of the system clock, SCLK.

This pin only clears TXDC when AutoClear mode is disabled. When AutoClear mode is enabled, this pin is ignored and TXDC is automatically cleared two clock cycles after TXEOF is asserted.

FCNTRL **Flow Control Enable** **Input**

When FCNTRL is HIGH, transmitter automatically transmits a MAC control pause frame. When FCNTRL is LOW, the controller resumes normal operation. FCNTRL is clocked in on the rising edge of the system clock, SCLK.

RXABORT **Receive FIFO Data Abort** **Input**

When RXABORT is asserted, the packet being read out on RXD[31:0] is aborted and discarded. When LOW, the packet is not aborted and discarded. RXABORT is clocked in on the rising edge of the system clock, SCLK.

RXBE[3:0] **Receive Byte Enable** **Output**

These outputs determine which bytes of the current data on RXD[31:0] contain valid data. RXBE[3:0] is clocked out of the device on the rising edge of the system interface clock, SCLK.

RXD[31:0] **Receive Data** **Output**

This output bus contains the 32-bit received data word that is clocked out on the rising edge of the system interface clock, SCLK.

RXDC **Receive Packet Discard** **Output**

When HIGH, device detects that current packet being output on the system interface has an error and should be discarded. When LOW, no discard.

Asserting the RXABORT pin or setting the AUTORXAB bit in register 9 (Configuration 3 Register) automatically discards the packet being output. RXDC is clocked out on the rising edge of the system clock, SCLK.

If AutoClear mode is not enabled, this output is latched HIGH and stays latched until cleared with the assertion of the CLR_RXDC pin. If AutoClear mode is enabled, this output is latched HIGH and automatically clears itself two clock cycles after RXEOF is asserted. RXDC can also be cleared with RXABORT if programmed to do so.

RXENn **Receive Enable** **Input**

This input must be asserted active LOW to enable the current data word to be clocked out of the receive FIFO on RXD[31:0]. RXENn is clocked in on the rising edge of the system interface clock, SCLK.

RXEOF **Receive End Of Frame** **Output**

This output is asserted on the same clock cycle when the last word of the packet is being read out of the receive FIFO on RXD[31:0]. RXEOF is clocked out of the device on the rising edge of the system interface clock, SCLK.

RXOEn **Receive Output Enable** **Input**

When LOW, all receive outputs are active. When HIGH, receive outputs (RXD[31:0], RXBE[3:0], RXSOF, RXEOF) are high-impedence.

RXSOF **Receive Start Of Frame** **Output**

This output is asserted on the same clock cycle when the first word of the packet is being read out of the receive FIFO on RXD[31:0]. RXSOF is clocked out of the device on the rising edge of the system interface clock, SCLK.

RXWM1 **Receive FIFO Watermark 1** **Output**

When RXWM1 is LOW, the receive FIFO data is less than or equal to the receive FIFO watermark 1 threshold. When HIGH, the receive FIFO data is greater than the watermark. RXWM1 is clocked out on the rising edge of the system clock, SCLK. Data is valid on RXD[31:0] when either RXWM1 or RXWM2 is asserted, independent of RXENn.

RXWM2 **Receive FIFO Watermark 2** **Output**

When RXWM2 is LOW, the receive FIFO data is less than or equal to the receive FIFO watermark 2 threshold and no EOF in FIFO. When HIGH, the receive FIFO data is greater than the watermark. RXWM2n is clocked out on the rising edge of the system clock, SCLK. Data is valid on RXD[31:0] when either RXWM1 or RXWM2 is asserted, independent of RXENn.

SCLK **System Interface Clock** **Input**

This input clocks data in and out of the transmit and receive FIFOs on TXD[31:0] and RXD[31:0], respectively. All system interface inputs and outputs are also clocked in and out on the rising edge of SCLK, with the exception of RXOEn. SCLK clock frequency must be between 33–66 MHz.

TXBE[3:0] **Transmit Byte Enable** **Input**

These inputs determine which bytes of the current 32-bit word on TXD[31:0] contain valid data. TXBE[3:0] is clocked into the device on the rising edge of the system interface clock, SCLK.

TXCRCn **Transmit CRC Enable** **Input**

When TXCRC is LOW, CRC is calculated and appended to the current packet being input on the system interface. When TXCRC is HIGH, CRC is not calculated. TXCRCn is clocked in on the rising edge of the system clock, SCLK, and must be asserted on the same SCLK clock cycle as TXSOF.

TXD[31:0] **Transmit Data** **Input**

This input bus contains the 32-bit data word that is clocked into the transmit FIFO on the rising edge of the system interface clock, SCLK.

TXDC **Transmit Packet Discard** **Output**

When TXDC is HIGH, the controller detects that the current packet being input on the system interface has an error, the rest of packet is ignored. When LOW, The packet is not discarded. TXDC is clocked out on thr rising edge of the system clock.

If AutoClear mode is not enabled, this output is latched HIGH and stays latched until cleared with the assertion of the CLR_TXDC pin. If the AutoClear mode is enabled, this output is latched HIGH and automatically clears itself two clock cycles after TXEOF is asserted.

TXENn **Transmit Enable** **Input**

This input must be low to enable the current data word on TXD[31:0] to be clocked into the transmit FIFO. TXENn is clocked in on the rising edge of the system interface clock, SCLK.

TXEOF **Transmit End Of Frame** **Input**

This input must be asserted on the same clock cycle when the last word of the packet is being clocked in on TXD[31:0]. TXEOF is clocked into the device on the rising edge of the system interface clock, SCLK.

TXSOF **Transmit Start Of Frame** **Input**

This input must be asserted in the same clock cycle that the first word of the packet is being clocked in on TXD[31:0]. TXSOF is clocked into the device on the rising edge of the system interface clock, SCLK.

TXWM1n **Transmit FIFO Watermark 1** **Output**

When TXWM1n is HIGH, the transmit FIFO data is less than or equal to the transmit FIFO watermark 1. When LOW, the transmit FIFO data is above the watermark. TXWM1n is clocked out on the rising edge of the system clock, SCLK.

TXWM2n **Transmit FIFO Watermark 2** **Output**

When TXWM2n is HIGH, the transmit FIFO data is less than or equal to the transmit FIFO watermark 2. When LOW, the transmit FIFO data is above the watermark. TXWM2n is clocked out on the rising edge of the system clock, SCLK.

10-Bit PHY Interface Signals

This section describes the 8101/8104 10-Bit PHY interface signals.

EN_CDET **Comma Detect Enable** **Output**
This output is asserted when either the receive 8B/10B PCS state machine is in the loss of synchronization state or the CDET bit is set in Register 9 (Configuration 3 register. This output is typically used to enable the comma detect function in an external physical layer device.

EWRAP **Loopback Output Enable** **Output**
This output is asserted whenever the EWRAP bit is set in Register 9 (Configuration 3 register). This output is typically used to enable loopback in an external physical layer device.

LCK_REFn **Receiver Lock** **Output**
This output is asserted whenever the LCK_REFn bit is set in Register 9 (Configuration 3 register). This output is typically used to enable the receive lock-to-reference mechanism in an external physical layer

RBC[1:0] **Receive Clock** **Input**
The RBC[1:0] signals clock receive data into the controller on the clock rising edge. RBC[1:0] are 62.5 MHz clocks, 180° out of phase, that clock data into the controller on RX[9:0] at an effective rate of 125 MHz. For the device to acquire synchronization, the comma code must be input on RX[9:0] on RBC[1:0] rising edges.

RX[9:0] **Receive Data** **Input**
These inputs contain receive data that are clocked in on the rising edges of RBC[1:0]

TBC **Transmit Clock** **Output**
This output clocks transmit data out on TX[9:0] on its rising edge. TBC is a 125 MHz clock and is generated from TCLK.

TX[9:0] **Transmit Data** **Output**
These interface outputs transmit data on the rising edge of TBC.

Register Interface Signals

This section describes the 8101/8104 register interface signals.

REGA[7:0] **Register Interface Address** **Input**
These inputs provide the address for the specific internal register to be accessed, and are clocked into the device on the rising edge of REGCLK.

REGCLK **Register Interface Clock** **Input**
This input clocks data in and out on REGD[15:0], REGA[7:0], REGRDn, and REGWRn on its rising edge. REGCLK frequency must be between 5–40 MHz.

REGCSn **Register Interface Chip Select** **Input**
This input must be asserted to enable reading and writing data on REGD[15:0] and REGA[7:0]. This input is clocked in on the rising edge of REGCLK.

REGD[15:0] **Register Interface Data Bus** **Bidirectional**
This bus is a bidirectional 16-bit data path to and from the internal registers. Data is read and written from and to the internal registers on the rising edge of the register clock, REGCLK.

REGINT **Register Interface Interrupt** **Output**
This output is asserted when certain interrupt bits in the registers are set, and it remains latched HIGH until all interrupt bits are read and cleared.

REGRDn **Register Interface Read** **Input**
When this input is asserted, the accessed internal register is read (data is output from the register). This input is clocked into the device on the rising edge of REGCLK.

REGWRn **Register Interface Write** **Input**
When this input is asserted, the accessed internal register is written (data is input to the register). This input is clocked into the device on the rising edge of REGCLK.

Micellaneous Signals

This section describes the 8101/8104 micellaneous signals.

LINKn **Receive Link** **Output**
When this signal is HIGH, there is no link. When this signal is asserted, the receive link is synchronized and configured.

RESERVED **Reserved**
These pins are reserved and must be left floating.

RESETn **Reset** **Input**
When this signal is HIGH, controller is in normal operation. When this signal is asserted, controller resets, FIFOs are cleared, counters are cleared, and register bits are set to default values.

SD **Signal Detect** **Input**
When this signal is asserted, data detected on receive 10-bit PHY is valid. When SD is LOW, data is not valid and the 8B/10B PCS receiver is forced to a loss of sync state. This signal is ignored (assumed high) unless the SD_EN bit in Register 9 (Configuration 3) register is cleared.

TAP **3-State All Pins** **Input**
This pin is used for testing purposes only. When asserted, all output and bidirectional pins are placed in a high-impedence state.

TEST **Test Mode** **Input**
This pin is used for factory test and must be tied LOW for proper operation.

TCLK **Transmit Clock** **Input**
This 125 MHz input clock is used by the 8B/10B PCS section and generates the 125 MHz transmit output clock, TBC is used to output data on the 10-bit PHY interface.

Power Supply Signals

This section describes the 8101/8104 power supply signals.

VCC	**Positive Supply** 3.3 V ± 5%	–
GND	**Ground** 0 Volts	–

Specifications

This section describes the specifications of the 8101/8104 Gigabit Ethernet Controller.

Absolute Maximum Ratings

Absolute maximum ratings are limits, which when exceeded may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VCC supply voltage	–0.3 V to +4.0 V
All inputs and outputs	–0.3 V to +5.5 V
Package power dissipation	2.2 Watt @ 70 ˚C
Storage temperature	–65 ˚C to +150 ˚C
Temperature under bias	–10 ˚C to +85 ˚C
Lead temperature (soldering, 10 s)	260 ˚C
Body temperature (soldering, 30 s)	220 ˚C

DC Electrical Characteristics

Table 3 lists and describes the DC electrical characteristics of the 8101/8104. Unless otherwise noted, all test conditions are as follows:

- TA = 0 to +70 ˚C
- VCC = 3.3 V ± 5%
- SCLK = 66 MHz ± 0.01%
- TCLK = 125 MHz ± 0.01%

Table 3 DC Electrical Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
VIL	Input LOW voltage	–	–	0.8	Volt	
VIH	Input HIGH voltage	2	-	5.5	Volt	
IIL	Input LOW current	–	-	–1	µA	VIN = GND
IIH	Input HIGH current	–	–	1	µA	VIN = VCC
VOL	Output LOW voltage	GND	–	0.4	Volt	IOL = –4 mA All except LINKn
		GND	–	1	Volt	IOL = –20 mA LINKn
VOH	Output HIGH voltage	2.4	–	VCC	Volt	IOL = 4 mA All except LINKn
		VCC –1.0	–	VCC	Volt	IOL = 20 mA LINKn
CIN	Input capacitance	–	–	5	pF	
ICC	VCC supply current	–	–	300	mA	No output load

AC Electrical Characteristics

The following tables list and describe the the AC electrical characteristics of the 8101/8104. Unless otherwise noted, all test conditions are as follows:

- TA = 0 to +70 ˚C
- VCC = 3.3 V ± 5%
- SCLK = 66 MHz ± 0.01%
- TCLK = 125 MHz ± 0.01%
- Input conditions:
  - All Inputs: tr, tf ≤ 4 ns, 0.8 V to 2.0 V
- Output loading
  - TBC, TX[9:0]: 10 pF
  - LINK: 50 pF
  - All other digital outputs: 30 pF
- Measurement points:
  - Data active to 3-state: 200 mV change
  - Data 3-state to active: 200 mV change
  - All inputs and outputs: 1.5 Volts

Table 4 Input Clock Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t1	SCLK cycle time	1/33		1/66	1 MHz	
t2	SCLK duty cycle	40		60	%	
t3	TCLK period	7.9992	8	8.0008	ns	
t4	TCLK HIGH time	3.6		4.4	ns	
t5	TCLK LOW time	3.6		4.4	ns	
t6	TCLK to TBC delay	0		8	ns	
t7	REGCLK cycle time	1/5		1/40	1 MHz	
t8	REGCLK duty cycle	40		60	%	

Note: Refer to Figure 5 for timing diagram.

Figure 5 Input Clock Timing

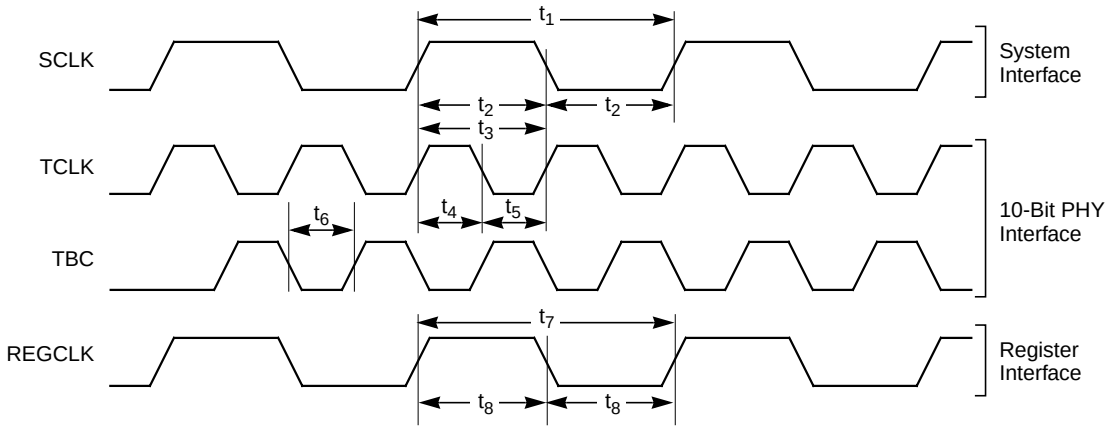
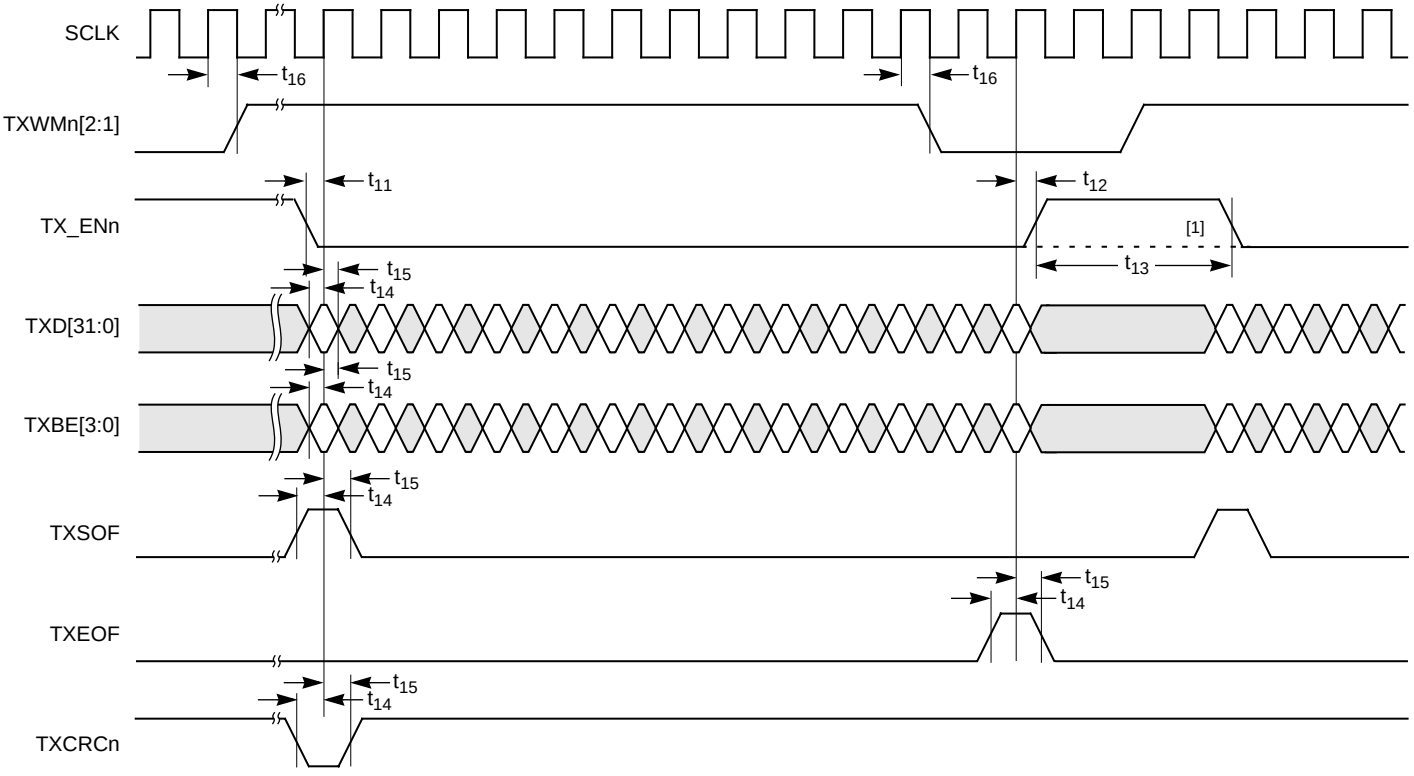


Table 5 Transmit System Interface Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t11	TXENn setup time	5			ns	
t12	TXENn hold time	0			ns	
t13	TXENn deassert time	1 SCLK cycle			ns	
t14	TXD, TXBE, TXSOFn, TXEOF, and TXCRC setup time	5			ns	
t15	TXD, TXBE, TXSOFn, TXEOF, and TXCRC hold time	0			ns	
t16	TXWMn[2:1] delay time	0		8	ns	
t17	TXWMn[2:1] rise/fall time			4	ns	

Note: Refer to Figure 6 for timing diagram.

Figure 6 Transmit System Interface Timing



Note:

[1] Back-to-back packet transmission allowed without TXENn deassertion.

Table 6 Receive System Interface Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t31	RXENn setup time	5			ns	
t32	RXENn hold time	1			ns	
t33	RXENn deassert time	3 SCLK cycles			ns	
t34	RXD, RXBE, RXSOF, RXEOF, and RXWM delay time	0		8	ns	
t35	RXD, RXBE, RXSOF, RXEOF, and RXWM rise/fall time			4	ns	
t41	RXABORT setup time	5			ns	
t42	RXABORT hold time	0			ns	
t43	RXABORT assert to RXWM deassert delay	0		1 SCLK cycle +8 ns	ns	
t46	RXOEn deassert to data High-Z delay	0		15	ns	
t47	RXOEn assert to data active delay	0		15	ns	

Note: Refer to Figure 7 through 9 for timing diagrams.

Figure 7 Receive System Interface Timing

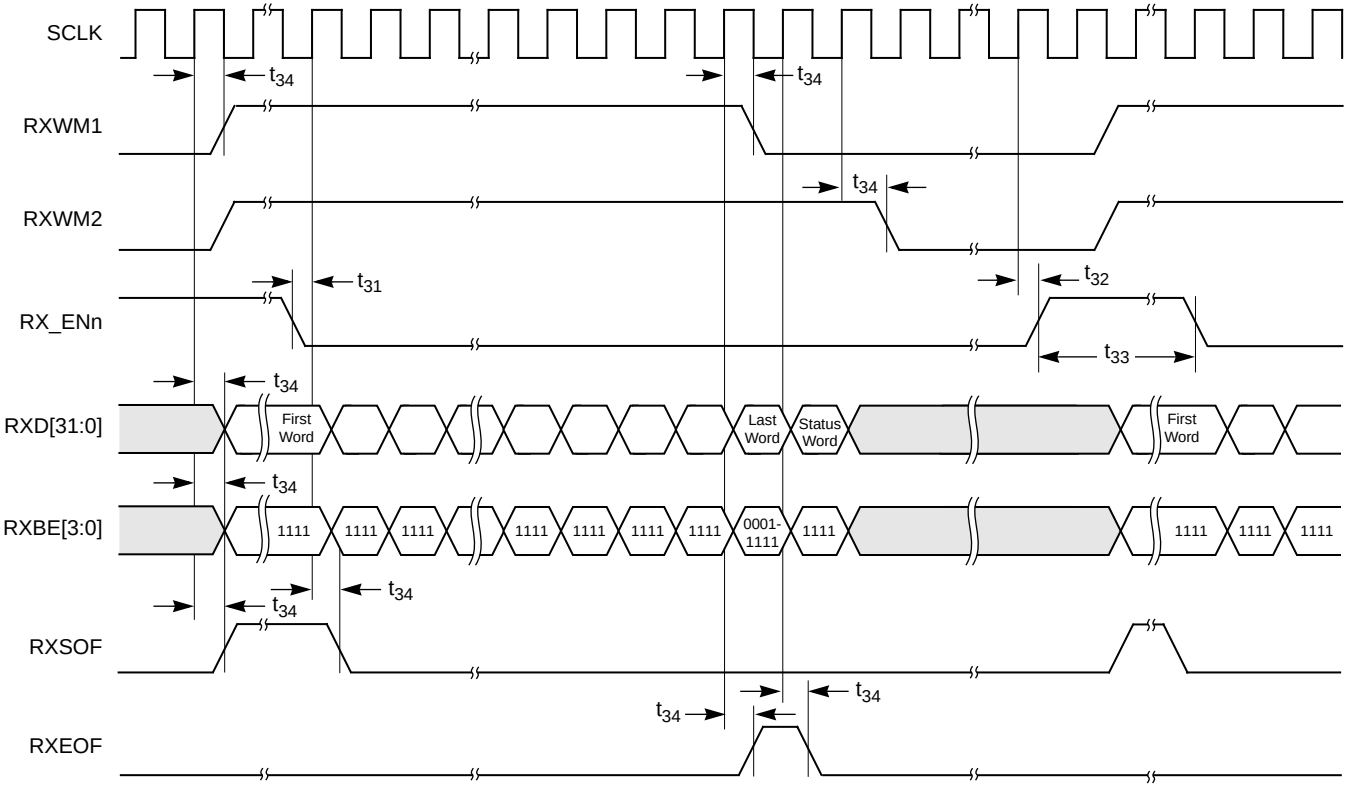


Figure 8 Receive System Interface RXABORT Timing

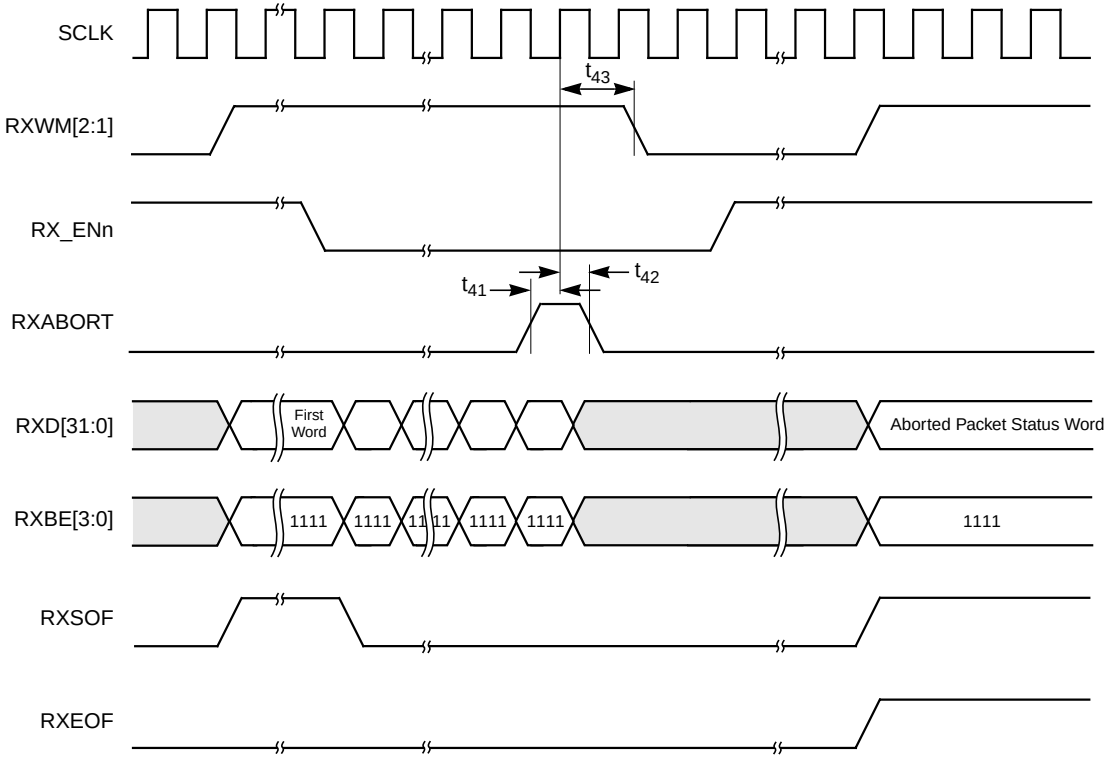


Figure 9 Receive System Interface RXOEn Timing

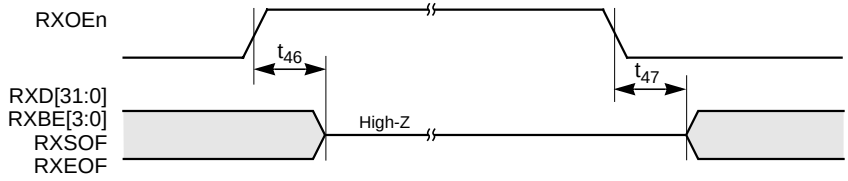


Table 7 System Interface TXDC/RXDC Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t51	TXDC/RXDC assert delay time	0		8	ns	
t52	TXDC/RXDC deassert delay time	0		2 SCLK cycles +8 ns	ns	AutoClear mode off
		0		3 SCLK cycles +8 ns	ns	AutoClear mode on
t53	CLR_TXDC/RXDC setup time	5			ns	
t54	CLR_TXDC/RXDC hold time	0			ns	
t55	TXDC/RXDC rise and fall time			4	ns	

Note: Refer to Figure 10 for timing diagram.

Figure 10 System Interface RXDC/TXDC Timing

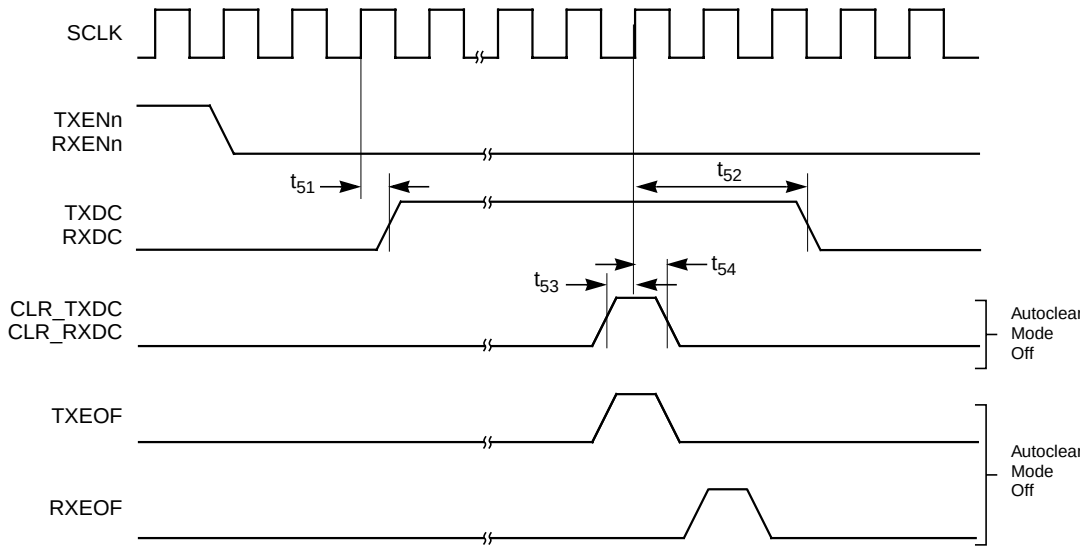


Table 8 Transmit 10-Bit PHY Interface Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t61	TBC period	7.992	8	8.008	ns	
t62	TBC HIGH time	3.2		4.8	ns	
t63	TBC LOW time	3.2		4.8	ns	
t64	TX[9:0] data valid before TBC rising edge	2.0			ns	Assumes TBC duty cycle = 40–60%
t65	TX[9:0] data valid after TBC rising edge	1.0			ns	Assumes TBC duty cycle = 40–60%
t66	TBC, TX[9:0] rise and fall time	0.7		2.4	ns	

Note: Refer to Figure 11 for timing diagram.

Figure 11 Transmit 10-Bit PHY Interface Timing

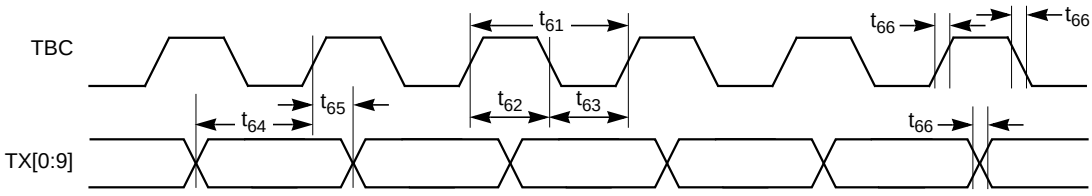


Table 9 Receive 10-Bit PHY Interface Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t71	RBC frequency	62.4937	62.5	62.5063	MHz	
t72	RBC HIGH time	6.4		9.6	ns	
		6.4		128	ns	During synchronization
t73	RBC LOW time	6.4		9.6	ns	
		6.4		128	ns	During synchronization
t74	RBC skew	7.5		8.5	ns	
t75	RX[9:0] setup time	2.5			ns	
t76	RX[9:0] hold time	1.5			ns	
t77	RBC, RX[9:0] rise and fall time	0.7		2.4	ns	

Note: Refer to Figure 12 for timing diagram.

Figure 12 Receive 10-Bit PHY Interface Timing

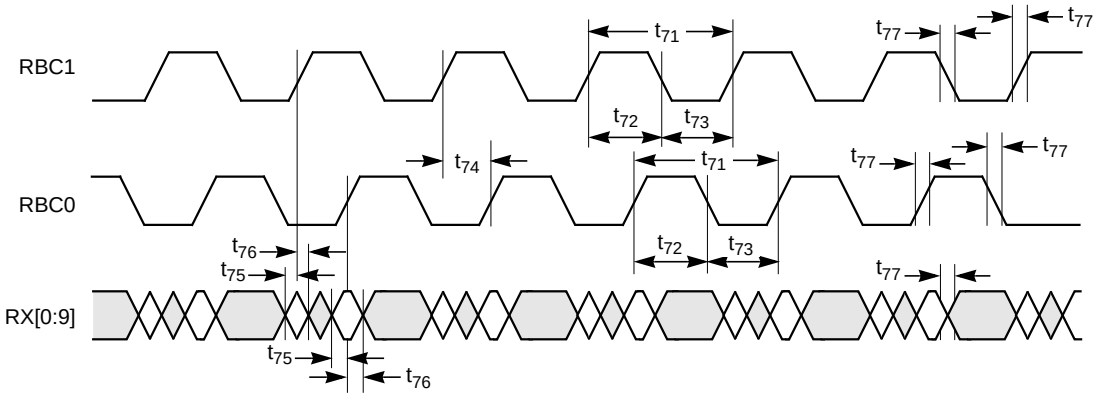


Table 10 Register Interface Timing Characteristics

Symbol	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t81	REGCSn, REGWRn, REGRDn, REGA, REGD setup time	10			ns	
t82	REGCSn, REGWRn, REGRDn, REGA, REGD hold time	1			ns	
t83	REGCLK to REGD active delay			10	ns	Read cycle. All registers except Counter Registers 1–53
				6 REGCLK cycles +10 ns	ns	Read cycle. Counter Registers 1–53, first 16 bits of counter result
				3 REGCLK cycles +10 ns	ns	Read cycle. Counter Registers 1–53, second 16 bits of counter result
t84	REGCLK to REGD 3-state delay	0		10	ns	
t85	REGCLK to REGINT assert delay	0		20	ns	
t86	REGCLK to REGINT deassert delay	0		20	ns	

Note: Refer to Figure 13 and Figure 14 for timing diagrams.

Figure 13 Register Interface Timing (Excluding Counter Read Cycle)

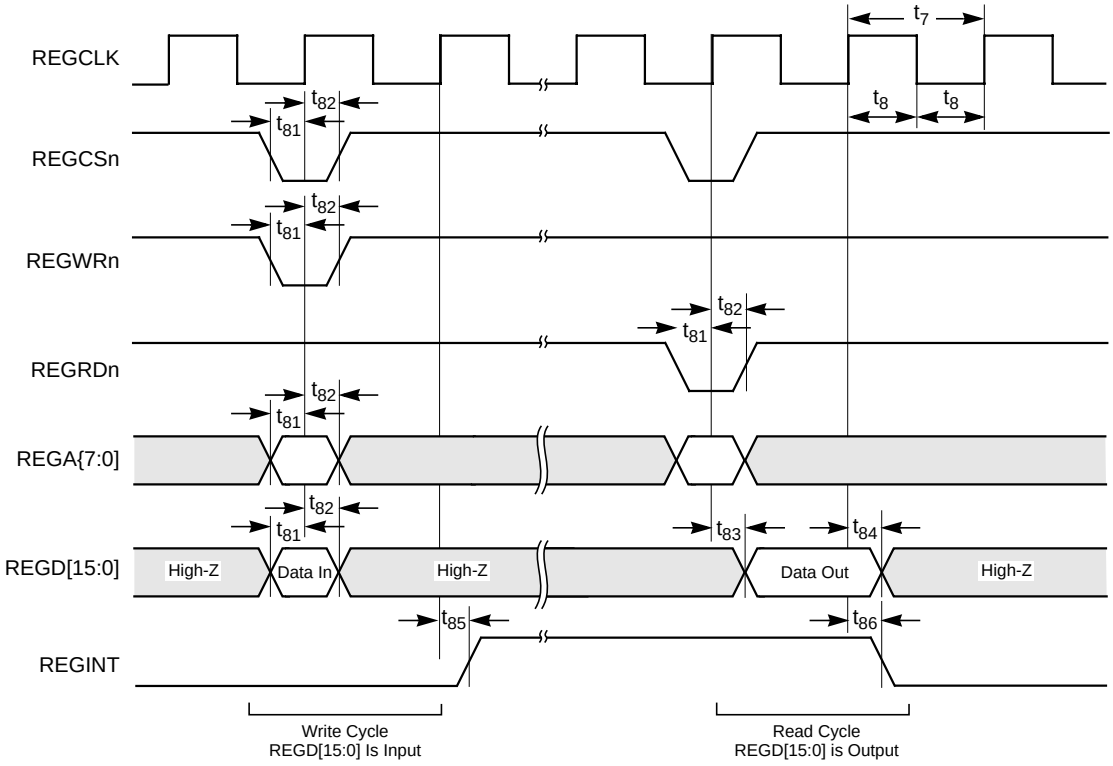
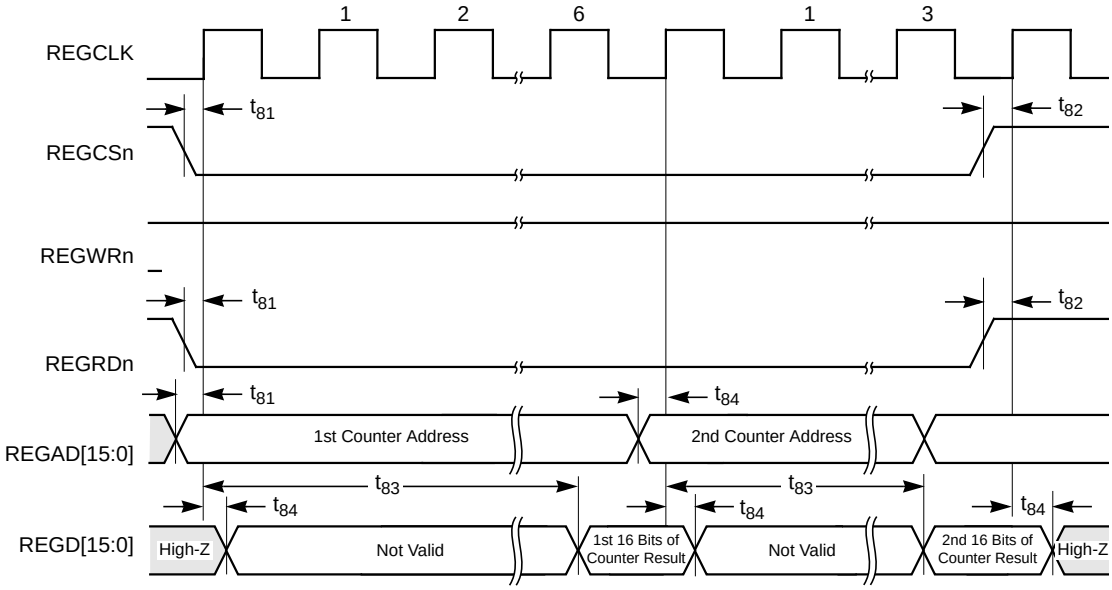


Figure 14 Register Interface Timing, Counter Read Cycle



8101/8104 Pinouts and Pin Listings

Figure 15 shows the pinout and Table 11 lists the pins for the 8101 and Figure 16 shows the pinout and Table 12 lists the pins for the 8104.

Figure 15 8101 208-Pin PQFP Pinout

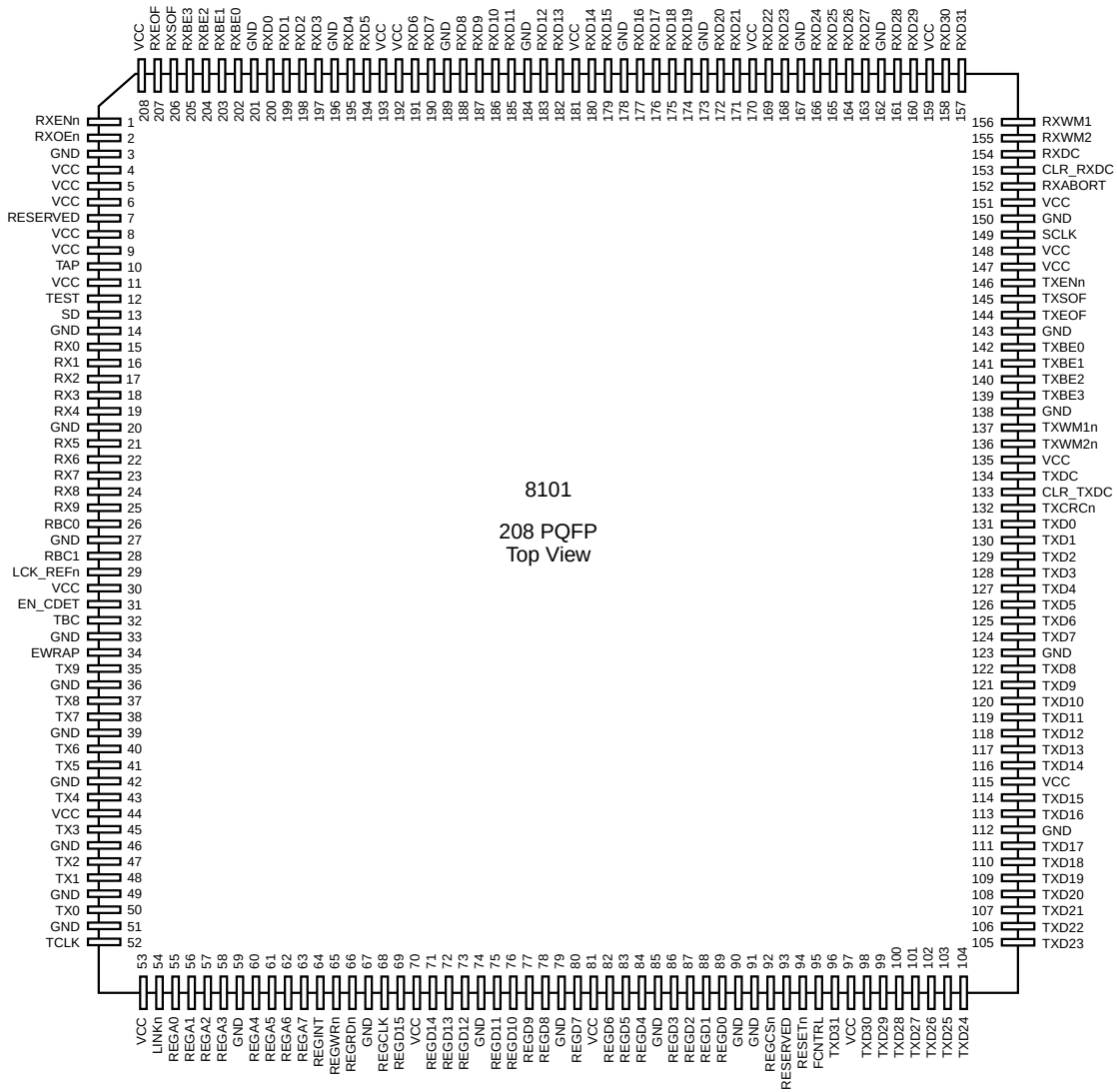


Table 11 8101 208-Pin PQFP Pin List (Alphabetical Listing)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
CLR_RXDC	153	REGA2	57	RXBE1	203	SCLK	149	TXD21	107
CLR_TXDC	133	REGA3	58	RXBE2	204	SD	13	TXD22	106
EN_CDET	31	REGA4	60	RXBE3	205	TAP	10	TXD23	105
EWRAP	34	REGA5	61	RXD0	200	TBC	32	TXD24	104
FCNTRL	95	REGA6	62	RXD1	199	TCLK	52	TXD25	103
GND	3	REGA7	63	RXD2	198	TEST	12	TXD26	102
GND	14	REGCLK	68	RXD3	197	TX0	50	TXD27	101
GND	20	REGCSn	92	RXD4	195	TX1	48	TXD28	100
GND	27	REGD0	89	RXD5	194	TX2	47	TXD29	99
GND	33	REGD1	88	RXD6	191	TX3	45	TXD30	98
GND	36	REGD2	87	RXD7	190	TX4	43	TXD31	96
GND	39	REGD3	86	RXD8	188	TX5	41	TXDC	134
GND	42	REGD4	84	RXD9	187	TX6	40	TXENn	146
GND	46	REGD5	83	RXD10	186	TX7	38	TXEOF	144
GND	49	REGD6	82	RXD11	185	TX8	37	TXSOF	145
GND	51	REGD7	80	RXD12	183	TX9	35	TXWM1n	137
GND	59	REGD8	78	RXD13	182	TXBE0	142	TXWM2n	136
GND	67	REGD9	77	RXD14	180	TXBE1	141	VCC	4
GND	74	REGD10	76	RXD15	179	TXBE2	140	VCC	5
GND	79	REGD11	75	RXD16	177	TXBE3	139	VCC	6
GND	85	REGD12	73	RXD17	176	TXCRCn	132	VCC	8
GND	90	REGD13	72	RXD18	175	TXD0	131	VCC	9
GND	91	REGD14	71	RXD19	174	TXD1	130	VCC	11
GND	112	REGD15	69	RXD20	172	TXD2	129	VCC	30
GND	123	REGINT	64	RXD21	171	TXD3	128	VCC	44
GND	138	REGRDn	66	RXD22	169	TXD4	127	VCC	53
GND	143	REGWRn	65	RXD23	168	TXD5	126	VCC	70
GND	150	RESERVED	7	RXD24	166	TXD6	125	VCC	81
GND	162	RESERVED	93	RXD25	165	TXD7	124	VCC	97
GND	167	RESETn	94	RXD26	164	TXD8	122	VCC	115
GND	173	RX0	15	RXD27	163	TXD9	121	VCC	135
GND	178	RX1	16	RXD28	161	TXD10	120	VCC	147
GND	184	RX2	17	RXD29	160	TXD11	119	VCC	148
GND	189	RX3	18	RXD30	158	TXD12	118	VCC	151
GND	196	RX4	19	RXD31	157	TXD13	117	VCC	159
GND	201	RX5	21	RXDC	154	TXD14	116	VCC	170
LCK_REFn	29	RX6	22	RXENn	1	TXD15	114	VCC	181
LINKn	54	RX7	23	RXEOF	207	TXD16	113	VCC	193
RBC0	26	RX8	24	RXOEn	2	TXD17	111	VCC	192
RBC1	28	RX9	25	RXSOF	206	TXD18	110	VCC	208
REGA0	55	RXABORT	152	RXWM1	156	TXD19	109		
REGA1	56	RXBE0	202	RXWM2	155	TXD20	108		

Figure 16 8104 208-Pin BGA Pinout

A1 VCC	A2 RXEOF	A3 RXBE3	A4 RXD0	A5 RXD4	A6 VCC	A7 RXD7	A8 RXD11	A9 RXD16	A10 RXD20	A11 RXD21	A12 RXD23	A13 RXD27	A14 RXD29	A15 RXD30	A16 RXD31
B1 RXOEn	B2 RXENn	B3 RXSOF	B4 RXBE2	B5 RXD2	B6 VCC	B7 RXD8	B8 RXD10	B9 RXD15	B10 RXD19	B11 VCC	B12 RXD25	B13 RXD28	B14 VCC	B15 RXWM1	B16 RXWM2
C1 GND	C2 VCC	C3 VCC	C4 RXBE1	C5 RXD3	C6 VCC	C7 RXD6	C8 RXD12	C9 RXD14	C10 RXD18	C11 RXD22	C12 RXD26	C13 GND	C14 RXABORT	C15 CLR_RXDC	C16 TXDC
D1 VCC	D2 VCC	D3 RESERVED	D4 RXBE0	D5 RXD1	D6 RXD5	D7 RXD9	D8 RXD13	D9 VCC	D10 RXD17	D11 VCC	D12 RXD24	D13 VCC	D14 VCC	D15 SLCK	D16 VCC
E1 VCC	E2 TAP	E3 VCC	E4 TEST									E13 GND	E14 TXEOF	E15 TXSOF	E16 TXENn
F1 SD	F2 RX0	F3 RX1	F4 RX2									F13 TXBE3	F14 TXBE2	F15 TXBE0	F16 TXBE1
G1 RX4	G2 RX3	G3 RX5	G4 RX6			G7 GND	G8 GND	G9 GND	G10 GND			G13 TXDC	G14 VCC	G15 TXWM2n	G16 TXWM1n
H1 RX8	H2 RX7	H3 RX9	H4 RBC0			H7 GND	H8 GND	H9 GND	H10 GND			H13 TXD1	H14 TXD0	H15 TXCRCn	H16 CLR_TXDC
J1 RBC1	J2 LCK_REFn	J3 VCC	J4 VCC			J7 GND	J8 GND	J9 GND	J10 GND			J13 TXD2	J14 TXD3	J15 TXD5	J16 TXD4
K1 TBC	K2 EN_CDET	K3 EWRAP	K4 TX9			K7 GND	K8 GND	K9 GND	K10 GND			K13 TXD6	K14 TXD7	K15 GND	K16 TXD8
L1 TX7	L2 TX8	L3 GND	L4 TX6									L13 TXD9	L14 TXD10	L15 TXD11	L16 TXD12
M1 GND	M2 TX5	M3 TX4	M4 VCC									M13 TXD13	M14 TXD14	M15 TXD15	M16 VCC
N1 TX3	N2 TX2	N3 GND	N4 GND	N5 REGWRn	N6 REGD15	N7 REGD12	N8 REGD8	N9 REGD7	N10 REGD5	N11 REGD1	N12 RESERVED	N13 VCC	N14 TXD17	N15 TXD18	N16 TXD16
P1 TX1	P2 TCLK	P3 REGA3	P4 REGA5	P5 REGINT	P6 REGCLK	P7 REGD13	P8 REGD9	P9 REGD6	P10 REGD4	P11 REGD0	P12 RESETn	P13 TXD30	P14 TXD19	P15 TXD22	P16 TXD20
R1 TX0	R2 VCC	R3 REGA2	R4 REGA4	R5 REGA6	R6 REGRDn	R7 VCC	R8 REGD11	R9 VCC	R10 REGD2	R11 GND	R12 TXD31	R13 TXD28	R14 TXD27	R15 TXD23	R16 TXD21
T1 LINKn	T2 REGA0	T3 REGA1	T4 GND	T5 REGA7	T6 GND	T7 REGD14	T8 REGD10	T9 VCC	T10 REGD3	T11 REGCSn	T12 FCNTRL	T13 TXD29	T14 TXD26	T15 TXD25	T16 TXD24

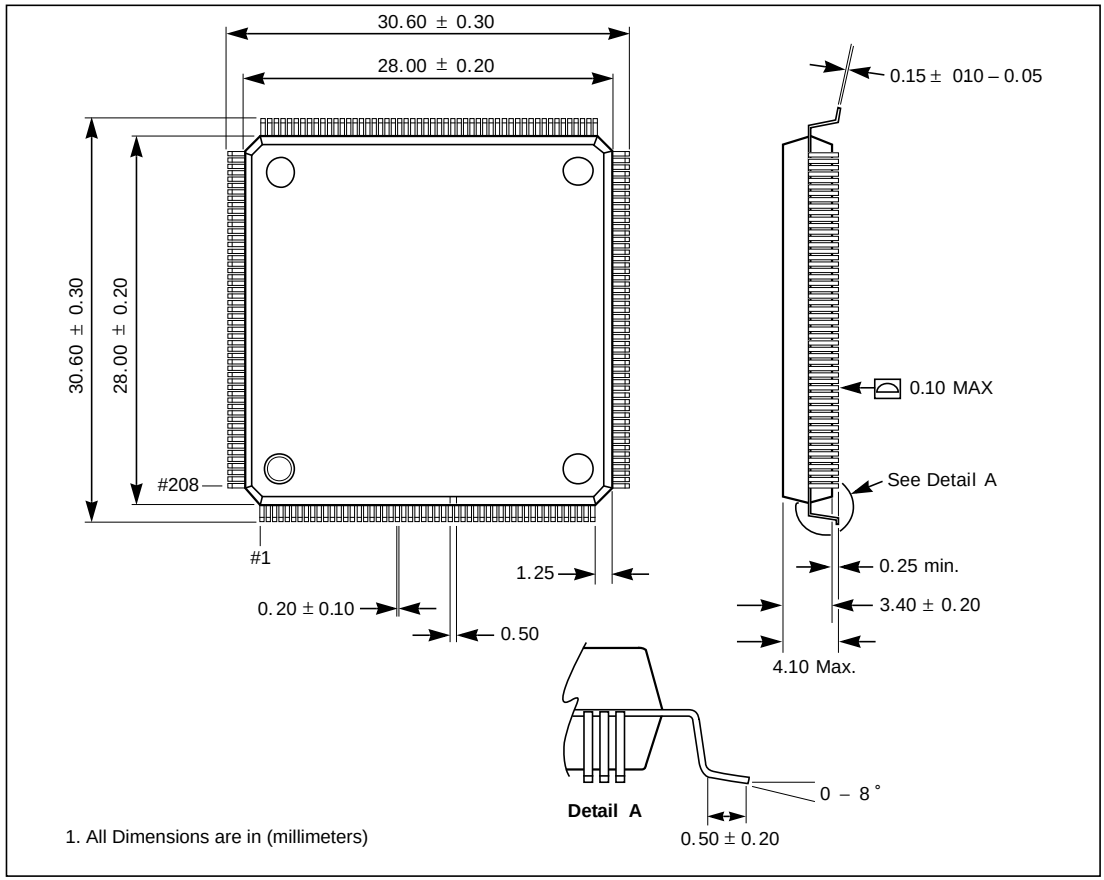
Table 12 8104 208-Pin BGA Pin List (Alphabetical Listing)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
CLR_RXDC	C15	REGA4	R04	RXBE3	A03	TBC	K01	TXD24	T16
CLR_TXDC	H16	REGA5	P04	RXD0	A04	TCLK	P02	TXD25	T15
COM_DET	F01	REGA6	R05	RXD1	D05	TEST	E04	TXD26	T14
EN_CDET	K02	REGA7	T05	RXD2	B05	TX0	R01	TXD27	R14
EWRAP	K03	REGCLK	P06	RXD3	C05	TX1	P01	TXD28	R13
FCNTRL	T12	REGCSn	T11	RXD4	A05	TX2	N02	TXD29	T13
GND	A07	REGD0	P11	RXD5	D06	TX3	N01	TXD30	P13
GND	C01	REGD1	N11	RXD6	C07	TX4	M03	TXD31	R12
GND	C13	REGD2	R10	RXD7	A07	TX5	M02	TXDC	G13
GND	E13	REGD3	T10	RXD8	B07	TX6	L04	TXENn	E16
GND	G07	REGD4	P10	RXD9	D07	TX7	L01	TXEOF	E14
GND	G08	REGD5	N10	RXD10	B08	TX8	L02	TXSOF	E15
GND	G09	REGD6	P09	RXD11	A08	TX9	K04	TXWM1n	G16
GND	G10	REGD7	N09	RXD12	C08	TXBE0	F15	TXWM2n	G15
GND	H07	REGD8	N08	RXD13	D08	TXBE1	F16	VCC	A01
GND	H08	REGD9	P08	RXD14	C09	TXBE2	F14	VCC	A06
GND	H09	REGD10	T08	RXD15	B09	TXBE3	F13	VCC	B06
GND	H10	REGD11	R08	RXD16	A09	TXCRCn	H15	VCC	B11
GND	J07	REGD12	N07	RXD17	D10	TXD0	H14	VCC	B14
GND	J08	REGD13	P07	RXD18	C10	TXD1	H13	VCC	C02
GND	J09	REGD14	T07	RXD19	B10	TXD2	J13	VCC	C03
GND	J10	REGD15	N06	RXD20	A10	TXD3	J14	VCC	D01
GND	K07	REGINT	P05	RXD21	A11	TXD4	J16	VCC	D02
GND	K08	REGRDn	R06	RXD22	C11	TXD5	J15	VCC	D09
GND	K09	REGWRn	N05	RXD23	A12	TXD6	K13	VCC	D11
GND	K10	RESERVED	D03	RXD24	D12	TXD7	K14	VCC	D13
GND	K15	RESERVED	N12	RXD25	B12	TXD8	K16	VCC	D14
GND	L03	RESETn	P12	RXD26	C12	TXD9	L13	VCC	D16
GND	M01	RX0	F02	RXD27	A13	TXD10	L14	VCC	E01
GND	N03	RX1	F03	RXD28	B13	TXD11	L15	VCC	E03
GND	N04	RX2	F04	RXD29	A14	TXD12	L16	VCC	G14
GND	R11	RX3	G02	RXD30	A15	TXD13	M13	VCC	J03
GND	T04	RX4	G01	RXD31	A16	TXD14	M14	VCC	J04
GND	T06	RX5	G03	RXDC	C16	TXD15	M15	VCC	M04
LCK_REFn	J02	RX6	G04	RXENn	B02	TXD16	N16	VCC	M16
LINKn	T01	RX7	H02	RXEOF	A02	TXD17	N14	VCC	N13
RBC0	H04	RX8	H01	RXOEn	B01	TXD18	N15	VCC	R02
RBC1	J01	RX9	H03	RXSOF	B03	TXD19	P14	VCC	R07
REGA0	T02	RXABORT	C14	RXWM1	B15	TXD20	P16	VCC	R09
REGA1	T03	RXBE0	D04	RXWM2	B16	TXD21	R16	VCC	T09
REGA2	R03	RXBE1	C04	SCLK	D15	TXD22	P15		
REGA3	P03	RXBE2	B04	TAP	E02	TXD23	R15		

Package Mechanical Dimensions

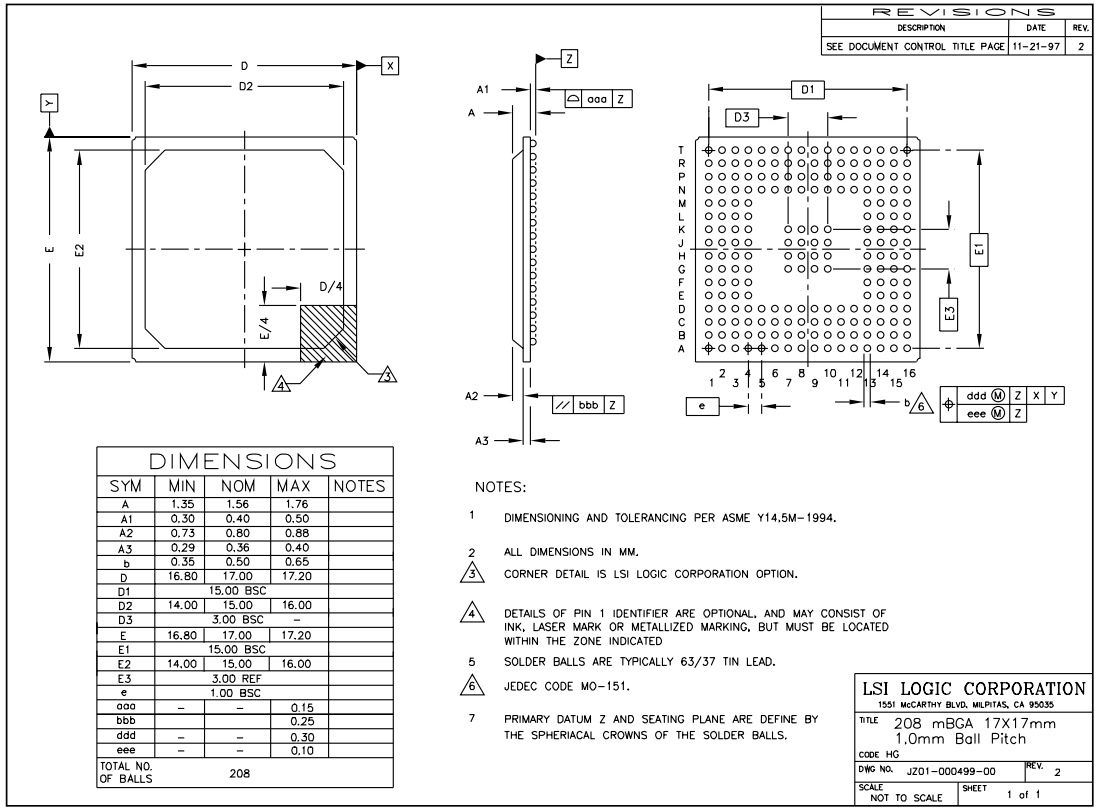
The 8101 Gigabit Ethernet Controller is available in the 208-pin Plastic Quad Flat Pack (PQFP) as shown in Figure 17. and the 8104 Ball Grid Array Package as shown in Figure 6.14

Figure 17 208-Pin PQFP Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing.**

Figure 18 208-Pin BGA Mechanical Drawing



DIMENSIONS				
SYM	MIN	NOM	MAX	NOTES
A	1.35	1.56	1.76	
A1	0.30	0.40	0.50	
A2	0.73	0.80	0.88	
A3	0.29	0.36	0.40	
b	0.35	0.50	0.65	
D	16.80	17.00	17.20	
D1	15.00 BSC			
D2	14.00	15.00	16.00	
D3	3.00 BSC		–	
E	16.80	17.00	17.20	
E1	15.00 BSC			
E2	14.00	15.00	16.00	
E3	3.00 REF			
e	1.00 BSC			
aaa	–	–	0.15	
bbb			0.25	
ddd	–	–	0.30	
eee	–	–	0.10	
TOTAL NO. OF BALLS	208			

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code HG.**

Notes

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