Wideband Quad Digital Down-converter/Up-converter

FEATURES

- **Four Independently Configurable Wideband Down-converter or Up-converter Channels**
- **Down-conversion Channel Mode**
  - **Input Clock Rates to 150-MSPS for 4 Channels, 300-MSPS for 2 Channels**
  - **Four Wideband Down-conversion Channels Support UMTS Standards**
  - **115 dB SFDR**
  - **FIR Filter Block Consists of 16 Cells that Provide up to 256 Taps per Channel**
  - **64 Parallel Input Bits and 64 Parallel Output Bits Provide Flexible I/O Options**
  - **Many multiplex output options**
- **Up-conversion Channel Mode**
  - **Output Rates to 150-MSPS for 4 Channels, 300-MSPS for 2 Channels**
  - **Four Up-conversion Channels Support UMTS Standards**
  - **FIR Filter Block Consists of 16 Cells that Provide up to 256 Taps per Channel**
  - **64 Parallel Input Bits and 64 Parallel Output Bits Provide Flexible I/O Options**
  - **Multiple real and complex output options**
  - **Two channel double rate real output mode with rates to 300 MSPS**
  - **Outputs can be Independent, Summed into Two or One Output(s), and optionally Merged with Multiple GC5016 Chips**
- **JTAG Boundary Scan**
- **3.3-V I/O, 1.8-V Core**
- **Power Dissipation: <1-Watt for 4 Channels**
- **Package: 252-Ball, 17-mm PBGA, 1-mm Pitch**

APPLICATIONS

- **Cellular Base Transceiver Station Transmit and Receive Channels**
  - **WCDMA**
  - **CDMA2000**

DESCRIPTION

The GC5016 is a flexible wideband 4-channel digital up-converter and down-converter. The GC5016 is designed for high-speed, high bandwidth digital signal processing applications like 3G cellular base transceiver station transmit and receive channels. The GC5016 is also applicable for general-purpose digital filtering applications. The four identical processing channels can be independently configured for upconversion, downconversion or a combination of two upconversion and two downconversion channels.

In up-conversion mode, the channel accepts real or complex signals, interpolates them by programmable amounts ranging from 1 to 4096, and modulates them up to selected center frequencies. The modulated signals are then summed together with other channels and optionally summed with modulated signals from other GC5016 chips. Channels can be used in pairs to increase the output sample rate or to increase the input bandwidth, or both. Each channel contains a user programmable input filter (PFIR), which can be used to shape the transmitted signal's spectrum, or can be used as a Nyquist transmit filter for shaping digital data such as QPSK, GMSK or QAM symbols.

In down-conversion mode, the channel accepts real or complex signals, demodulates them from selected carrier frequencies, decimates them by programmable amounts ranging from 1 to 4096, applies a gain from a user defined automatic gain control, and produces 20-bit outputs. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the interpolation and filtering of each circuit. Channels can be synchronized to support beamforming or frequency hopped systems. The output from the down-conversion channel is formatted and output in up to four output ports as either real or complex data.

FUNCTIONAL BLOCK DIAGRAM

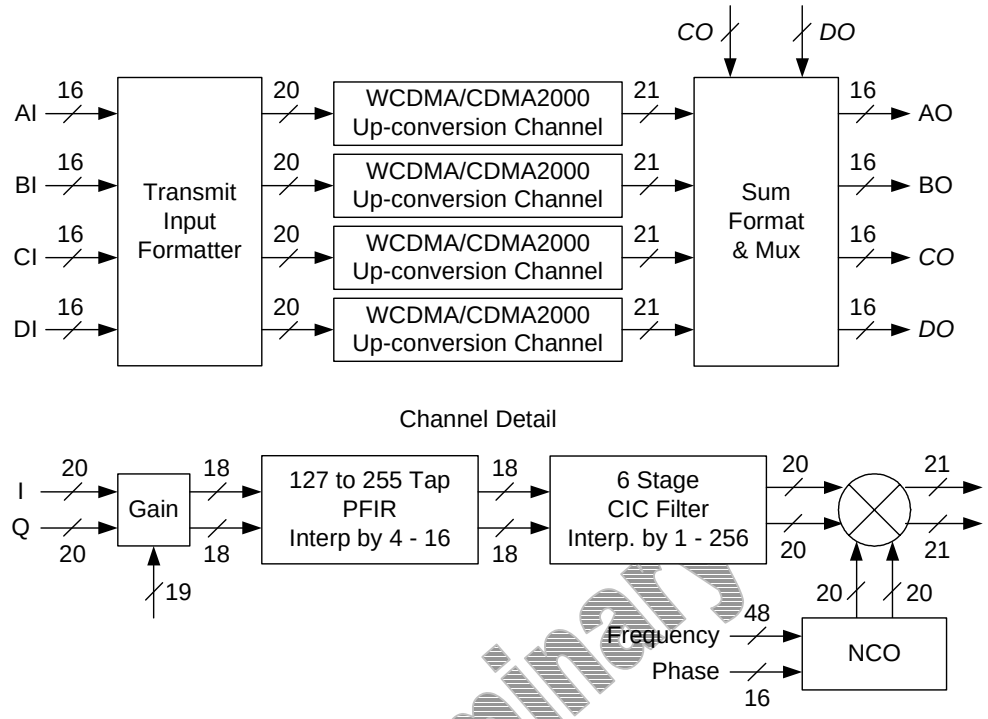

Figure 1. GC5016 in Digital Up-conversion Mode.

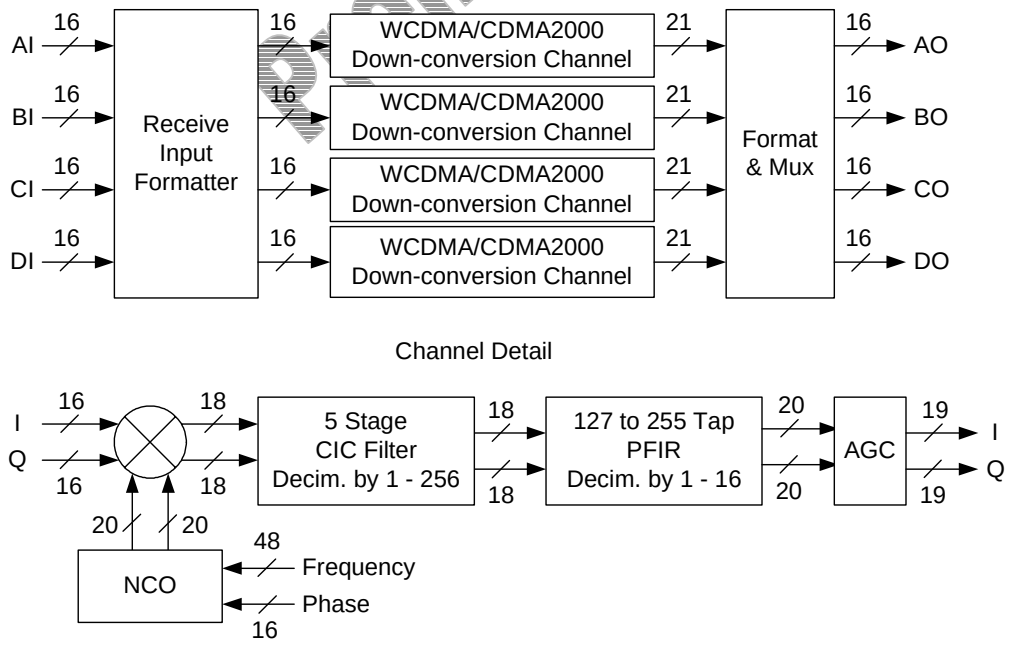

Figure 2. GC5016 in Digital Down-conversion Mode.

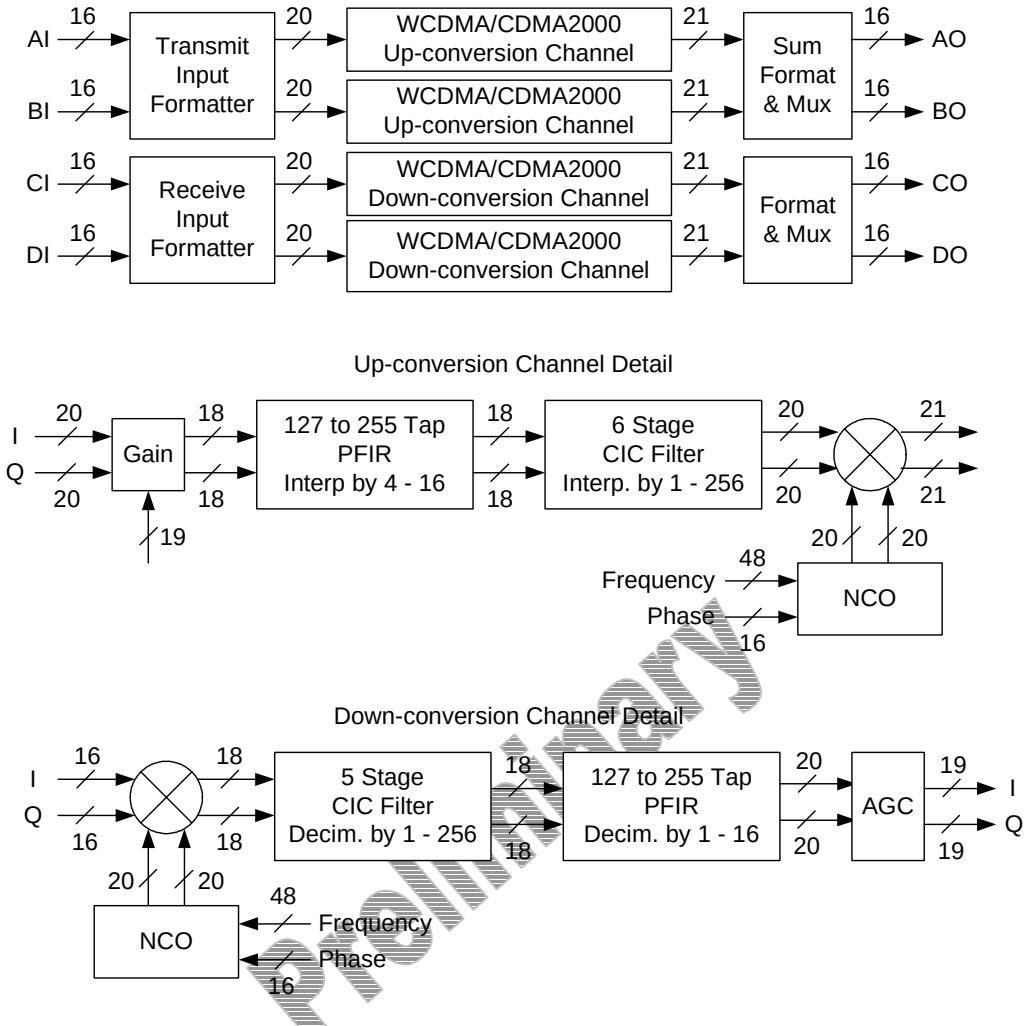

Figure 3. GC5016 in Transceiver Mode.

- **Package: 252-Ball, 17-mm PBGA, 1-mm Pitch**

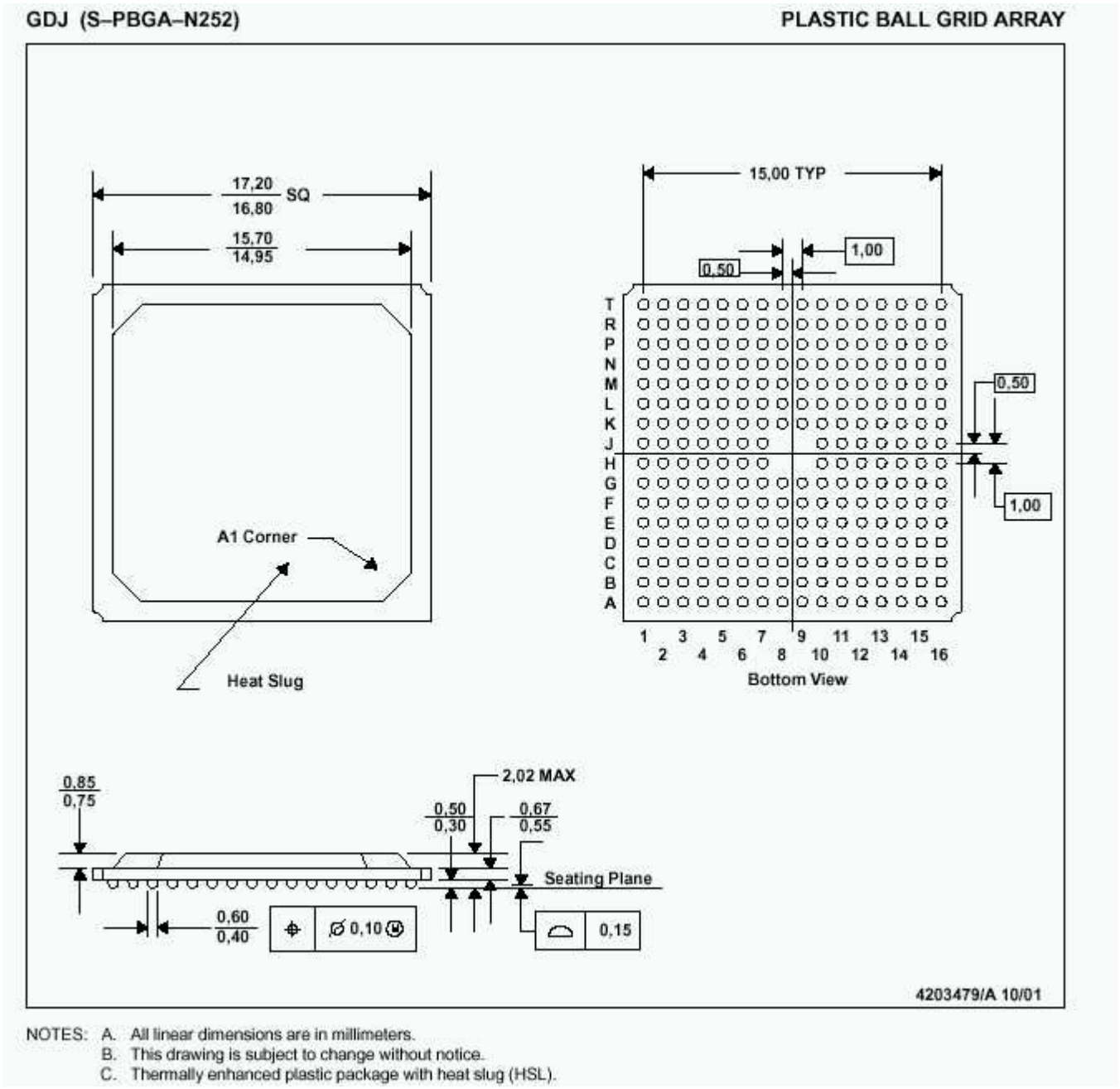

Figure 4. PBGA PACKAGE.

Pinout locations

Table 1. Pinout Locations

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	BCK	BO14	BO13	AO11	AO10	BO8	GND	GND	AO6	BO4	BO3	AO1	IFLG	TMS	GND
B	AI1	BI0	AO15	AO14	BO11	BO10	AO9	VPAD	VPAD	BO5	AO4	BO2	BO0	TDI	trstB	rstB
C	BI3	BI2	AI0	AFS	BO15	AO12	BO9	AO7	BO6	AO5	AO3	BO1	soB	GND	sibB	CI15
D	AI5	AI3	AI2	BFS	ACK	AO13	BO12	BO7	AO8	AO2	AO0	TDO	TCK	DI15	DI14	CI13
E	BI6	AI6	BI5	BI1	GND	VPAD	VPAD	VPAD	VPAD	VPAD	VPAD	GND	SIAB	DI13	DI12	DI11
F	AI8	BI7	AI7	BI4	VCOR	GND	GND	VPAD	VPAD	GND	GND	VCOR	CI14	CI12	CI11	DI10
G	BI9	AI9	BI8	AI4	VCOR	GND	GND	GND	GND	GND	GND	VCOR	CI10	CI9	DI8	CI8
H	GND	AI10	BI11	BI10	VCOR	VCOR	GND	/	/	GND	VCOR	VCOR	DI9	VPAD	DI7	GND
J	GND	BI12	AI12	AI11	VCOR	VCOR	GND	/	/	GND	VCOR	VCOR	DI5	CI7	DI6	GND
K	AI13	BI13	AI14	BI14	VCOR	GND	GND	GND	GND	GND	GND	VCOR	CI5	DI4	CI4	CI6
L	AI15	BI15	CK	A0	VCOR	GND	GND	VPAD	VPAD	GND	GND	VCOR	CCK	DI2	CI3	DI3
M	A1	A2	A3	A4	GND	VPAD	VPAD	VPAD	VPAD	VPAD	VPAD	GND	DFS	CI1	DI1	CI2
N	ceB	rdB	WRMODE	C0	C3	C9	C10	DO1	CO2	CO7	CO12	DO13	CO15	DCK	CI0	DI0
P	wrB	C1	GND	C5	C8	C14	DO2	CO4	DO4	CO6	DO8	CO11	CO13	GND	DO15	CFS
R	C2	C4	C6	C12	C13	DO0	CO3	VPAD	VPAD	DO5	DO7	CO9	DO10	DO12	CO14	DO14
T	GND	C7	C11	C15	CO0	CO1	DO3	GND	GND	CO5	DO6	CO8	DO9	CO10	DO11	GND

/ - No Ball

PIN FUNCTIONS

On all buses the bit 0 is the least significant bit. All outputs are tristatable. Jtag related inputs have pullups – if an external pulldown is used it must be less than 500 Ohms. Whenever I and Q are multiplexed I comes first. All clocked inputs are registered on the rising edge of CK, and all clocked outputs are released on the rising edge of CK except for Jtag output (TDO).

SIGNAL	TYPE	DESCRIPTION
		CONTROL I/O
A[4..0]	I	Control Address Bus – Active high inputs These pins are used to address the control registers within the chip. Each of the control registers within the chip are assigned a unique address. A control register can be written to or read from by having the page register set to the appropriate page and then setting A[4..0] to the register's address.
C[15..0]	I/O	Control Data I/O Bus – Active high bidirectional I/O pins This is the 16-bit control data I/O bus. Control registers are written to or read from through these pins. The chip drives these pins when ceB is low, rdB is low and wrB is high.
ceB	I	Chip Enable – Active low input pin This control strobe enables the read or write operations.
wrB	I	Write Enable – Active low input pin The value on the C[15..0] pins is written into the register selected by the A[4..0] and page register when wrB and ceB are low.
rdB	I	Read Enable – Active low input pin The register selected by A[4..0] and the page register is output on the C[15..0] pins when rdB and ceB are low.
		DATA I/O
AI[15..0]	I	Clocked input port A, data bits 0 through 15 Can be configured for many possible input formats.
BI[15..0]	I	Clocked input port B, data bits 0 through 15 Can be configured for many possible input formats.
CI[15..0]	I	Clocked input port C, data bits 0 through 15 Can be configured for many possible input formats.
DI[15..0]	I	Clocked input port D, data bits 0 through 15 Can be configured for many possible input formats.
AO[15..0]	O	Clocked output port A, data bits 0 through 15 Can be configured for many possible output formats.
BO[15..0]	O	Clocked output port B, data bits 0 through 15 Can be configured for many possible output formats.
CO[15..0]	I/O	Dual function: Clocked output - port C, data bits 0 through 15 Can be configured for many possible output formats. Clocked input – Sum IO input data, data bits 0 through 15 Can be configured for many possible input formats.
DO[15..0]	I/O	Dual function: Clocked output - port D, data bits 0 through 15 Can be configured for many possible output formats.

		Clocked input – Sum IO input data, data bits 0 through 15 Can be configured for many possible input formats.
[A..D]CK	O	Clocked output for ports [A..D] The clock for input ports in up-conversion mode, and output ports in down-conversion mode. When configured as a transceiver channels A and B are in upconversion and channels C and D are in downconversion mode.
[A..D]FS	O	Clocked output frame stobes for channels A..D – Used to signify the beginning of a data frame for each input port in up-conversion mode, and output in down-conversion mode. The frame strobes are set high by the GC5016 with the first word in a frame. The frame strobes can be programmed to be sent early.
GND		Ground.
CK	I	Main Input Clock. The clock input to the chip.
IFLG	O	Clocked output A flag used to indicate which samples are real or imaginary in upconversion mode when I and Q are time multiplexed.
NC		No Connect.
VCOR		Core Supply Voltage. Used to supply the core logic, nominally set to 1.8V.
VPAD		Interface Voltage. Used to set the I/O levels for all pins, nominally set at 3.3V.
WRMODE		A static control input that changes the timing of control writes. Normally tied low. When low control write data must be stable for a setup time ahead and hold time after the end of the write strobe. When high data must be stable for a setup time ahead of the write strobe going active until a hold time after it goes inactive.
rstB		Chip reset bar. Active low signal. Not clocked.
siaB	I	Sync input A bar. Active low data input signal.
sibB	I	Sync input B bar. Active low data input signal.
soB	O	Sync output bar. Active low data output signal.
TCK	I	JTAG Clock – Active high input. Internal pullup.
TDI	I	JTAG data in – Active high input clocked on TCK rising. Internal pullup.
TDO	O	JTAG data out – Tristate output clocked on falling edge of TCK.
TMS	I	JTAG Interface – – Active high input clocked on TCK rising. Internal pullup.
TRSB	I	Asynchronous JTAG reset bar. Internal pullup.

DETAILED DESCRIPTION

The GC5016 is a flexible wideband 4-channel digital up-converter and down-converter. The GC5016 is designed for high-speed, high bandwidth digital signal processing applications like 3G cellular base transceiver station transmit and receive channels. The GC5016 is also applicable for general-purpose digital filtering applications. The four processing channels can be independently configured upconversion, downconversion, or a combination of two upconversion and two downconversion channels. The GC5016 processing channels can also be used in pairs to increase the input sample rate, bandwidth or both.

The GC5016 is organized into four channels A, B, C, & D. The channels are organized in pairs (AB and CD). Each pair can do one of:

- Two channel digital upconversion to main input clock (CK) rate
- One channel digital upconversion to twice CK rate
- Two channel digital downconversion from CK rate
- One channel digital downconversion from twice CK rate.

If the chip is configured to do both up and down conversion channels AB are assumed to be in up conversion and CD in down conversion.

The chip is very flexible which can make it daunting to manually program. A software program is available to configure the chip based on signal processing oriented user input.

A general purpose synchronization mechanism is used to allow flexibility in synchronization allowing the user to select which functions are synchronized to each of two hardware sync inputs, a s/w one shot, or a periodic counter. The synchronization mechanism is described in more detail in a later section.

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