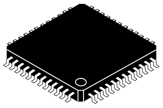


18-BIT, 500-kHz, UNIPOLAR INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- **500-kHz Sample Rate**
- **18-Bit NMC Ensured Over Temperature**
- **Zero Latency**
- **Low Power: 110 mW at 500 kHz**
- **Unipolar Input Range**
- **Onboard Reference Buffer**
- **High-Speed Parallel Interface**
- **Wide Digital Supply**
- **8-/16-/18-Bit Bus Transfer**
- **48-Pin TQFP Package**

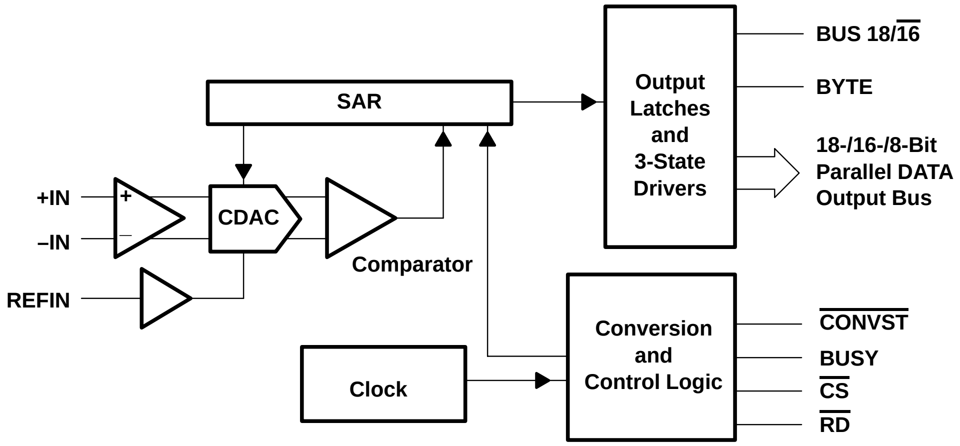
APPLICATIONS

- **Medical Instruments**
- **Optical Networking**
- **Transducer Interface**
- **High Accuracy Data Acquisition Systems**
- **Magnetometers**

DESCRIPTION

The ADS8383 is an 18-bit, 500 kHz A/D converter. The device includes a 18-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8383 offers a full 18-bit interface, a 16-bit option where data is read using two read cycles or even an 8-bit bus using three read cycles if necessary.

The ADS8383 is available in a 48-lead TQFP package and is characterized over the industrial –40°C to 85°C temperature range.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8383I	±10	–2~7	17	48 Pin TQFP	PFB	–40°C to 85°C	ADS8383IPFBT	Tape and reel 250
							ADS8383IPFBR	Tape and reel 1000
ADS8383IB	±7	–1~2.5	18	48 Pin TQFP	PFB	–40°C to 85°C	ADS8383IBPFBT	Tape and reel 250
							ADS8383IBPFBR	Tape and reel 1000

NOTE: For the most current specifications and package information, refer to our website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†

Voltage, +IN to AGND	+VA + 0.1 V
Voltage, –IN to AGND	0.5 V
Voltage range, +VA to AGND	–0.3 V to 7 V
Voltage range, +VBD to BDGND	–0.3 V to 7 V
Voltage range, +VA to +VBD	–0.3 V to 2.5 V
Digital input voltage to BDGND	–0.3 V to +VBD + 0.3 V
Digital output voltage to BDGND	–0.3 V to +VBD + 0.3 V
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Junction temperature (T_J max)	150°C
TQFP package: Power dissipation	$(T_J\text{Max} – T_A)/\theta_{JA}$
θ_{JA} thermal impedance	86°C/W
Lead temperature, soldering: Vapor phase (60 sec)	215°C
Infrared (15 sec)	220°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = –40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
Full-scale input voltage (see Note 1)		+IN – –IN	0		V_{ref}	V
Absolute input voltage		+IN	–0.2		V_{ref} + 0.2	V
		–IN	–0.2		0.2	
Input capacitance				45		pF
Input leakage current				1		nA
System Performance						
Resolution				18		Bits
No missing codes	ADS8383I	(+IN – –IN) < 0.5 FS	18			Bits
		(+IN – –IN) ≥ 0.5 FS	17			
	ADS8383IB		18			
Integral linearity (see Notes 2 and 3)	ADS8383I	(+IN – –IN) < 0.125 FS	–4		4	LSB (18 bit)
		(+IN – –IN) < 0.5 FS	–6		6	
		(+IN – –IN) ≥ 0.5 FS	–10		10	
	ADS8383IB		–7	–2/3	7	
Differential linearity	ADS8383I	(+IN – –IN) < 0.125 FS	–1		2	LSB (18 bit)
		(+IN – –IN) < 0.5 FS	–1		3	
		(+IN – –IN) ≥ 0.5 FS	–2		7	
	ADS8383IB		–1	–1/1.4	2.5	
Offset error (see Note 4)	ADS8383I		–1	±0.5	1	mV
	ADS8383IB		–0.75	±0.25	0.75	
Gain error (see Note 4)	ADS8383I	V_{ref} = 4.096 V	–0.1		0.1	%FS
	ADS8383IB	V_{ref} = 4.096 V	–0.06		0.06	%FS
Noise				60		µV RMS
Power supply rejection ratio		At 3FFFFh output code		75		dB
Sampling Dynamics						
Conversion time					1.5	µs
Acquisition time			0.4			µs
Throughput rate					500	kHz
Aperture delay				4		ns
Aperture jitter				15		ps
Step response				150		ns
Over voltage recovery				150		ns

NOTES:
1. Ideal input span, does not include gain or offset error.
2. LSB means least significant bit
3. This is endpoint INL, not best fit.
4. Measured relative to an ideal full-scale input (+IN – –IN) of 4.096 V

SPECIFICATIONS (CONTINUED)

T_A = –40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics						
Total harmonic distortion (THD) (see Note 1)	ADS8383I	V_{IN} = 4 V_{pp} at 1 kHz		–110		dB
	ADS8383IB			–112		
	ADS8383I	V_{IN} = 4 V_{pp} at 10 kHz		–98		
	ADS8383IB			–108		
	ADS8383I	V_{IN} = 4 V_{pp} at 50 kHz		–98		
	ADS8383IB			–99		
	ADS8383I	V_{IN} = 4 V_{pp} at 100 kHz		–90		
	ADS8383IB			–91		
Signal to noise ratio (SNR) (see Note 1)	ADS8383I	V_{IN} = 4 V_{pp} at 1 kHz		87		dB
	ADS8383IB			88		
	ADS8383I	V_{IN} = 4 V_{pp} at 10 kHz		87		
	ADS8383IB			87		
	ADS8383I	V_{IN} = 4 V_{pp} at 50 kHz		87		
	ADS8383IB			87		
	ADS8383I	V_{IN} = 4 V_{pp} at 100 kHz		87		
	ADS8383IB			87		
Signal to noise + distortion (SINAD) (see Note 1)	ADS8383I	V_{IN} = 4 V_{pp} at 1 kHz		86		dB
	ADS8383IB			87		
	ADS8383I	V_{IN} = 4 V_{pp} at 10 kHz		86		
	ADS8383IB			86		
	ADS8383I	V_{IN} = 4 V_{pp} at 50 kHz		86		
	ADS8383IB			86		
	ADS8383I	V_{IN} = 4 V_{pp} at 100 kHz		85		
	ADS8383IB			85		
Spurious free dynamic range (SFDR) (see Note 1)	ADS8383I	V_{IN} = 4 V_{pp} at 1 kHz		110		dB
	ADS8383IB			112		
	ADS8383I	V_{IN} = 4 V_{pp} at 10 kHz		98		
	ADS8383IB			107		
	ADS8383I	V_{IN} = 4 V_{pp} at 50 kHz		98		
	ADS8383IB			98		
	ADS8383I	V_{IN} = 4 V_{pp} at 100 kHz		90		
	ADS8383IB			94		
–3dB Small signal bandwidth				3		MHz
Voltage Reference Input						
Reference voltage at REFIN, V_{ref}			2.5	4.096	4.2	V
Reference resistance (see Note 2)				100		kΩ
Reference current drain		f_S = 500 kHz			1	mA
Bias Input						
Bias input range			2	2.048	2.1	V
Bias input drift					±5	%FS
Bias input current, sink			–150	–100		µA

NOTES: 1 Calculated on the first nine harmonics of the input frequency

2 Can vary ±30%

SPECIFICATIONS (CONTINUED)

T_A = –40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output						
Logic family				CMOS		
Logic level	V_{IH}	I_{IH} = 5 µA	+VBD–1		$+V_{BD}$ + 0.3	V
	V_{IL}	I_{IL} = 5 µA	–0.3		0.8	
	V_{OH}	I_{OH} = 2 TTL loads	$+V_{BD}$ – 0.6			
	V_{OL}	I_{OL} = 2 TTL loads			0.4	
Data format				Straight Binary		
Power Supply Requirements						
Power supply voltage	+VBD (see Notes 1 and 2)		2.95	3.3	5.25	V
	+VA (see Note 2)		4.75	5	5.25	V
Supply current, 500-kHz sample rate (see Note 3)				22	26	mA
Power dissipation, 500-kHz sample rate (see Note 3)				110	130	mW
Temperature Range						
Operating free-air			–40		85	°C

NOTES: 1.. The difference between +VA and +VBD shoudl be no less than 2.3 V, i.e. if +VA is 5.5 V, +VBD should be at least 2.95 V.

2.. +VBD ≥ +VA – 2.3 V

3.. This includes only +VA current. +VBD current is typical 1 mA with 5 pF load capacitance on all output pins.

TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = +VBD = 5 V (see Notes 1, 2, and 3)

PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			1.5	µs
t_{ACQ}	Acquisition time	0.4			µs
t_{pd1}	$\overline{\text{CONVST}}$ low to conversion started (BUSY high)	10		50	ns
t_{pd2}	Propagation delay time, End of conversion to BUSY low	10		20	ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	40			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})		1	µs
t_{w4}	Pulse duration, BUSY signal high			1.52	µs
t_{h1}	Hold time, First data bus data transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low time	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			20	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	5			ns
t_{d3}	Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid	10		20	ns
t_{w6}	$\overline{\text{RD}}$ high	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	125			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge	Max(t_{d5})			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{16}$ rising edge to $\overline{\text{RD}}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{16}$ falling edge to $\overline{\text{RD}}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			20	ns
t_{d5}	Delay time, BUSY low to MSB data valid			30	ns
t_{su4}	Setup time, BYTE or BUS18/$\overline{16}$ change before BUSY falling edge	10		20	µs

NOTES:
1. All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
2. See timing diagrams.
3. All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

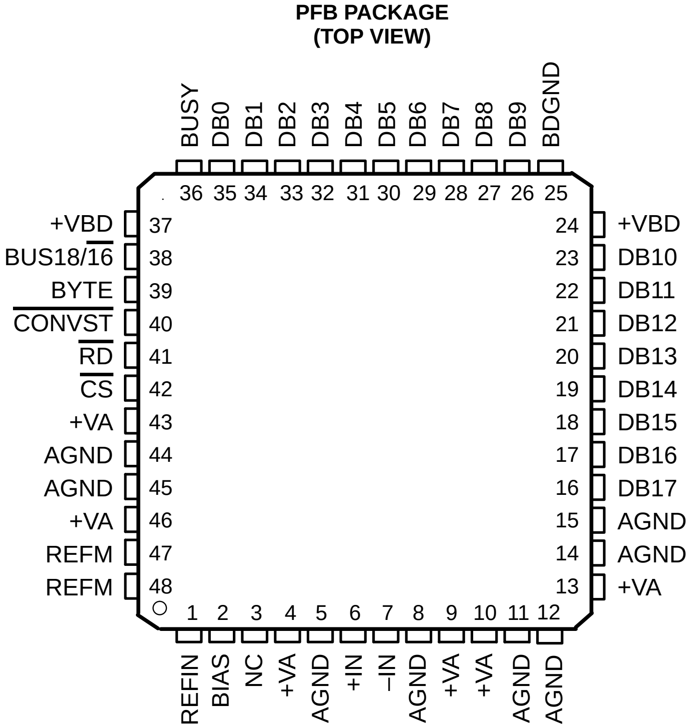
TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C, +VA = 5 V, +VBD = 3 V (see Notes 1, 2, and 3)

PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			1.5	µs
t_{ACQ}	Acquisition time	0.4			µs
t_{pd1}	$\overline{\text{CONVST}}$ low to conversion started (BUSY high)	10		50	ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low	10		20	ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	40			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})		1	µs
t_{w4}	Pulse duration, BUSY signal high			1.52	µs
t_{h1}	Hold time, first data bus transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS 18/$\overline{16}$ input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			30	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	10			ns
t_{d3}	Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid	10		30	ns
t_{w6}	Pulse duration, $\overline{\text{RD}}$ high time	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	125			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge	Max(td5)			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{16}$ rising edge to $\overline{\text{RD}}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{16}$ falling edge to $\overline{\text{RD}}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			30	ns
t_{d5}	Delay time, BUSY low to MSB data valid delay time			40	ns
t_{su4}	Setup time, BYTE or BUS18/$\overline{16}$ change before BUSY falling edge	10		30	µs

NOTES:
1. All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
2. See timing diagrams.
3. All timing are measured with 10 pF equivalent loads on all data bits and BUSY pins.

PIN ASSIGNMENTS

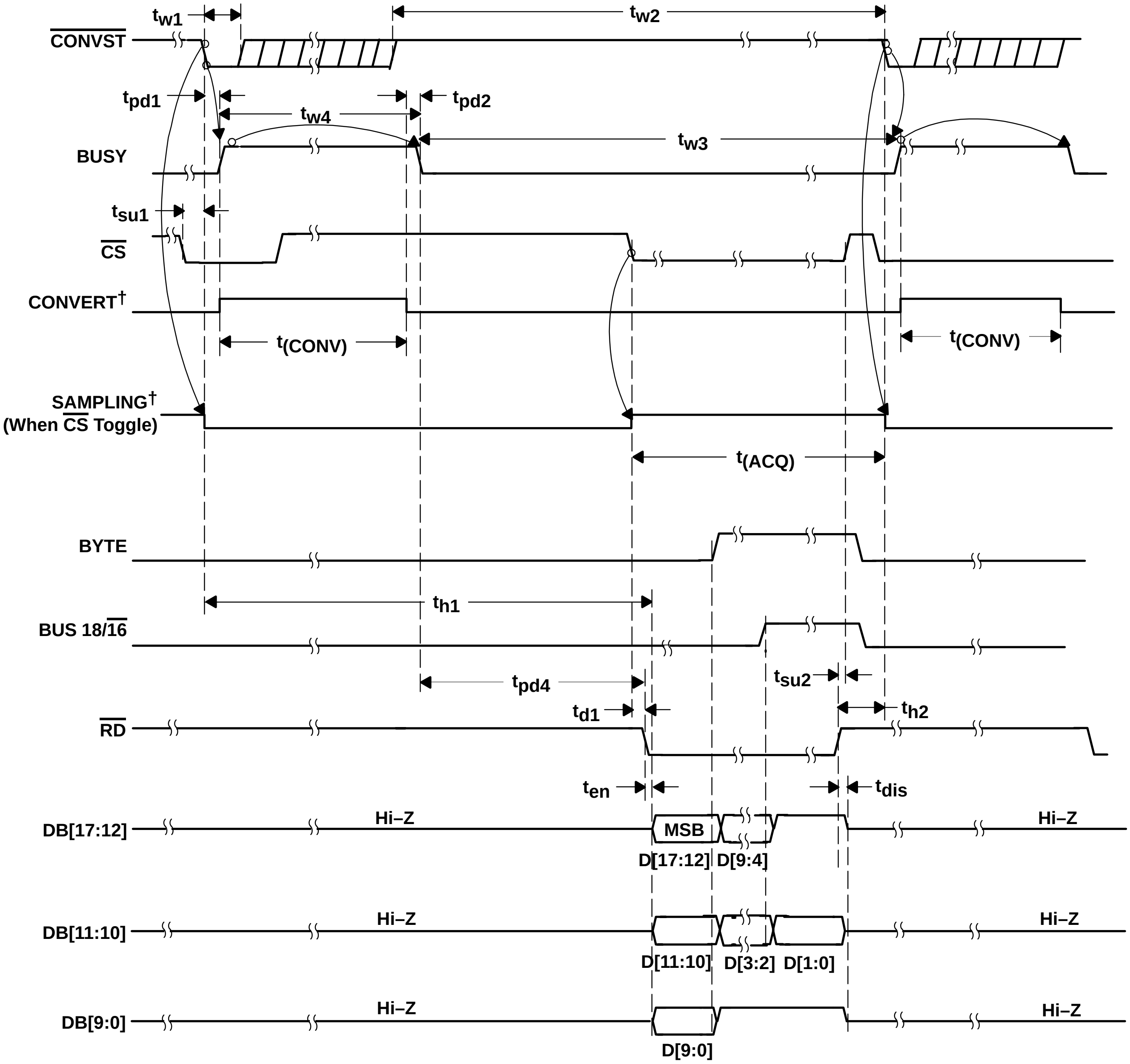


NC – No connection.

TERMINAL FUNCTIONS

<table>
<tr><th>NAME</th><th>NO.</th><th>I/O</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td>AGND</td><td>5, 8, 11, 12, 14, 15, 44, 45</td><td>–</td><td colspan="6">Analog ground</td></tr>
<tr><td>BDGND</td><td>25</td><td>–</td><td colspan="6">Digital ground for bus interface digital supply</td></tr>
<tr><td>BIAS</td><td>2</td><td>I</td><td colspan="6">Bias to internal circuit</td></tr>
<tr><td>BUSY</td><td>36</td><td>O</td><td colspan="6">Status output. High when a conversion is in progress.</td></tr>
<tr><td>BUS18/$\overline{16}$</td><td>38</td><td>I</td><td colspan="6">Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer.
0: Data bits output on the 18-bit data bus pins DB[17:0].
1: Last two data bits D[1:0] from 18-bit wide bus output on:
a) the low byte pins DB[9:2] if BYTE = 0
b) the high byte pins DB[17:10] if BYTE = 1</td></tr>
<tr><td>BYTE</td><td>39</td><td>I</td><td colspan="6">Byte select input. Used for 8-bit bus reading.
0: No fold back
1: Low byte D[9:2] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[17:10].</td></tr>
<tr><td>$\overline{\text{CONVST}}$</td><td>40</td><td>I</td><td colspan="6">Convert start</td></tr>
<tr><td>$\overline{\text{CS}}$</td><td>42</td><td>I</td><td colspan="6">Chip select</td></tr>
<tr><td rowspan="3">Data Bus</td><td rowspan="3"></td><td rowspan="3"></td><td colspan="3">8-Bit Bus</td><td colspan="2">16-Bit Bus</td><td>18-Bit Bus</td></tr>
<tr><td>BYTE = 0</td><td>BYTE = 1</td><td>BYTE = 1</td><td>BYTE = 0</td><td>BYTE = 0</td><td>BYTE = 0</td></tr>
<tr><td>BUS18/$\overline{16}$ = 0</td><td>BUS18/$\overline{16}$ = 0</td><td>BUS18/$\overline{16}$ = 1</td><td>BUS18/$\overline{16}$ = 0</td><td>BUS18/$\overline{16}$ = 1</td><td>BUS18/$\overline{16}$ = 0</td></tr>
<tr><td>DB17</td><td>16</td><td>O</td><td>D17 (MSB)</td><td>D9</td><td>All ones</td><td>D17 (MSB)</td><td>All ones</td><td>D17 (MSB)</td></tr>
<tr><td>DB16</td><td>17</td><td>O</td><td>D16</td><td>D8</td><td>All ones</td><td>D16</td><td>All ones</td><td>D16</td></tr>
<tr><td>DB15</td><td>18</td><td>O</td><td>D15</td><td>D7</td><td>All ones</td><td>D15</td><td>All ones</td><td>D15</td></tr>
<tr><td>DB14</td><td>19</td><td>O</td><td>D14</td><td>D6</td><td>All ones</td><td>D14</td><td>All ones</td><td>D14</td></tr>
<tr><td>DB13</td><td>20</td><td>O</td><td>D13</td><td>D5</td><td>All ones</td><td>D13</td><td>All ones</td><td>D13</td></tr>
<tr><td>DB12</td><td>21</td><td>O</td><td>D12</td><td>D4</td><td>All ones</td><td>D12</td><td>All ones</td><td>D12</td></tr>
<tr><td>DB11</td><td>22</td><td>O</td><td>D11</td><td>D3</td><td>D1</td><td>D11</td><td>All ones</td><td>D11</td></tr>
<tr><td>DB10</td><td>23</td><td>O</td><td>D10</td><td>D2</td><td>D0(LSB)</td><td>D10</td><td>All ones</td><td>D10</td></tr>
<tr><td>DB9</td><td>26</td><td>O</td><td>D9</td><td>All ones</td><td>All ones</td><td>D9</td><td>All ones</td><td>D9</td></tr>
<tr><td>DB8</td><td>27</td><td>O</td><td>D8</td><td>All ones</td><td>All ones</td><td>D8</td><td>All ones</td><td>D8</td></tr>
<tr><td>DB7</td><td>28</td><td>O</td><td>D7</td><td>All ones</td><td>All ones</td><td>D7</td><td>All ones</td><td>D7</td></tr>
<tr><td>DB6</td><td>29</td><td>O</td><td>D6</td><td>All ones</td><td>All ones</td><td>D6</td><td>All ones</td><td>D6</td></tr>
<tr><td>DB5</td><td>30</td><td>O</td><td>D5</td><td>All ones</td><td>All ones</td><td>D5</td><td>All ones</td><td>D5</td></tr>
<tr><td>DB4</td><td>31</td><td>O</td><td>D4</td><td>All ones</td><td>All ones</td><td>D4</td><td>All ones</td><td>D4</td></tr>
<tr><td>DB3</td><td>32</td><td>O</td><td>D3</td><td>All ones</td><td>All ones</td><td>D3</td><td>D1</td><td>D3</td></tr>
<tr><td>DB2</td><td>33</td><td>O</td><td>D2</td><td>All ones</td><td>All ones</td><td>D2</td><td>D0 (LSB)</td><td>D2</td></tr>
<tr><td>DB1</td><td>34</td><td>O</td><td>D1</td><td>All ones</td><td>All ones</td><td>D1</td><td>All ones</td><td>D1</td></tr>
<tr><td>DB0</td><td>35</td><td>O</td><td>D0 (LSB)</td><td>All ones</td><td>All ones</td><td>D0 (LSB)</td><td>All ones</td><td>D0 (LSB)</td></tr>
<tr><td>–IN</td><td>7</td><td>I</td><td colspan="6">Inverting input channel</td></tr>
<tr><td>+IN</td><td>6</td><td>I</td><td colspan="6">Noninverting input channel</td></tr>
<tr><td>NC</td><td>3</td><td>–</td><td colspan="6">No connection</td></tr>
<tr><td>REFIN</td><td>1</td><td>I</td><td colspan="6">Reference input.</td></tr>
<tr><td>REFM</td><td>47, 48</td><td>I</td><td colspan="6">Reference ground.</td></tr>
<tr><td>$\overline{\text{RD}}$</td><td>41</td><td>I</td><td colspan="6">Synchronization pulse for the parallel output.</td></tr>
<tr><td>+VA</td><td>4, 9, 10, 13, 43, 46</td><td>–</td><td colspan="6">Analog power supplies, 5-V dc</td></tr>
<tr><td>+VBD</td><td>24, 37</td><td>–</td><td colspan="6">Digital power supply for bus</td></tr>
</table>

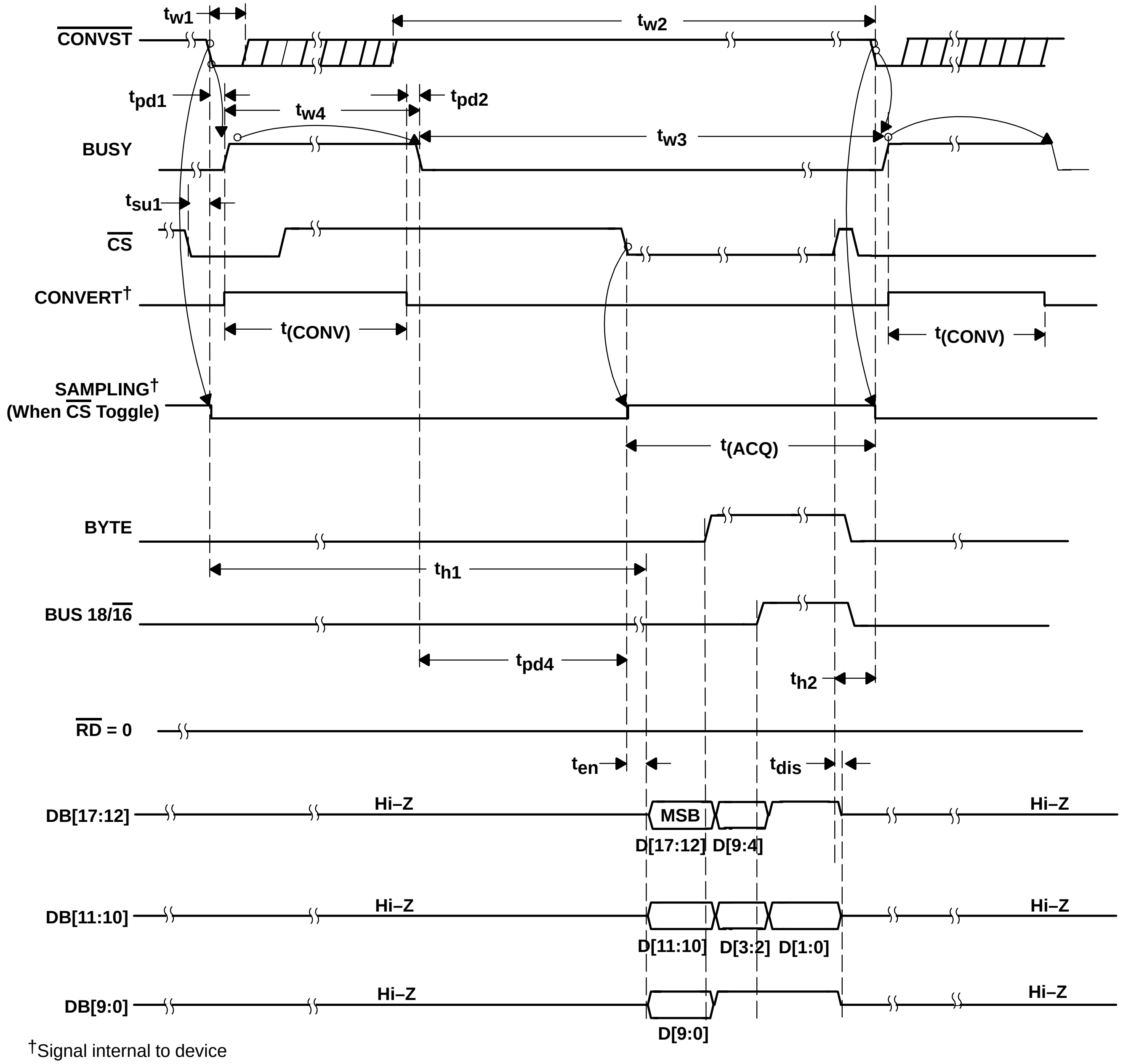
TIMING DIAGRAMS



†Signal internal to device

Figure 1. Timing for Conversion and Acquisition Cycles With CS and RD Toggling

TIMING DIAGRAMS (CONTINUED)

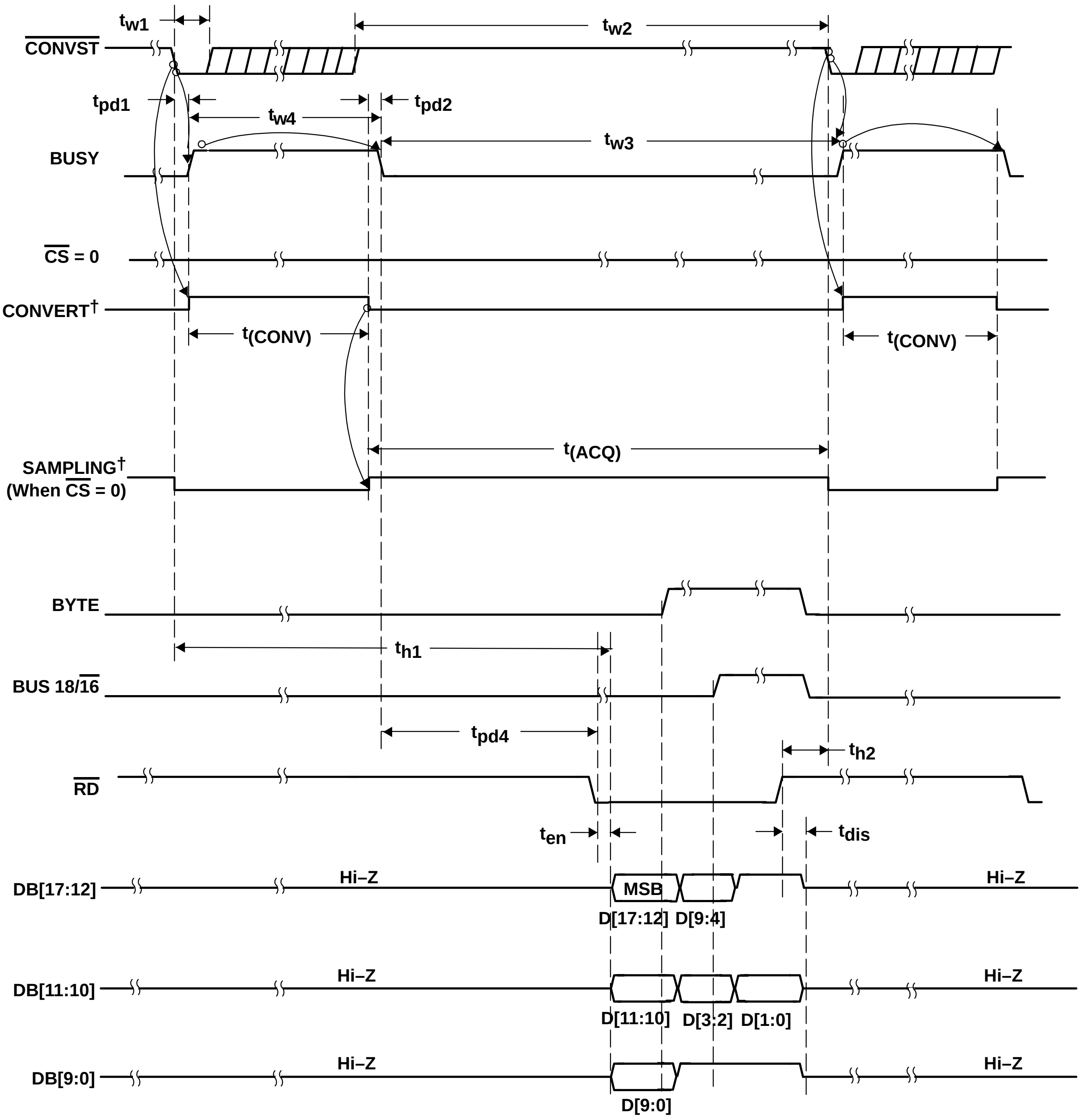


†Signal internal to device

NOTE: $\overline{\text{RD}}$ cannot be tied to BDGND. Three read cycles are required at power on.

Figure 2. Timing for Conversion and Acquisition Cycles With $\overline{\text{CS}}$ Toggling, $\overline{\text{RD}}$ Tied to BDGND

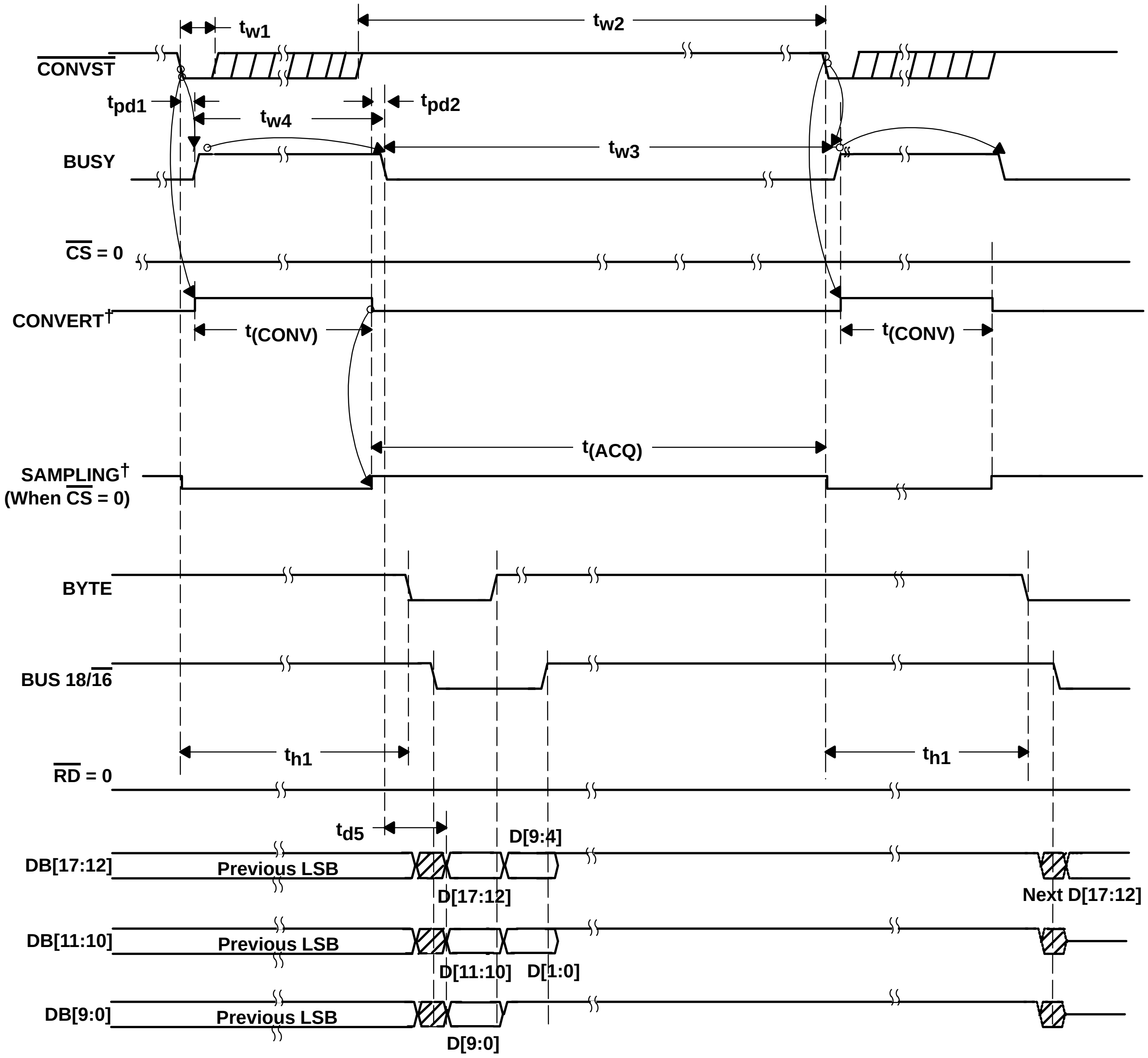
TIMING DIAGRAMS (CONTINUED)



†Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With CS Tied to BDGND, RD Toggling

TIMING DIAGRAMS (CONTINUED)



†Signal internal to device

NOTE: RD cannot be tied to BDGND. Three read cycles are required at power on.

Figure 4. Timing for Conversion and Acquisition Cycles With CS and RD Tied to BDGND - Auto Read

TIMING DIAGRAMS (CONTINUED)

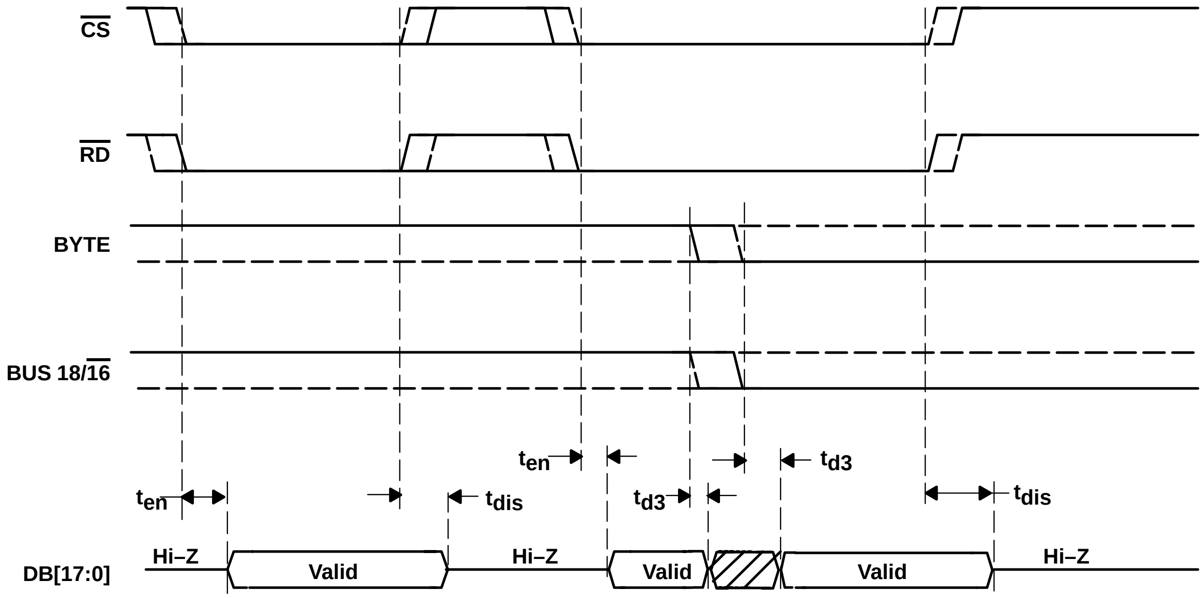


Figure 5. Detailed Timing for Read Cycles

TYPICAL CHARACTERISTICS†

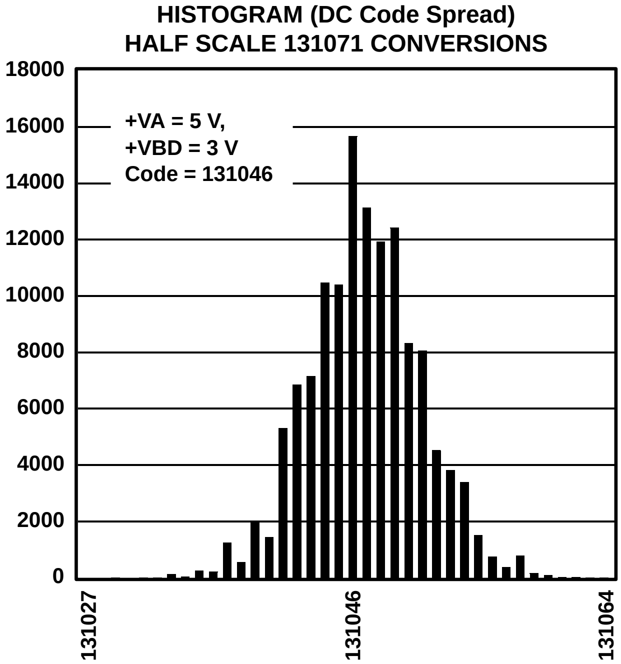


Figure 6

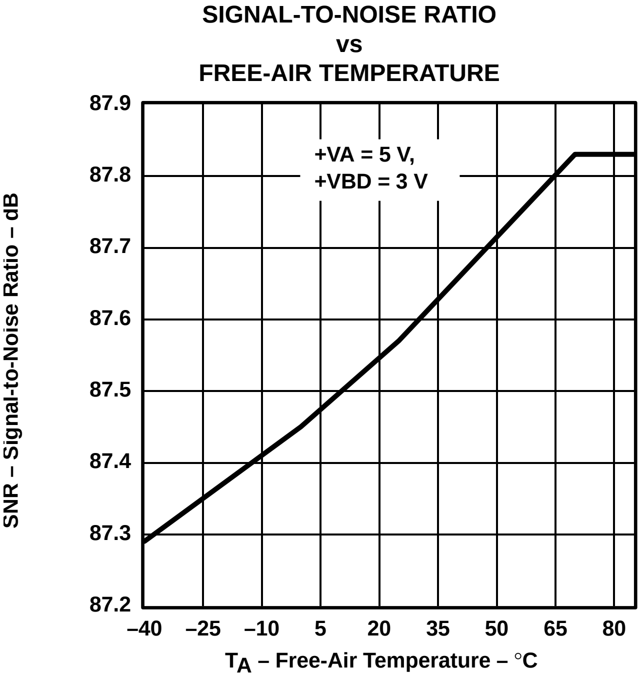


Figure 7

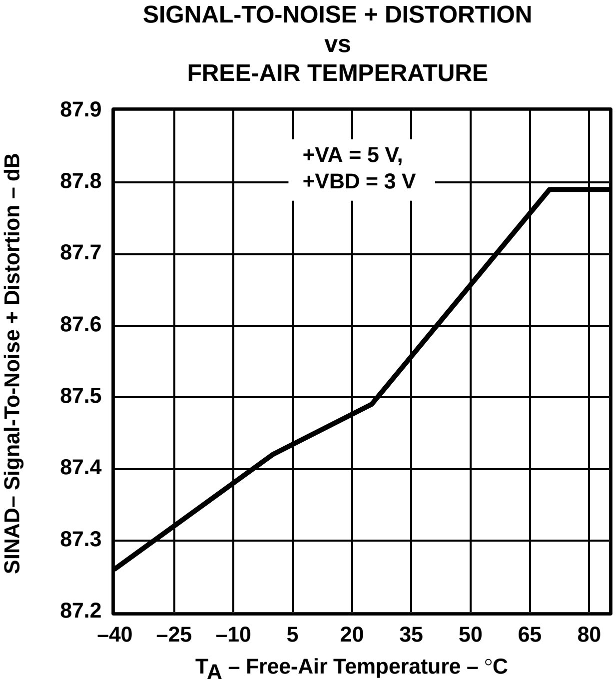


Figure 8

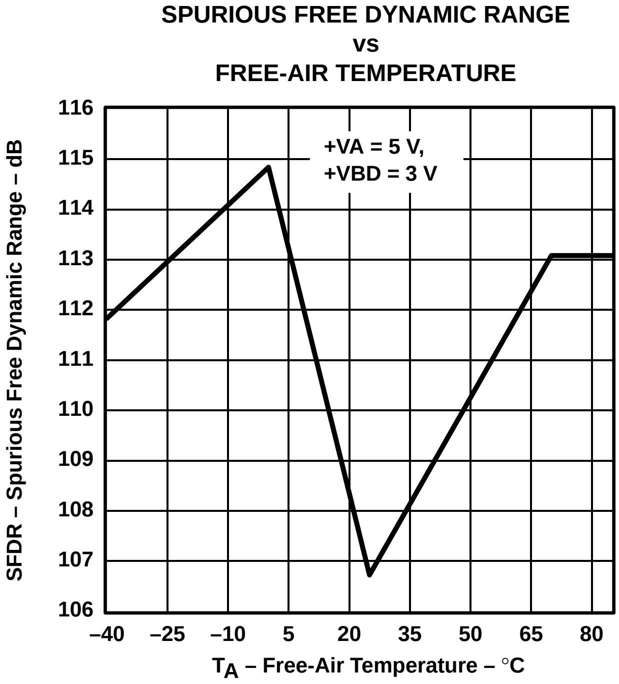


Figure 9

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

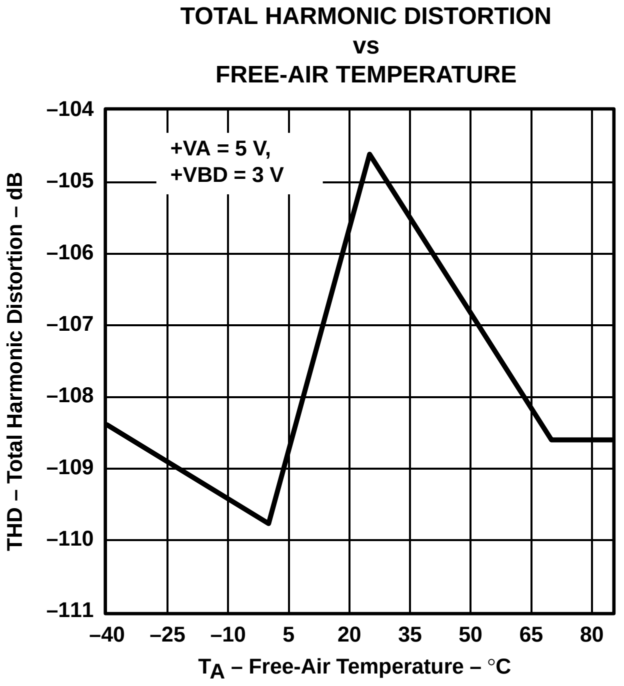


Figure 10

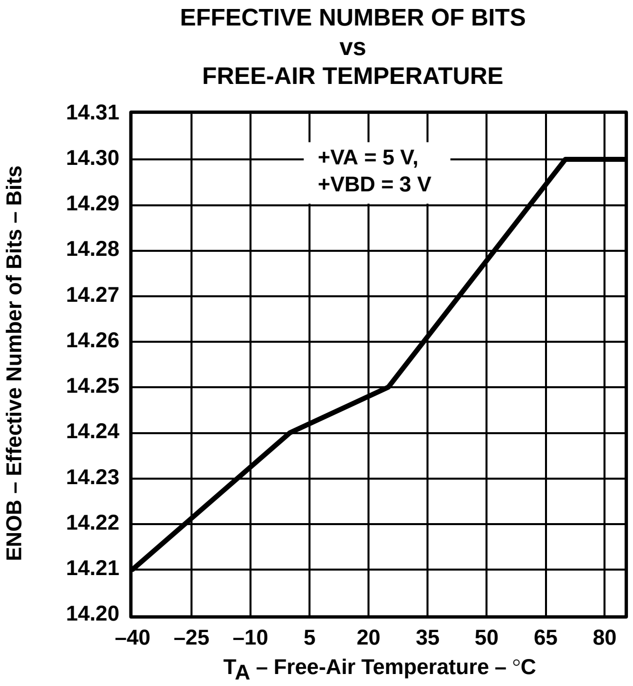


Figure 11

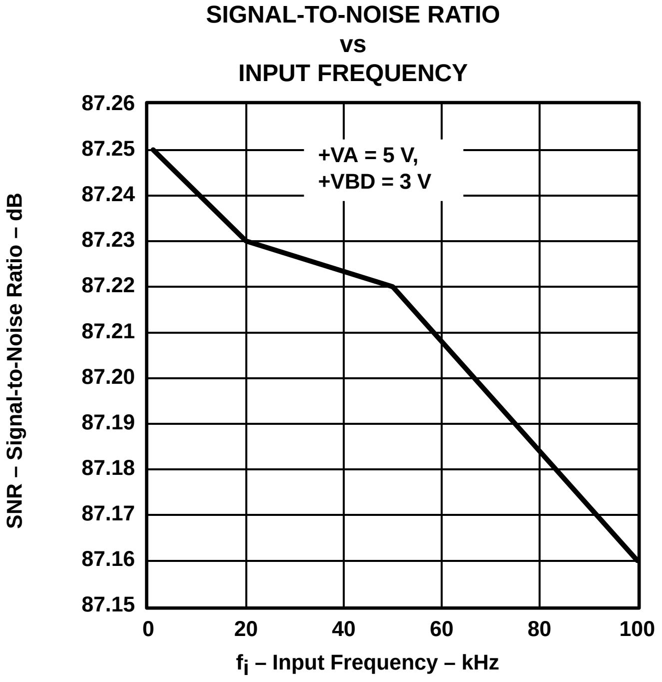


Figure 12

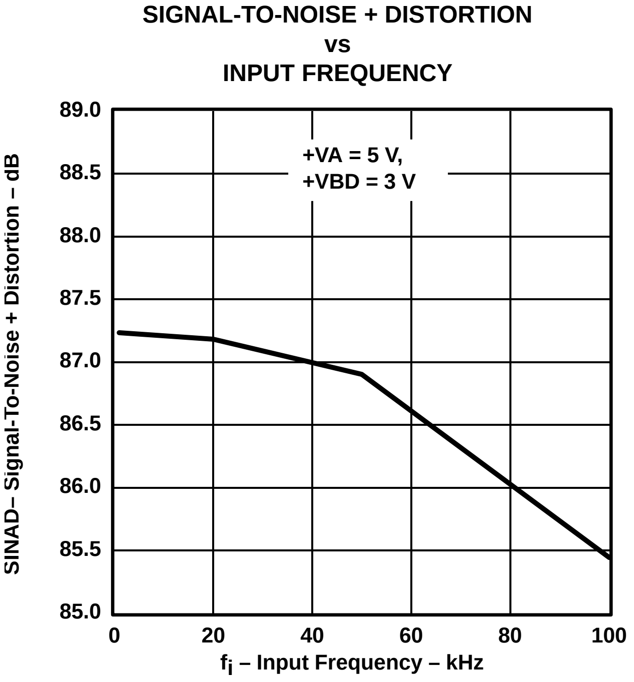


Figure 13

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

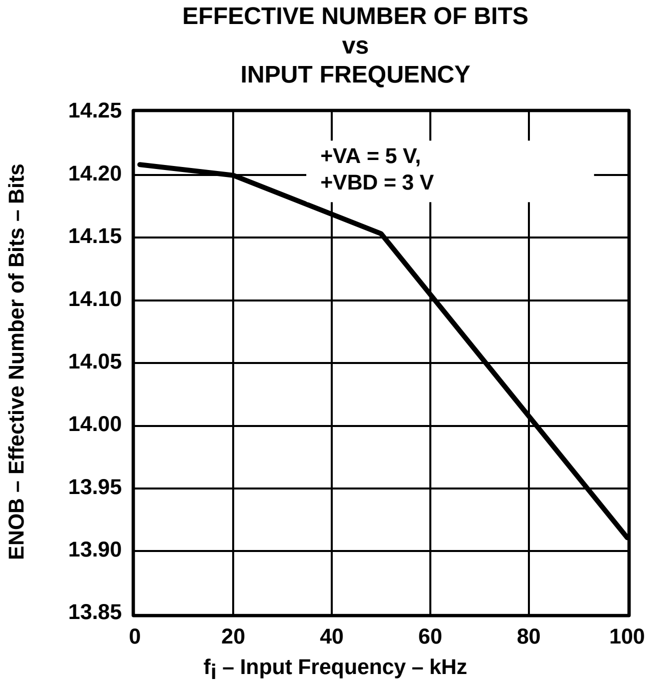


Figure 14

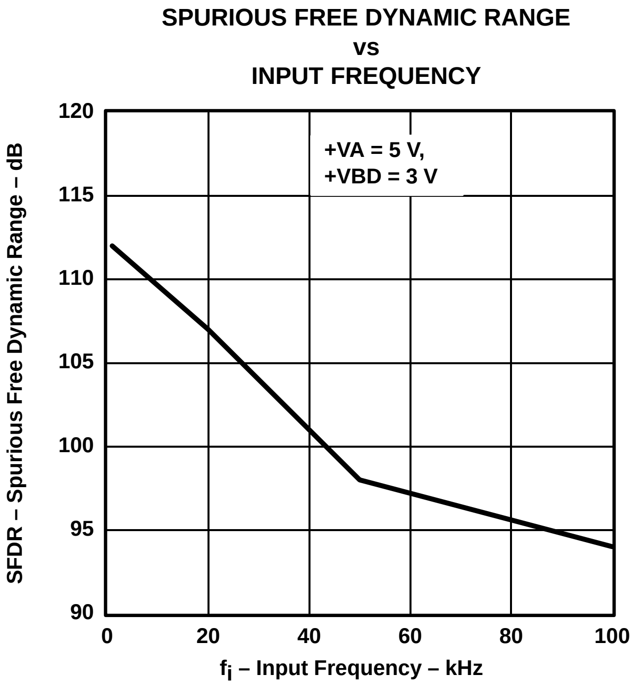


Figure 15

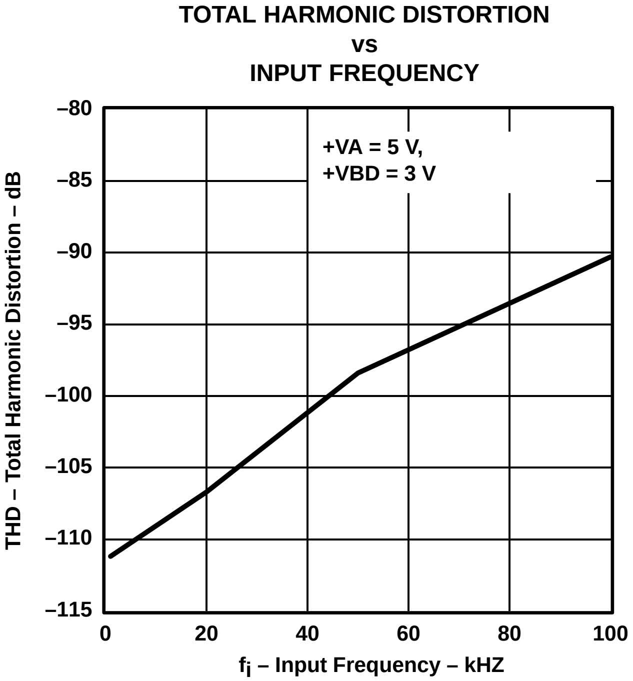


Figure 16

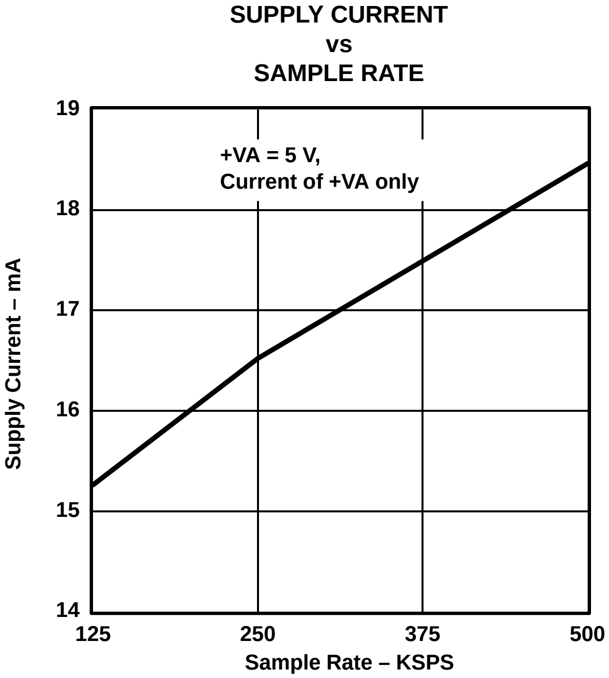


Figure 17

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† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

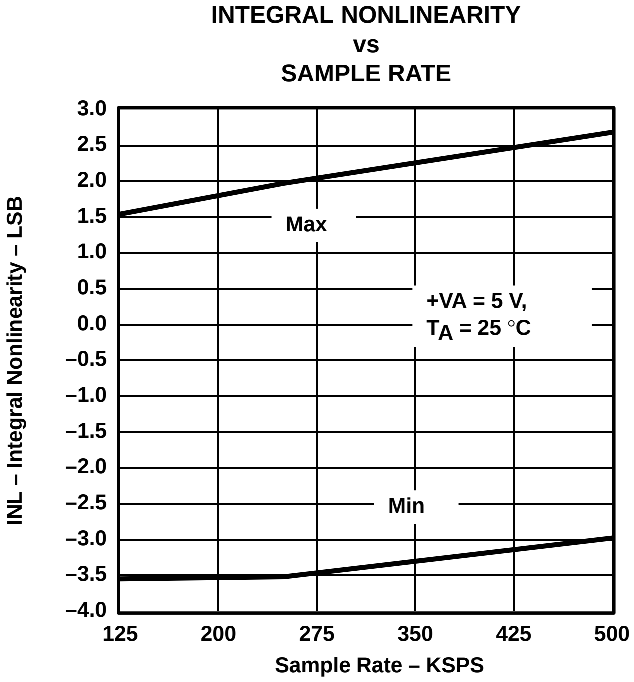

Figure 18

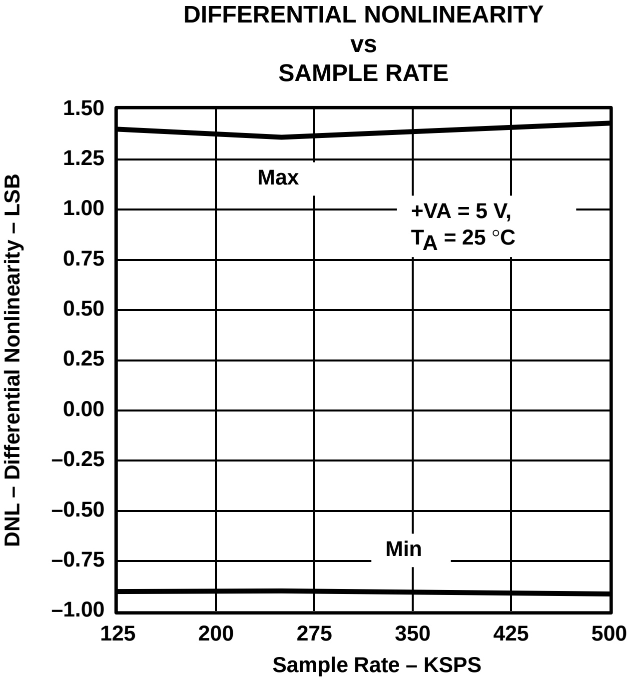

Figure 19

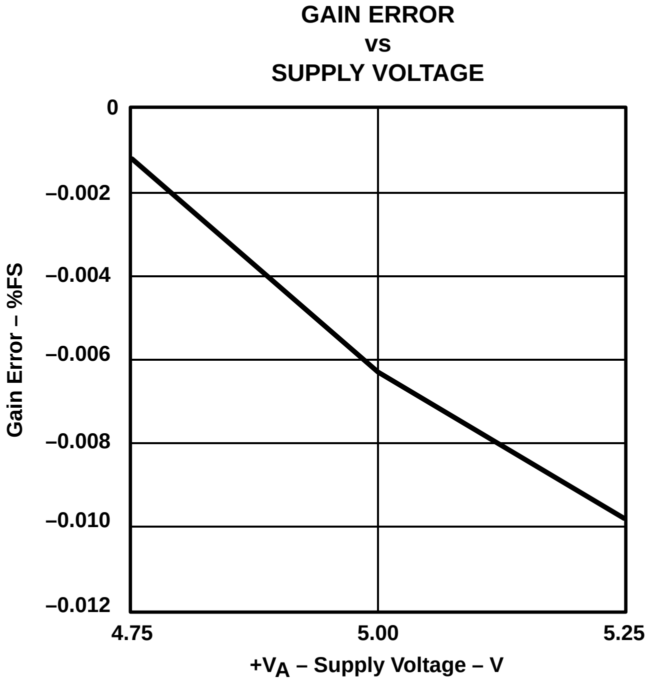

Figure 20

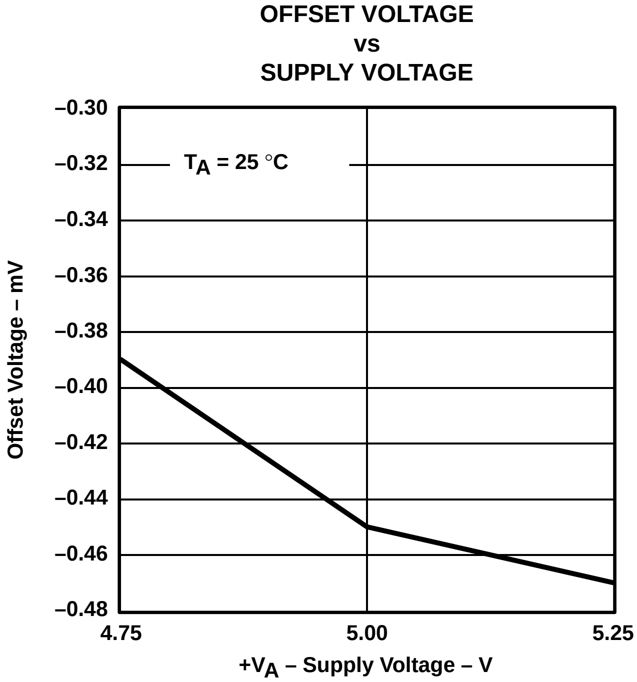

Figure 21

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

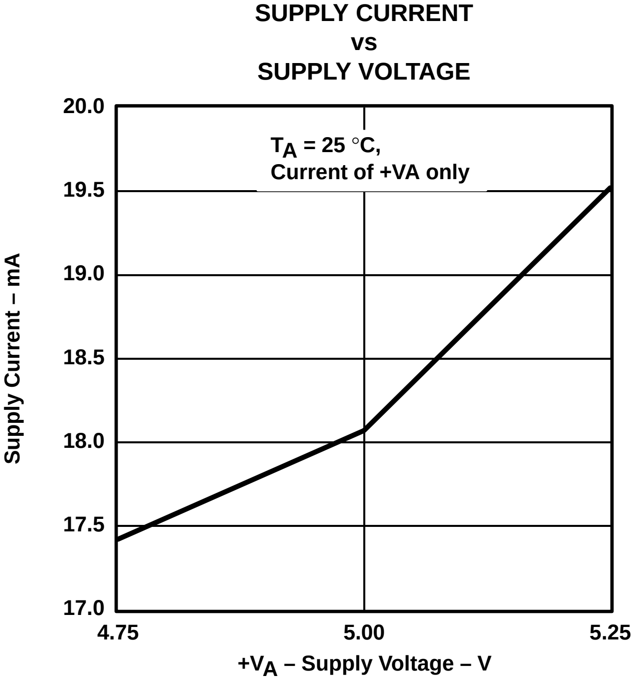

Figure 22

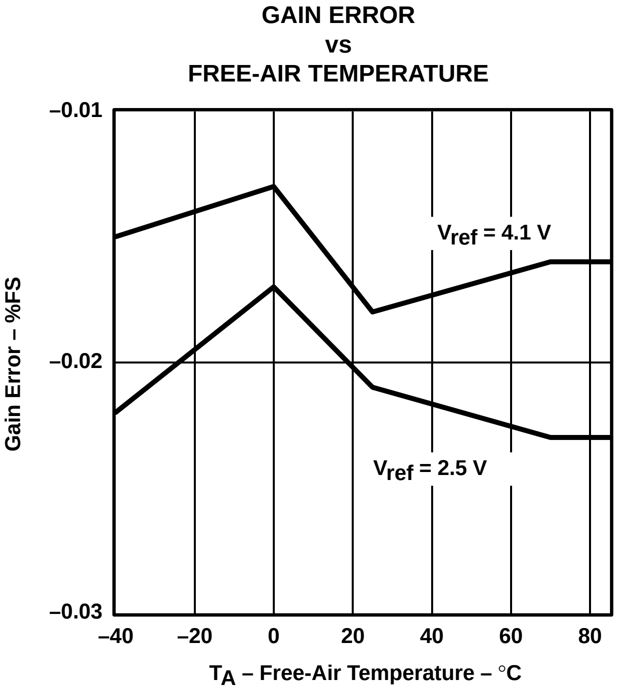

Figure 23

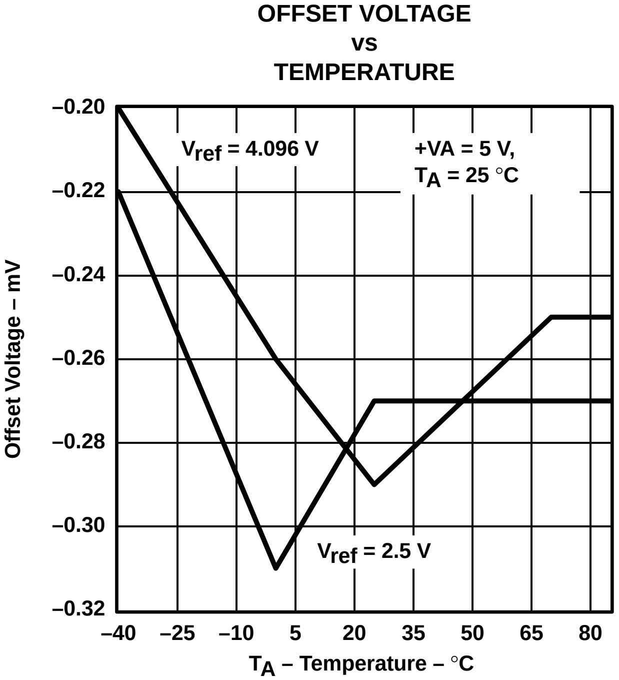

Figure 24

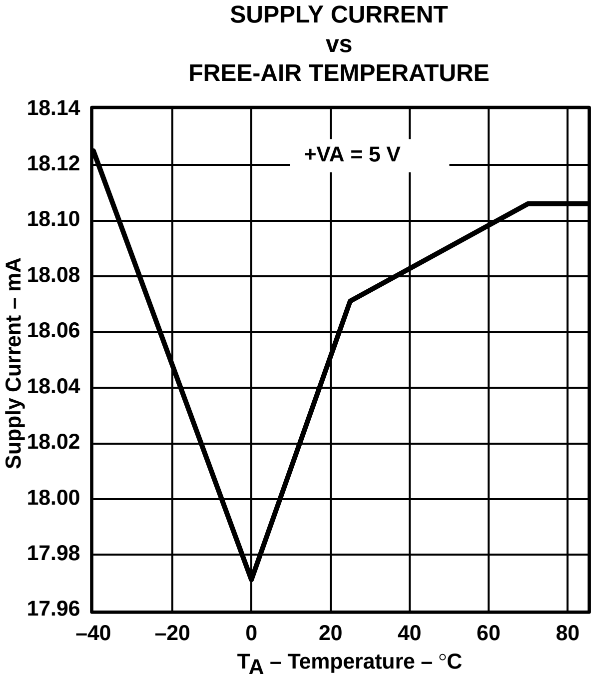

Figure 25

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† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

DIFFERENTIAL NONLINEARITY (Max)
vs
TEMPERATURE

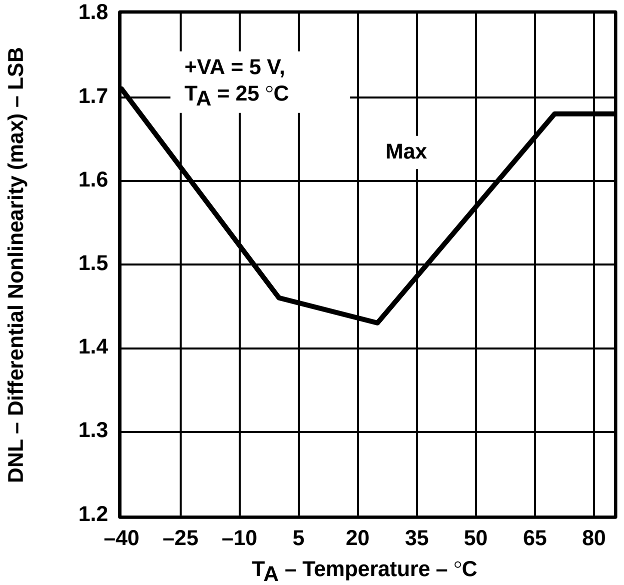


Figure 26

DIFFERENTIAL NONLINEARITY (Min)
vs
TEMPERATURE

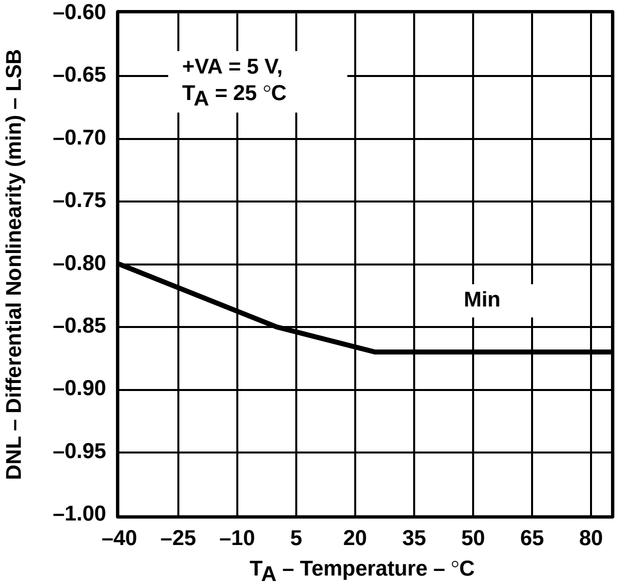


Figure 27

INTEGRAL NONLINEARITY (Max)
vs
TEMPERATURE

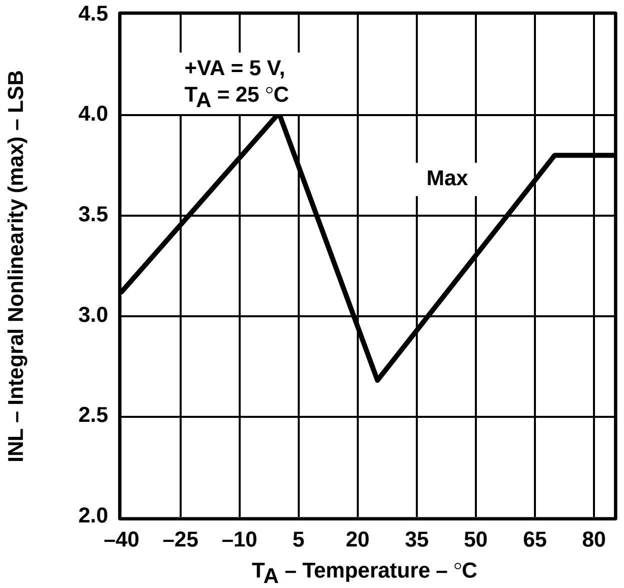


Figure 28

INTEGRAL NONLINEARITY (Min)
vs
TEMPERATURE

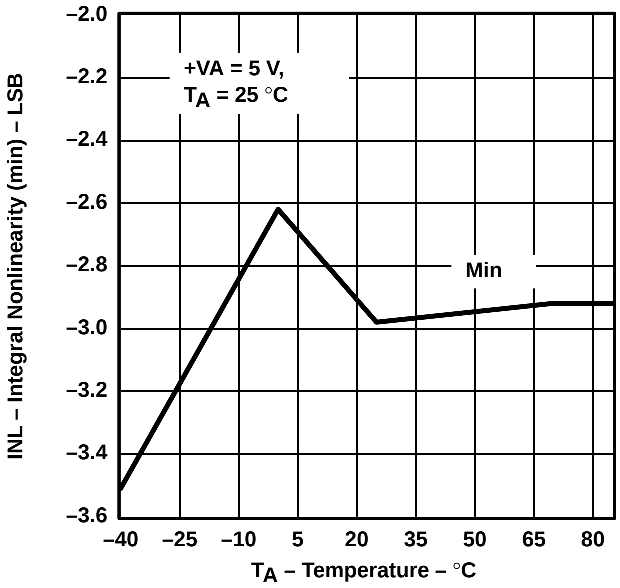


Figure 29

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

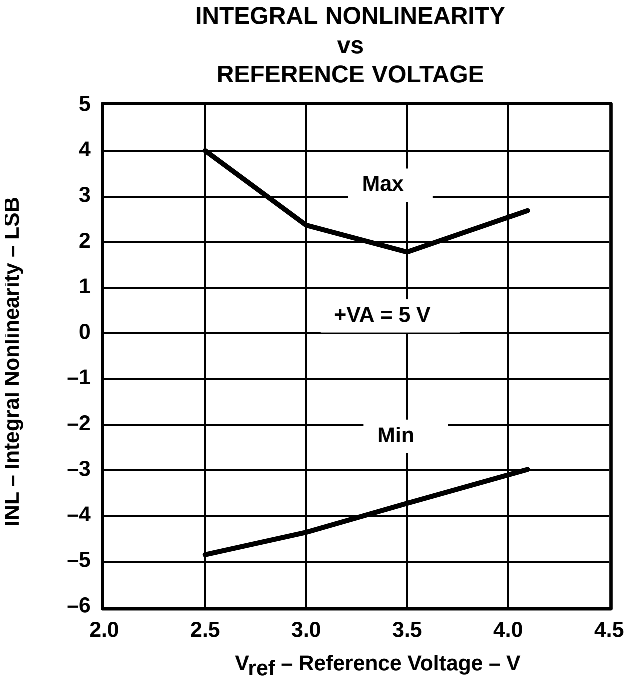


Figure 30

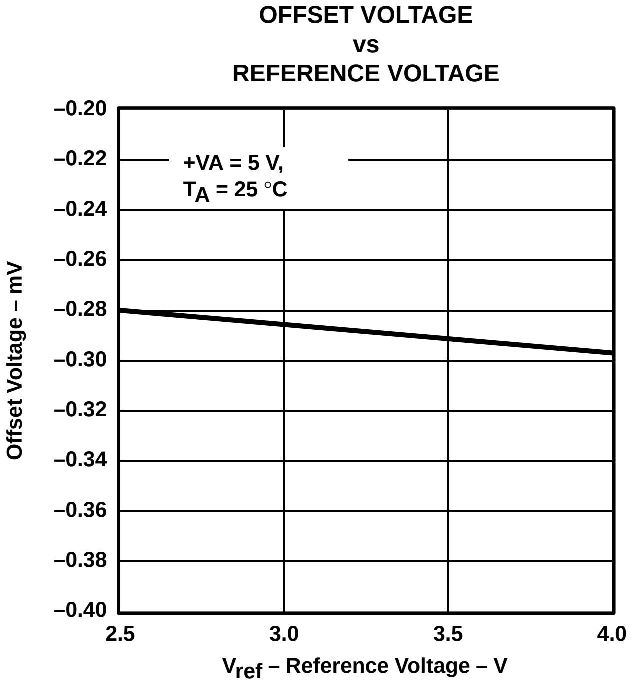


Figure 31

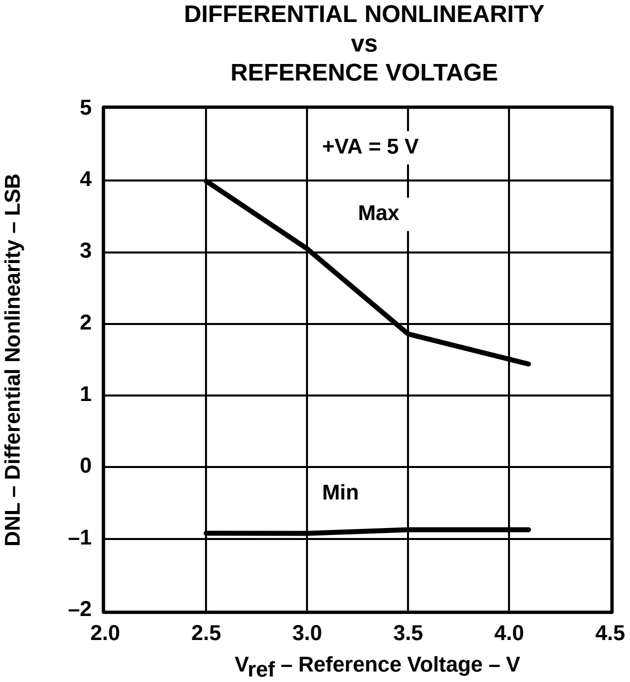


Figure 32

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

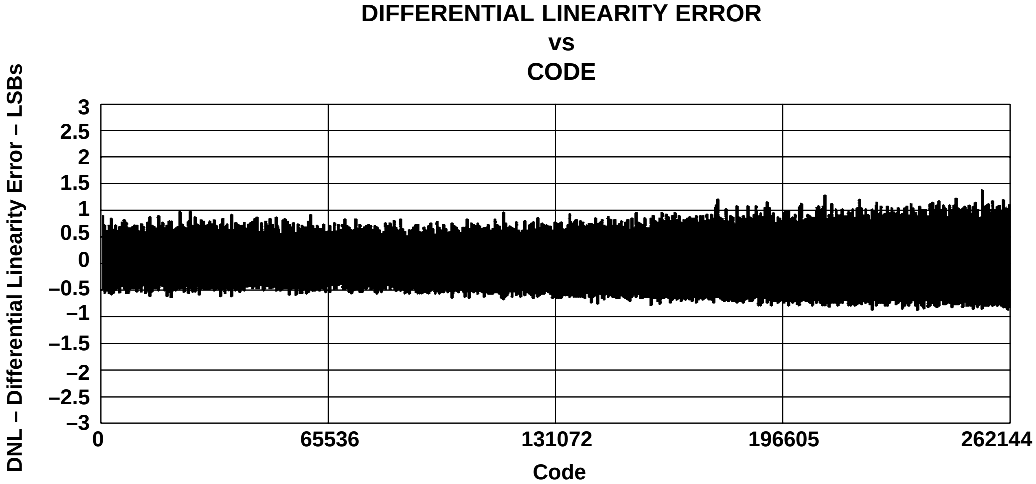


Figure 33

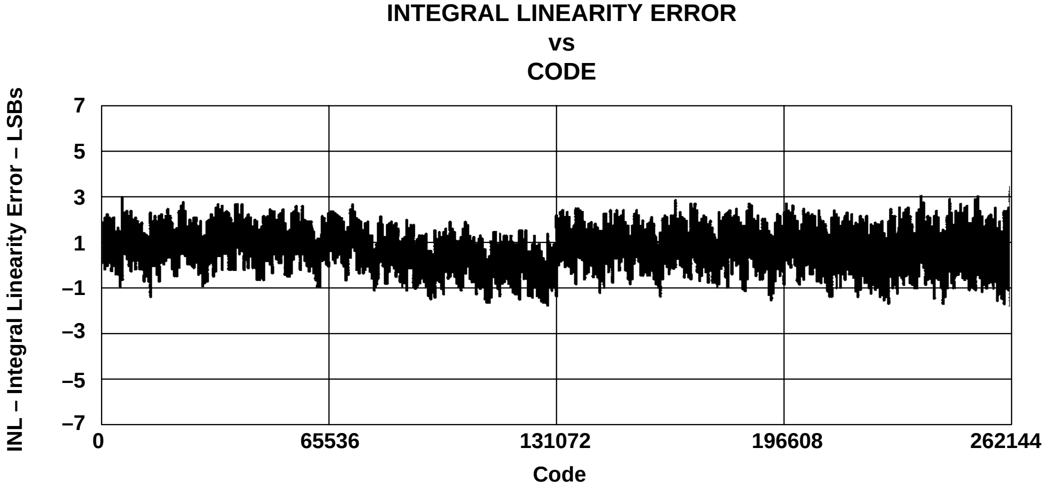


Figure 34

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

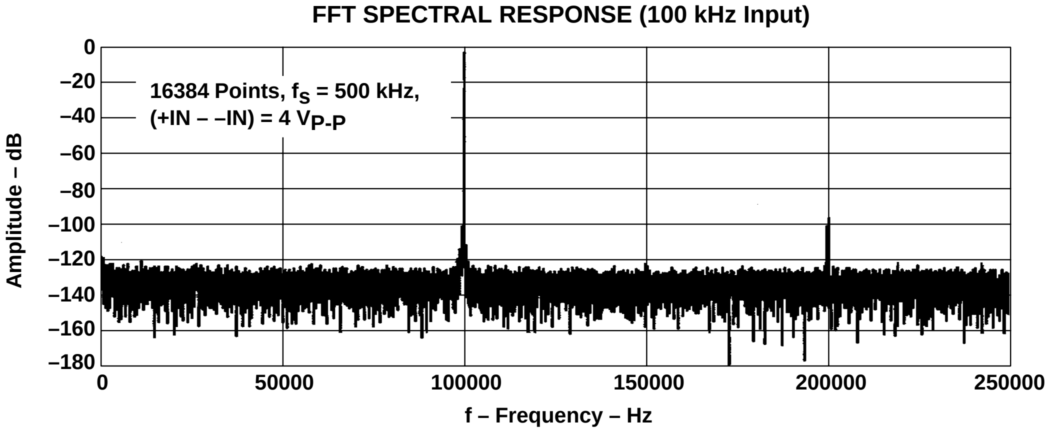


Figure 35

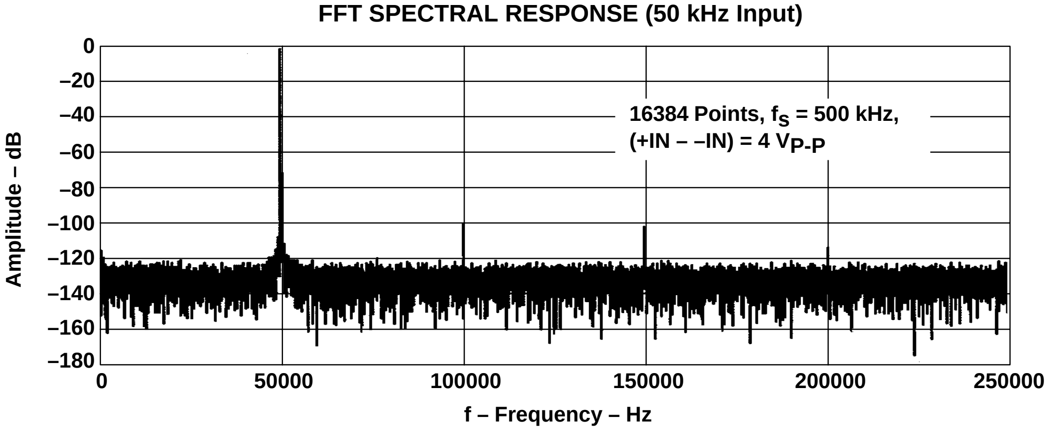


Figure 36

† At –40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

APPLICATION INFORMATION

MICROPROCESSOR INTERFACING

ADS8383 to 8-Bit Microprocessor Interface

Figure 37 shows a parallel interface between the ADS8383 and a typical micro controller using the 8-bit data bus.

The BUSY signal is used as a falling-edge interrupt to the microprocessor.

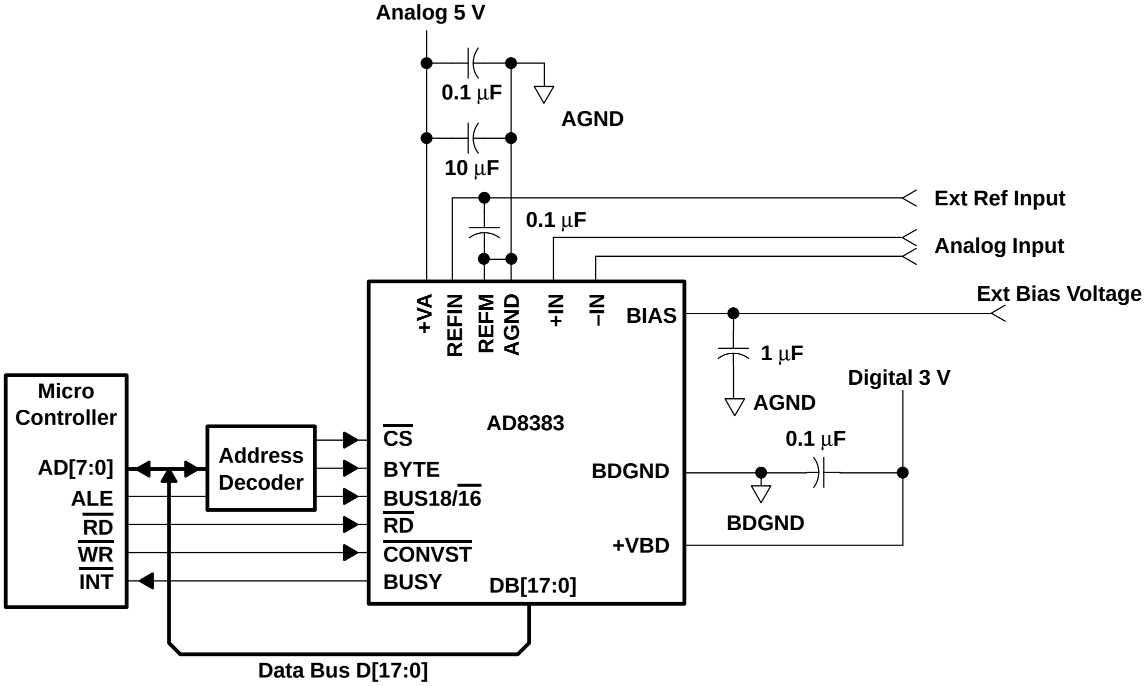


Figure 37. ADS8383 Application Circuitry

PRINCIPLES OF OPERATION

The ADS8383 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 37 for the application circuit for the ADS8383.

The conversion clock is generated internally. The conversion time of 1.6 µs is capable of sustaining a 500-kHz throughput.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8383 can operate with an external 4.096-V reference for a corresponding full-scale range of 4.096 V.

BIASING THE ADS8383

The ADS8383 requires an external 2.048-V bandgap reference to generate the bias currents for internal circuitry. Figure 38 shows the internal circuitry used to generate the bias currents. The bias generation circuit also pumps 100 µA (150 µA max) out from the BIAS pin. The bandgap used should be capable of sinking 100 µA (150 µA max) while holding the voltage on the pin steady. Table 1 shows the specification of the bandgap used to drive the BIAS pin of the ADS8383.

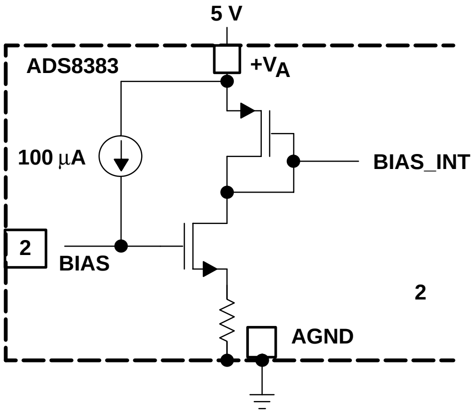


Figure 38. Bias Current Generation

Table 1. Bias Specifications

PARAMETER	MIN	TYP	MAX	UNITS
Output Voltage	2	2.048	2.1	V
I_{sink}		100	150	µA

Any common bandgap like REF3020 can be used to drive the BIAS pin of the ADS8383. Figure 39 shows how REF3020 can be used with the ADS8383. A 1 µF decoupling capacitor is recommended between pins 2 and AGND of the ADS8383 for optimal performance.

PRINCIPLES OF OPERATION

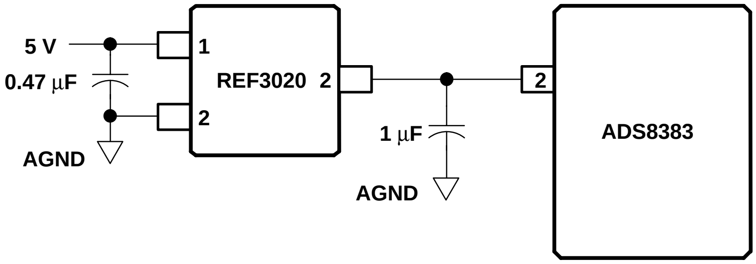


Figure 39. Using the REF3020 to Drive the ADS8383 BIAS Pin

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.2 V to V_{ref} + 0.2 V. The input span (+IN – (–IN)) is limited to 0 V to V_{ref}.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8383 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 18-bit settling level within the acquisition time (400 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array.

PRINCIPLES OF OPERATION

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8383 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The ADS8383 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high through the conversion process and returns low when the conversion has ended.

Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

Reading Data

The ADS8383 outputs full parallel data in straight binary format as shown in Table 2. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 125 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ sets the parallel output to 3-state. BYTE and BUS18/$\overline{16}$ are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/$\overline{16}$ is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 2 for ideal output codes.

Table 2. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
FULL SCALE RANGE	V_{ref}		
Least significant bit (LSB)	V_{ref}/262144	BINARY CODE	HEX CODE
Full scale	V_{ref} – 1 LSB	11 1111 1111 1111 1111	3FFFF
Midscale	V_{ref}/2	10 0000 0000 0000 0000	20000
Midscale – 1 LSB	V_{ref}/2 – 1 LSB	01 1111 1111 1111 1111	1FFFF
Zero	0 V	00 0000 0000 0000 0000	00000

The output data is a full 18-bit word (D17–D0) on DB17–DB0 (MSB–LSB) if both BUS18/$\overline{16}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/$\overline{16}$ high while holding BYTE low. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

PRINCIPLES OF OPERATION

DIGITAL INTERFACE (CONTINUED)

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/$\overline{16}$ and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/$\overline{16}$ low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/$\overline{16}$ high while holding BYTE high. When BUS18/$\overline{16}$ is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active $\overline{\text{RD}}$ (toggling) or with $\overline{\text{RD}}$ held low for simplicity. This is referred to as the AUTO READ operation. Note that $\overline{\text{RD}}$ may not be tied to BDGND permanently due to the requirement of power-on initialization.

Table 3. Conversion Data Read Out

BYTE	BUS18/$\overline{16}$	DATA READ OUT				
		DB17–DB12	**DB11–DB10**	**DB9–DB4**	**DB3–DB2**	**DB1–DB0**
High	High	All One’s	D1–D0	All One’s	All One’s	All One’s
Low	High	All One’s	All One’s	All One’s	D1–D0	All One’s
High	Low	D9–D4	D3–D2	All One’s	All One’s	All One’s
Low	Low	D17–D12	D11–D10	D9–D4	D3–D2	D1–D0

POWER-ON INITIALIZATION

At first power on there are three read cycles required ($\overline{\text{RD}}$ must be toggled three times). If conversion cycle is attempted before these intialization read cycles, the first three conversion cycles will not produce valid results. This is used to load factory trimming data for a specific device to assure high accuracy of the converter. Because of this requirement, the $\overline{\text{RD}}$ pin cannot be tied permanently to BDGND. System designers can still achieve the AUTO READ function if the power-on requirement is satisfied.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8383 circuitry.

As the ADS8383 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8383 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor is recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

PRINCIPLES OF OPERATION

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

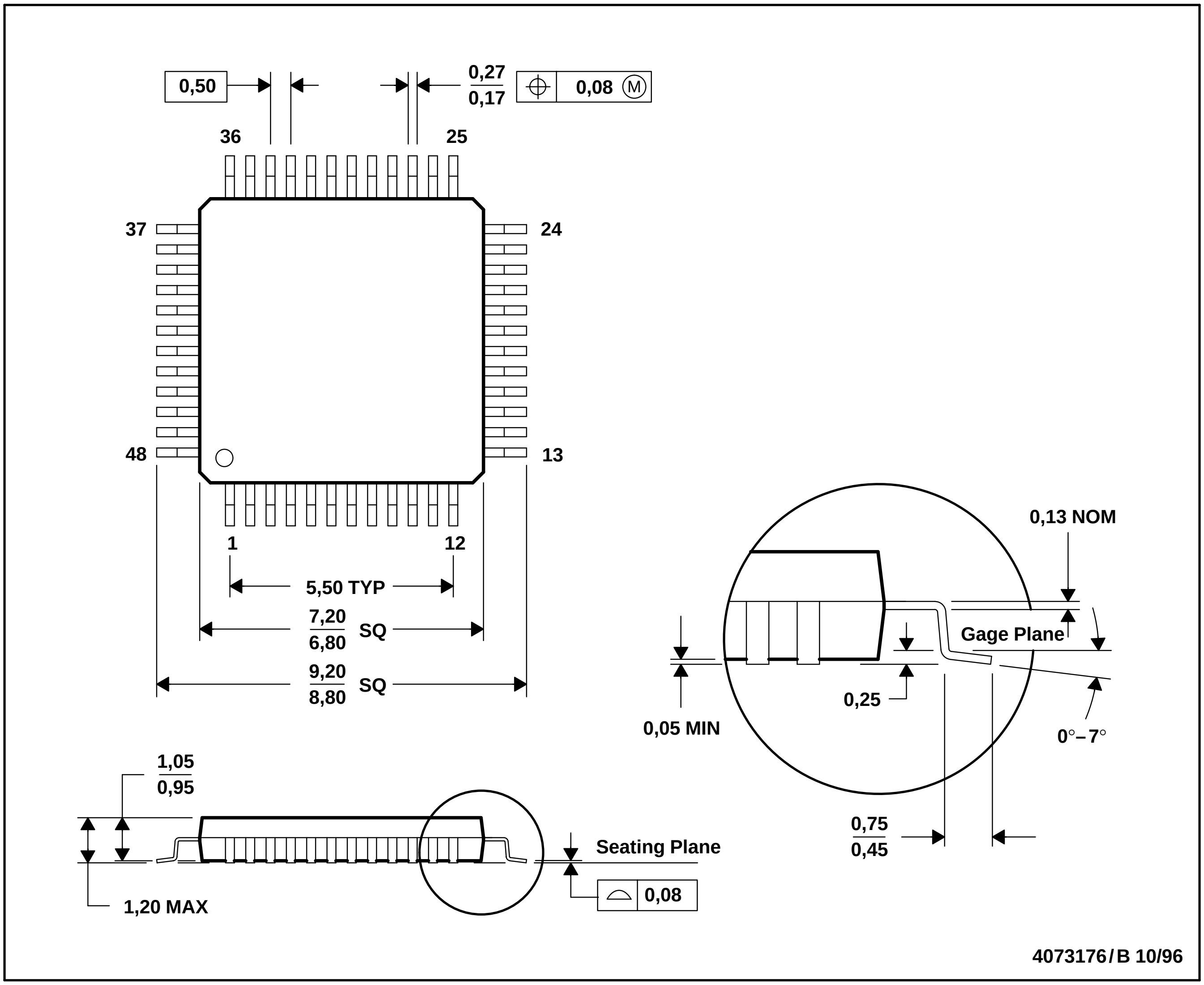
As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8383 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1-µF to 10-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 4. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
SUPPLY PINS		
Pin pairs that require shortest path to decoupling capacitors	(4,5), (8,9), (10,11), (13,15), (43,44), (45,46)	(24,25)
Pins that require no decoupling	12, 14	37

MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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