FAIRCHILD
SEMICONDUCTOR®

SPT9693

WIDE INPUT VOLTAGE, JFET COMPARATOR

TECHNICAL DATA

MARCH 1, 2001

FEATURES

- Common mode range –3.0 to +8.0 V
- Low input bias current <100 pA
- Propagation delay 1.5 ns (max)
- Low offset ±25 mV
- Low feedthrough and crosstalk
- Differential latch control

APPLICATIONS

- Automated test equipment
- High-speed instrumentation
- Window comparators
- High-speed timing
- Line receivers
- High-speed triggers
- Threshold detection
- Peak detection

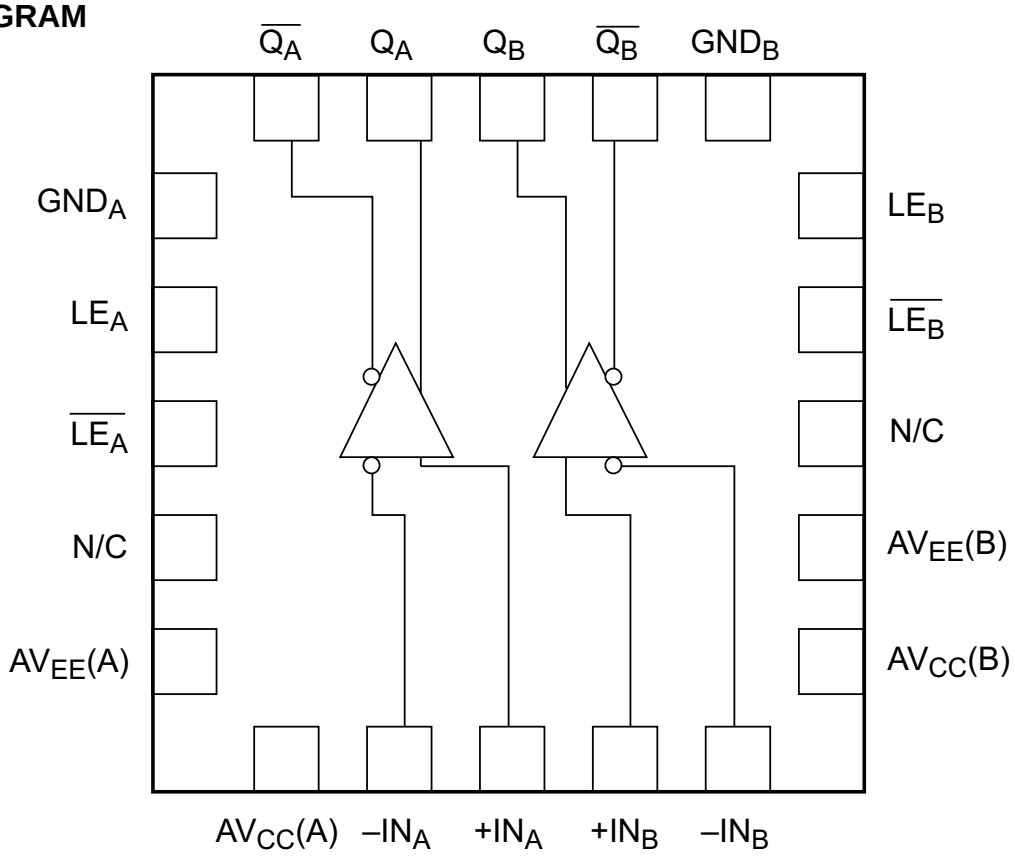
GENERAL DESCRIPTION

The SPT9693 is a high-speed, wide common mode voltage, JFET input, dual comparator. It is designed for applications that measure critical timing parameters in which wide common mode input voltages of –3.0 to +8.0 V are required. Propagation delays are constant for overdrives greater than 50 mV.

JFET inputs reduce the input bias currents to the nanoamp level, eliminating the need for input drivers and buffers in most applications. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. Each comparator has a complementary latch enable control that can be driven by standard ECL logic.

The SPT9693 is available in 20-contact LCC and 20-lead PLCC packages over the commercial temperature range. It is also available in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages (Measured to GND)

Positive Supply Voltage (AV_{CC}) ..... –0.5 to +11.0 V
Negative Supply Voltage (AV_{EE}) ..... –11.0 to +0.5 V

Input Voltages

Input Common Mode Voltage ..... –6 to +AV_{CC}+1
Differential Input Voltage ..... –12.0 to +12.0 V
Input Voltage, Latch Controls ..... –6 to 0.5 V
V_{IN} to AV_{CC} Differential Voltage ..... –16 to +1.0 V
V_{IN} to AV_{EE} Differential Voltage ..... +4 to +21.0 V

Output

Output Current ..... 30 mA

Temperature

Operating Temperature, ambient ..... 0 to +70 °C
junction.....+150 °C
Lead Temperature, (soldering 60 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, AV_{CC} = +10 V, AV_{EE} = –10.0 V, R_L = 50 Ohm to –2 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Offset Voltage	V_{IN} (Common Mode) = 0	I	–25	0.0	+25	mV
	$T_{MIN}<T_A<T_{MAX}$	IV	–25	0.0	+25	mV
Offset Voltage Tempco		V		50		µV/°C
Input Bias Current	$T_{MIN}<T_A<T_{MAX}$ V_{IN} (Common Mode) = –3 to +7 V	I		±10	±100	nA
Input Bias Current	$T_{MIN}<T_A<T_{MAX}$ V_{IN} (Common Mode) = +7 to +8 V	I		±50	±150	nA
Input Offset Current		V		±1.0		nA
	$T_{MIN}<T_A<T_{MAX}$	V		±10		nA
Positive Supply Current (Dual)	AV_{CC}=10 V	I		3	6	mA
Negative Supply Current (Dual)	AV_{EE}=–10.0 V	I		40	55	mA
Positive Supply Voltage, AV_{CC}		IV	9.75	10.0	10.25	V
Negative Supply Voltage, AV_{EE}		IV	–9.75	–10.0	–10.25	V
Input Common Mode Range		I	–3.0		+8.0	V
Latch Enable Common Mode Range		IV	–2.0		0	V
Differential Voltage Range		I			±10	V
Open Loop Gain		V		52		dB
Differential Input Resistance		V		2		GΩ
Input Capacitance		V		1.0		pF
Power Supply Sensitivity		V		60		dB
Common Mode Rejection Ratio		I	50	60		dB
	$T_{MIN}<T_A<T_{MAX}$	IV	45	55		dB
Power Dissipation	Dual	I		430	610	mW
Output High Level	ECL 50 Ohms to –2 V	I	–.98		–.70	V
Output Low Level	ECL 50 Ohms to –2 V	I	–1.95		–1.65	V

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, AV_{CC} = +10 V, AV_{EE} = –10.0 V, R_L = 50 Ohm to –2 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL PARAMETERS						
Propagation Delay[1]	50 mV O.D., Slew 10 V/ns	IV	.75	1.25	1.50	ns
Propagation Delay Tempco		V		2		ps/ °C
Propagation Delay Skew (A vs B)		V		100		ps
Delay Dispersion from Input Direction		V		50		ps
Delay Dispersion from Input Common Mode		V		60		ps
Latch Set-up Time		V		500		ps
Latch to Output Delay	50 mV O.D.	V		500		ps
Latch Pulse Width		V		500		ps
Latch Hold Time		V		0		ps
Rise Time	20% to 80%	V		0.45		ns
Fall Time	20% to 80%	V		0.45		ns
Slew Rate		V		5		V/ns

[1]Valid for both high-to-low and low-to-high transitions

TEST LEVEL CODES

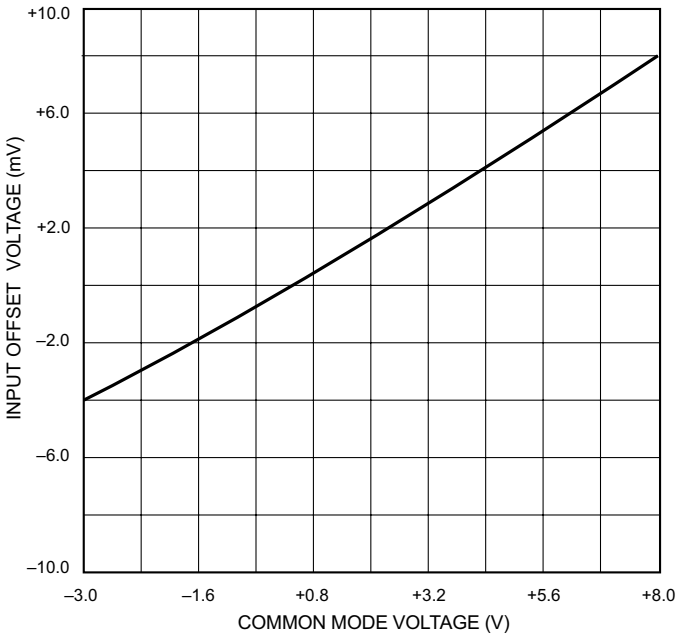
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

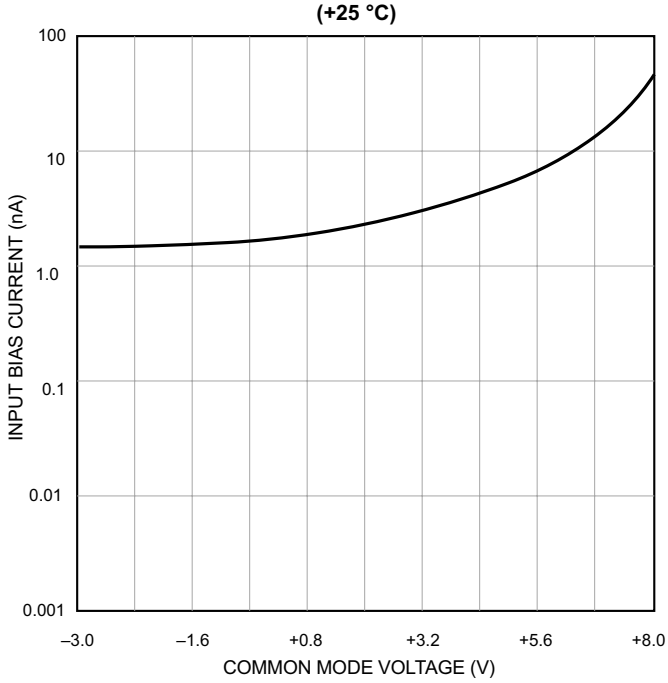
LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

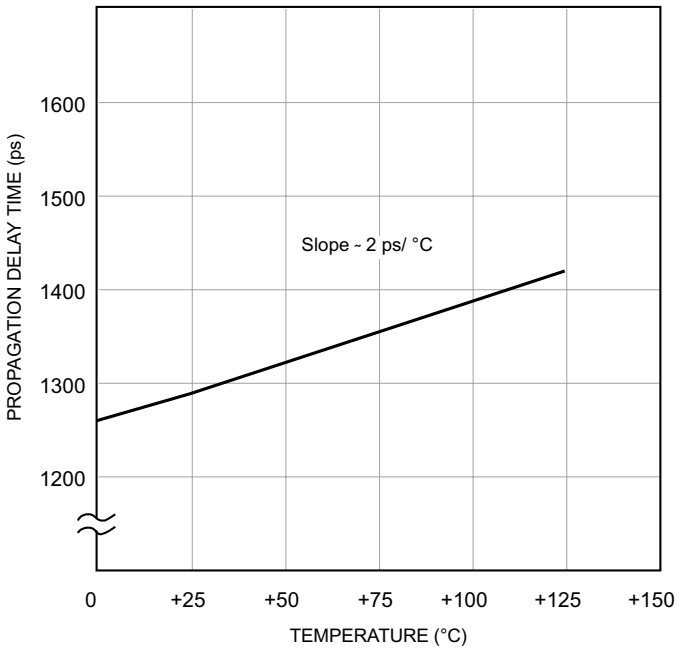
INPUT OFFSET VOLTAGE vs COMMON MODE VOLTAGE (T=+25 °C)



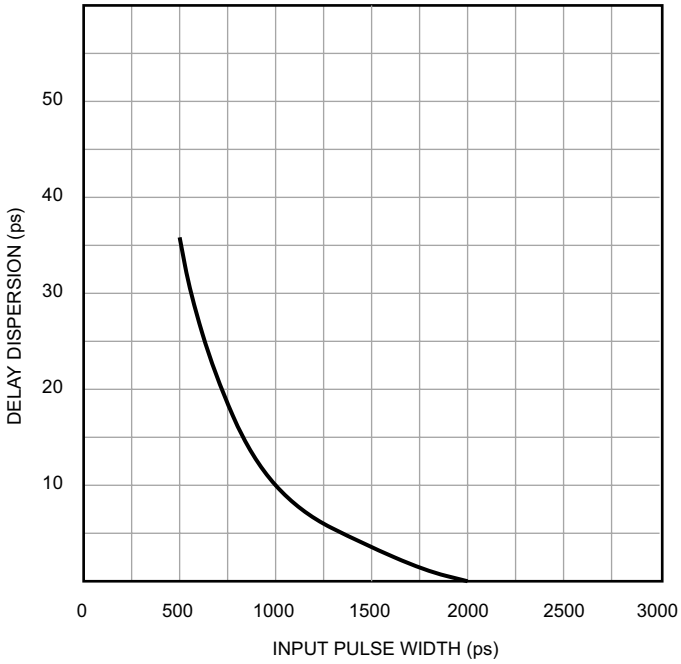
INPUT BIAS CURRENT vs COMMON MODE VOLTAGE (+25 °C)



PROPAGATION DELAY TIME vs TEMPERATURE

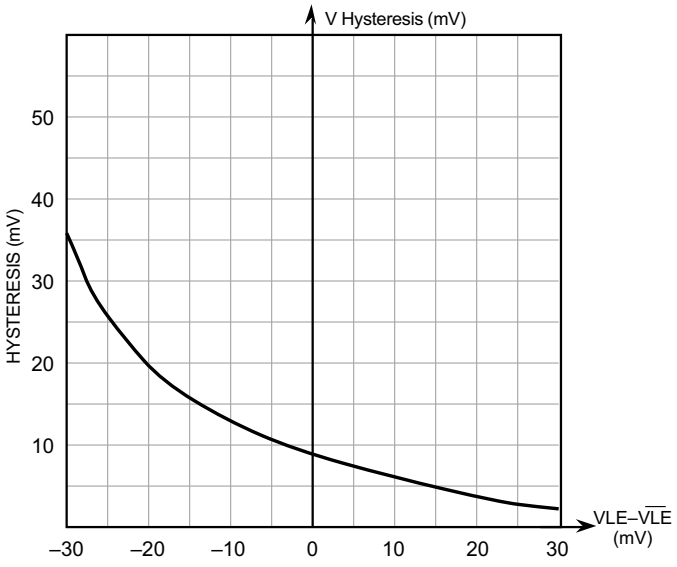


DELAY DISPERSION vs INPUT PULSE WIDTH

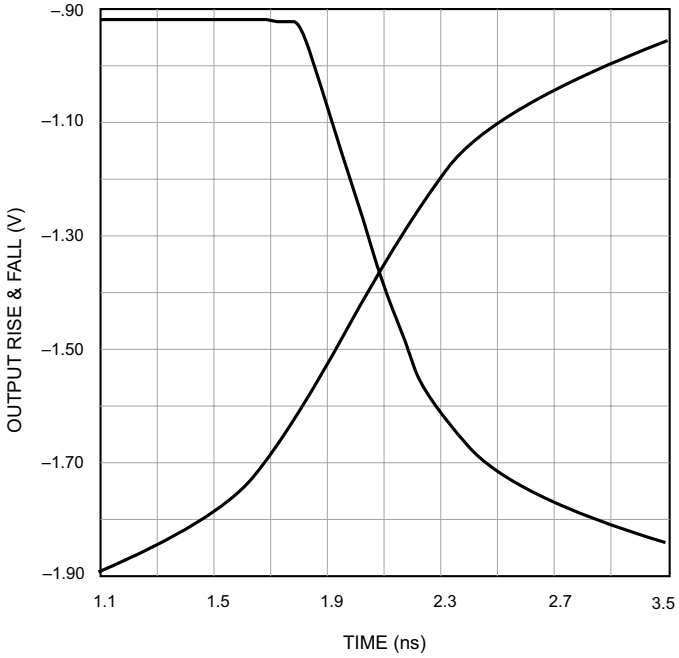


TYPICAL PERFORMANCE CHARACTERISTICS

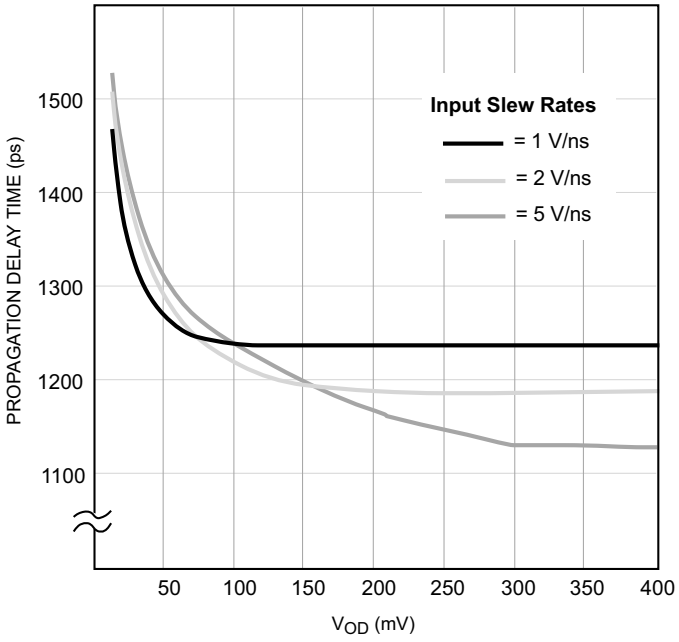
HYSTERESIS vs ∆LATCH VOLTAGE



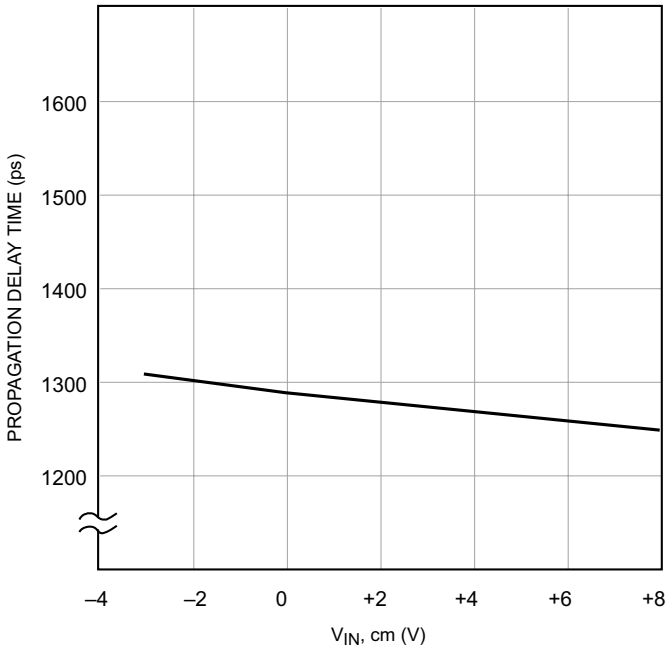
RISE AND FALL OF OUTPUTS vs TIME CROSSOVER



PROPAGATION DELAY vs INPUT OVERDRIVE VOLTAGE



PROPAGATION DELAY vs COMMON MODE INPUT VOLTAGE



GENERAL INFORMATION

The SPT9693 is an ultrahigh-speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9693 has a complementary latch enable control for each comparator. Both should be driven by standard ECL logic levels.

A common mode voltage range of –3 V to +8 V is achieved by a proprietary JFET input design, which requires a separate negative power supply (AV_{EE}).

The dual comparators have separate AV_{CC}, AV_{EE}, and grounds for each comparator to achieve high crosstalk rejection.

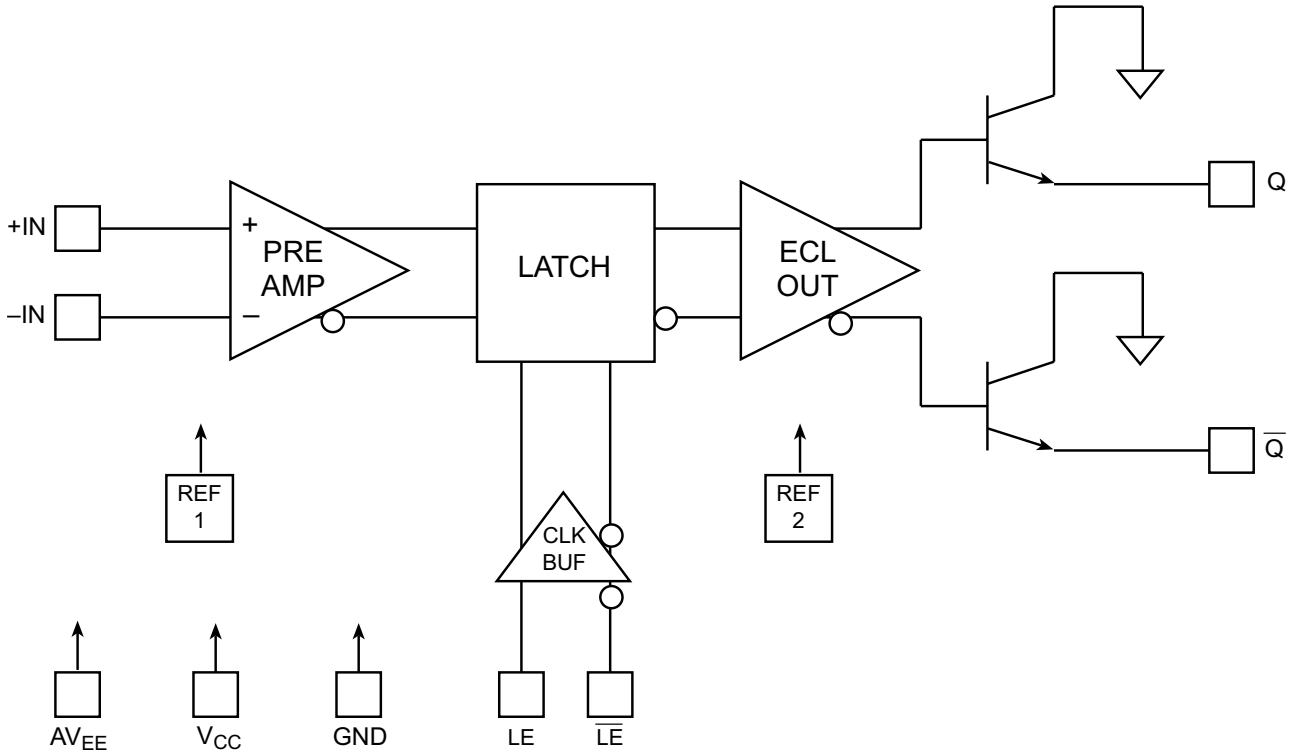
Single-channel operation can be accomplished by floating *all* pins (including the ground and supply pins) of the unused comparator. Power dissipation during single-channel operation is 50% of the dissipation during dual-channel operation.

This comparator offers the following improvements over existing devices:

- Ultra low input bias current and input current offset
- Common mode voltage of –3 to +8 V
- Short propagation delays
- Excellent input and output rejection between comparator channels
- Improved input protection reliability due to JFET input stage design

All of these combined features produce high-performance products with timing stability and repeatability for large system precision.

Figure 1 – Internal Function Diagram



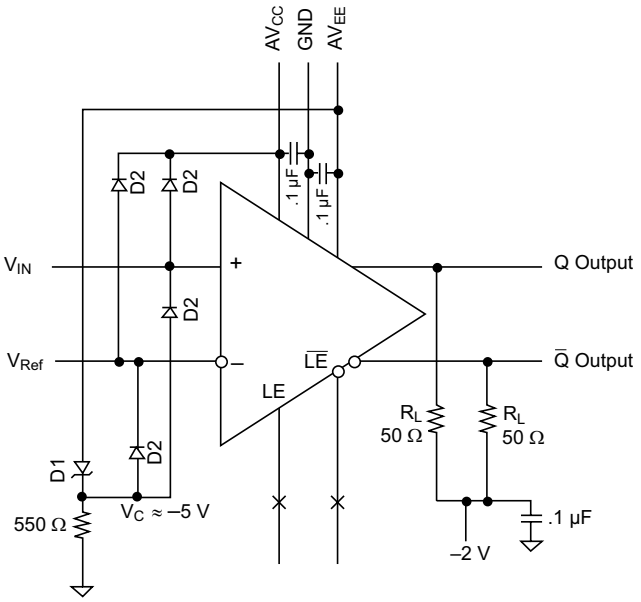
TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 2. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9693 comparator is a very high-frequency and high-gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. All supply voltages should be decoupled with high-frequency capacitors as close to the device as possible. If using the SPT9693 as a single comparator, the outputs of the inactive comparator can be grounded, left open or terminated with 50 ohms to –2 V. All outputs on the active comparator, whether used or unused, should have identical terminations to minimize ground current switching transients.

All ground pins should be connected to the same ground plane to further improve noise immunity and shielding. Unused outputs must be terminated with 50 ohms to ground.

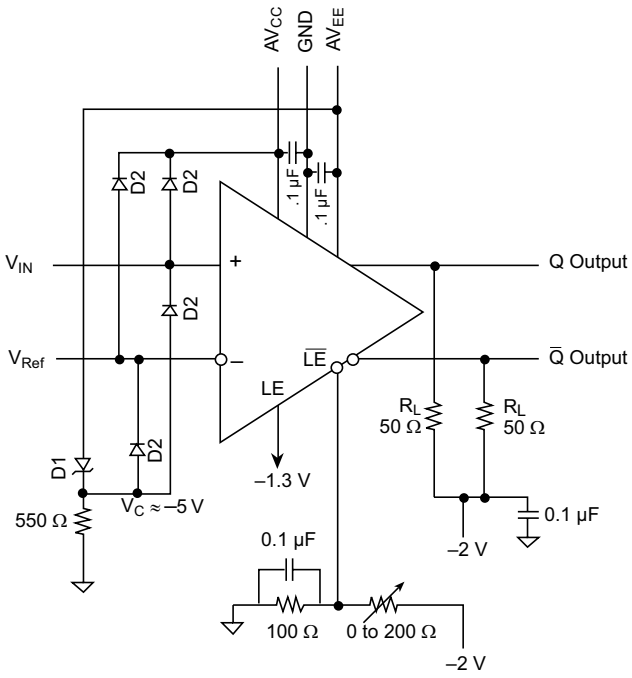
Figure 2 – SPT9693 Typical Interface Circuit



Notes:

1) D1 = 1N5231B or 1N751 or equivalent.
2) D2 = 1N914 or equivalent.
3) At no time should *both* inputs be allowed to float with power applied to the device. At least one of the inputs should be tied to a voltage within the common mode range (–3.0 to +8.0 V) to prevent possible damage to the device. Additional protection diodes D2 should be used on the inputs if there is the possibility of exceeding the absolute maximum ratings.

Figure 3 – SPT9693 Typical Interface Circuit with Hysteresis



Notes:

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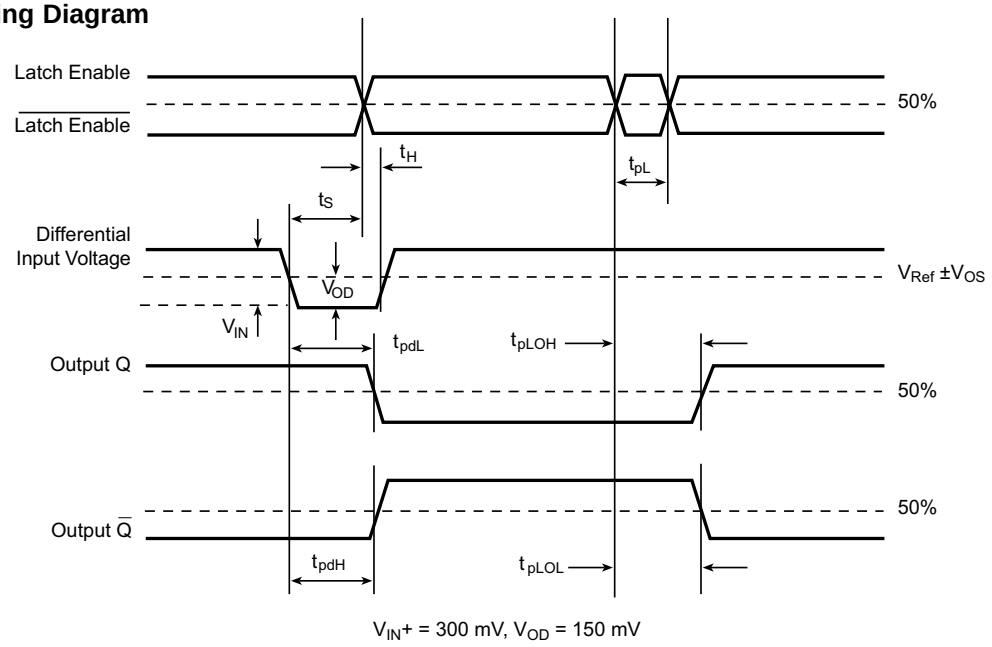
TIMING INFORMATION

The timing diagram for the comparator is shown in figure 4. If LE is high and $\overline{LE}$ low in the SPT9693, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of a 150 mV overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

Figure 4 – Timing Diagram



V_{IN}+ = 300 mV, V_{OD} = 150 mV

SWITCHING TERMS (Refer to figure 4)

t_{pdH} INPUT TO OUTPUT HIGH DELAY – The propagation delay measured from the time the input signal reaches the reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY – The propagation delay measured from the time the input signal reaches the reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME – The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

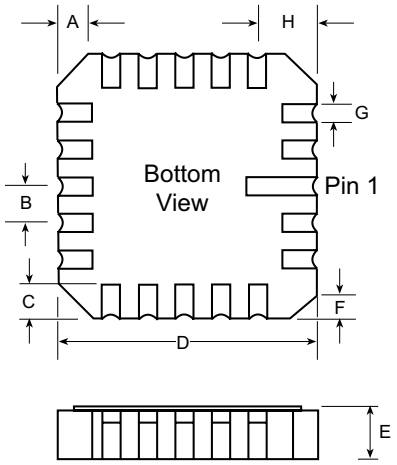
t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME – The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

V_{OD} VOLTAGE OVERDRIVE – The difference between the differential input and reference input voltages.

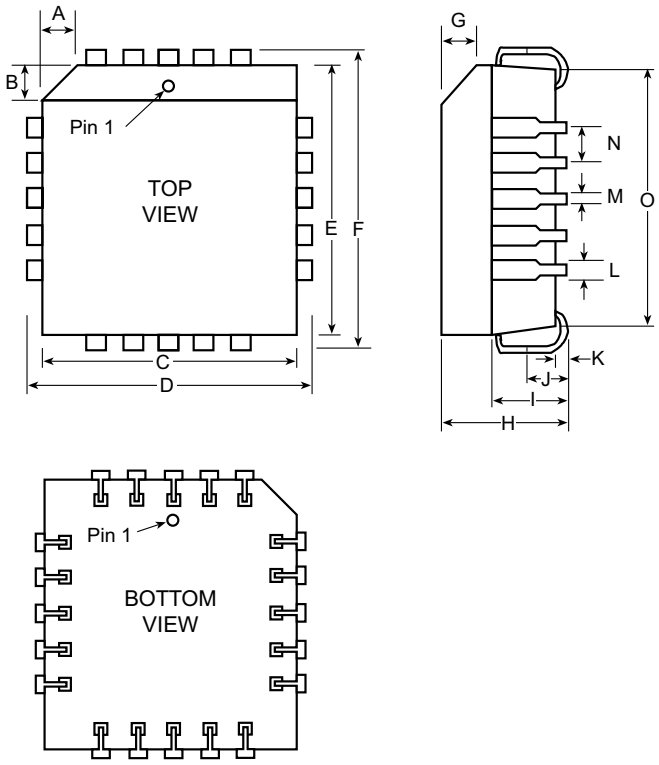
PACKAGE OUTLINES

20-Contact Leadless Chip Carrier (LCC)



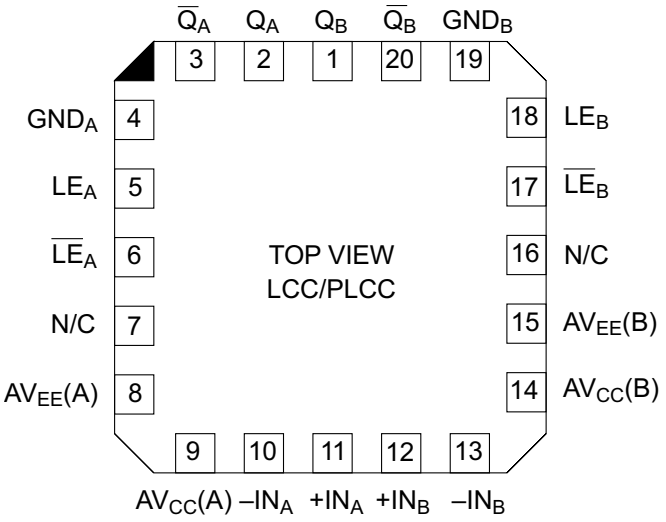
	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	.040 typ		1.02 typ	
B	.050 typ		1.27 typ	
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F	.020 typ		0.51 typ	
G	0.022	0.028	0.56	0.71
H		0.075		1.91

20-Lead Plastic Leadless Chip Carrier (PLCC)



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	.045 typ		1.14 typ	
B	.045 typ		1.14 typ	
C	0.350	0.356	8.89	9.04
D	0.385	0.395	9.78	10.03
E	0.350	0.356	8.89	9.04
F	0.385	0.395	9.78	10.03
G	0.042	0.056	1.07	1.42
H	0.165	0.180	4.19	4.57
I	0.085	0.110	2.16	2.79
J	0.025	0.040	0.64	1.02
K	0.015	0.025	0.38	0.64
L	0.026	0.032	0.66	0.81
M	0.013	0.021	0.33	0.53
N		0.050		1.27
O	0.290	0.330	7.37	8.38

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
$\overline{LE}_A$	Inverted Latch Enable A
LE_A	Latch Enable A
$AV_{CC}(A)$	Positive Supply Voltage (+10 V)
$AV_{EE}(A)$	Negative Supply Voltage (–10 V)
$AV_{CC}(B)$	Positive Supply Voltage (+10 V)
$AV_{EE}(B)$	Negative Supply Voltage (–10 V)
$-IN_A$	Inverting Input A
$+IN_A$	Noninverting Input A
$+IN_B$	Noninverting Input B
$-IN_B$	Inverting Input B
$\overline{LE}_B$	Inverted Latch Enabled B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B
N/C	Not Connected

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT9693SCC	0 to +70 °C	LCC
SPT9693SCP	0 to +70 °C	PLCC
SPT9693SCU	+25 °C	Die*

*Please see the die specification for guaranteed electrical performance.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.