

FEATURES

- Second Source of AD9101
- 350 MHz Sampling Bandwidth
- 125 MHz Sampling Rate
- Excellent Hold Mode Distortion
 - 75 dB at 50 MSPS (23 MHz V_{IN})
 - 62 dB at 100 MSPS (48 MHz V_{IN})
- 7 ns Acquisition Time to 0.1%
- <1 ps Aperture Jitter
- 66 dB Feedthrough Rejection at 50 MHz
- Low Spectral Noise Density

GENERAL DESCRIPTION

The SPT9101 is a high-speed track-and-hold amplifier designed for a wide range of use. The SPT9101 is capable of sampling at speeds up to 125 MSPS with resolutions ranging from 8 to 12 bits. Trim programmable internal hold and compensation capacitors provide for optimized input bandwidth and slew rate versus noise performance.

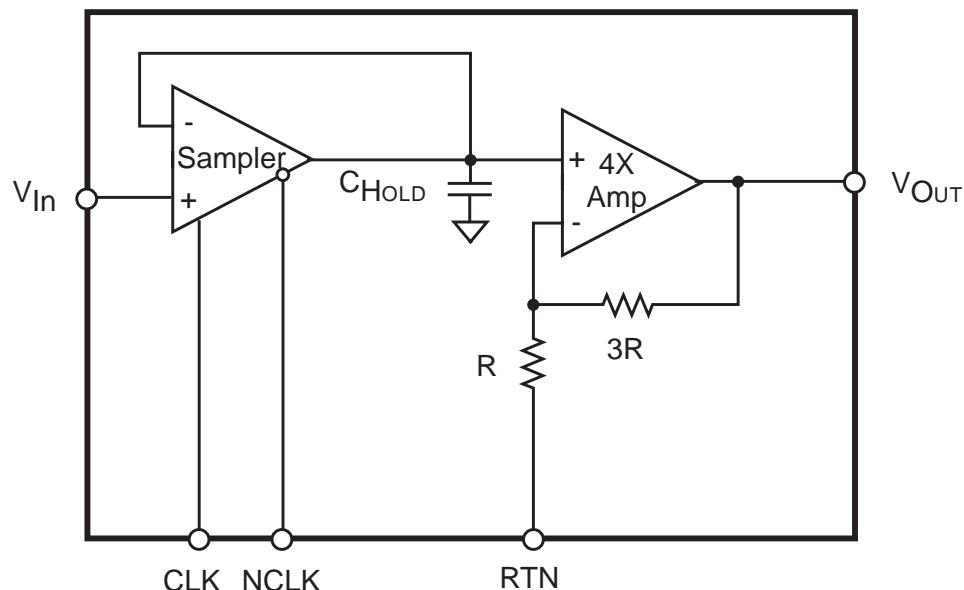
APPLICATIONS

- Test Instrumentation Equipment
- RF Demodulation Systems
- High Performance CCD Capture
- Digital Sampling Oscilloscopes
- Commercial and Military Radar
- High-Speed DAC Deglitching

The performance of this device makes it an excellent front end driver for a wide range of ADCs on the market today. Significant improvements in dynamic performance can be achieved by using this device ahead of virtually all ADCs that do not have an internal track-and-hold.

The SPT9101 is offered in 20-lead SOIC and LCC packages over the industrial temperature range and in die form. Contact the factory for military and /833 package options.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)¹

Supply Voltages

Supply Voltage (+V_S) -0.5 V to +6 V
Supply Voltage (-V_S) -6 V to +0.5 V

Input Voltages

Analog Input Voltage ±5 V
CLK, NCLK Input -5 V to +0.5 V

Output Currents

Continuous Output Current 70 mA

Temperature

Operating Temperature -40 to +85 °C
Junction Temperature +150 °C
Lead, Soldering (10 seconds) +220 °C
Storage -65 to +150 °C

Note 1: Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical application.

ELECTRICAL SPECIFICATIONS

+V_S=+5.0 V, -V_S=-5.2 V, R_{LOAD}=100 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9101			UNITS
			MIN	TYP	MAX	
DC Performance						
Gain $\Delta V_{IN} = 0.5\text{ V}$	+25 °C	I	3.93	4.0	4.07	V/V
	Full Temp.	VI	3.9		4.1	V/V
Offset $\Delta V_{IN} = 0\text{ V}$	+25 °C	I		±3	±10	mV
	Full Temp.	VI			±30	mV
Output Resistance	+25 °C	V		0.5		Ω
Output Short Circuit Current	Full Temp.	V		±60		mA
PSRR $\Delta V_S = 0.5\text{ V p-p}$	+25 °C	VI	37	43		dB
Pedestal Sensitivity to Pos. Supply $\Delta V_S = 0.5\text{ V p-p}$	Full Temp.	V		4		mV/V
Pedestal Sensitivity to Neg. Supply $\Delta V_S = 0.5\text{ V p-p}$	Full Temp.	V		8		mV/V
Analog Input/Output						
Maximum Output Voltage Range ⁶	Full Temp.	VI	±2.4	±2.7		V
Input Bias Current	+25 °C	I		±15	±30	μA
	Full Temp.	VI			±35	μA
Input Capacitance	+25 °C	V		2		pF
Input Resistance	Full Temp.	VI	100	450		kΩ
Clock Inputs						
Input Bias Current	+25 °C	VI		3	30	μA
Input Low Voltage	Full Temp.	VI		-1.8	-1.5	V
Input High Voltage	Full Temp.	VI	-1.0	-0.8		V
Track Mode Dynamics						
Bandwidth (-3 dB) $V_{Out} = 1.0\text{ V p-p}$	Full Temp.	IV	150	180		MHz
Slew Rate 4 V Output Step	Full Temp.	IV	1100	1400		V/μs
Overdrive Recovery Time ¹	To 0.1%	V		55		ns
Integrated Output Noise	BW = 5 to 200 MHz	V		270		μV
Input RMS Spectral Noise	10 MHz	V		3.9		nV/√Hz

ELECTRICAL SPECIFICATIONS

+V_S=+5.0 V, -V_S=-5.2 V, R_{LOAD}=100 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9101			UNITS
			MIN	TYP	MAX	
Hold Mode Dynamics						
Worst Harmonic V _{Out} = 2 V p-p	23 MHz, 50 MSPS +25 °C	V		-75		dB FS
Worst Harmonic V _{Out} = 2 V p-p	48 MHz, 100 MSPS +25 °C	IV		-62	-57	dB FS
Worst Harmonic V _{Out} = 2 V p-p	48 MHz, 100 MSPS Full Temp.	IV			-53	dB FS
Worst Harmonic V _{Out} = 2 V p-p	48 MHz, 125 MSPS +25 °C	V		-57		dB FS
Sampling Bandwidth ² V _{IN} = 0.5 V p-p	-3 dB, +25 °C	V		350		MHz
Hold Noise ³ (RMS)	+25 °C	V		150 x t _H		mV/s
Droop Rate	V _{IN} =0.0 V, +25 °C	V		-40		mV/μs
Feedthrough Rejection (50 MHz) V _{Out} = 2 V p-p	Full Temp.	V		-66		dB
Maximum Hold Time, V _{IN} =0 V	Full Temp.	IV	100	200		ns
Track-and-Hold Switching						
Aperture Delay	+25 °C	V		-250		ps
Aperture Jitter	+25 °C	V		<1		ps rms
Pedestal Offset, V _{IN} =0 V	+25 °C	I		±10	±25	mV
	Full Temp.	VI			±35	mV
Transient Amplitude	V _{IN} = 0 V, Full Temp.	V		8		mV
Settling Time to 4 mV	Full Temp.	V		4		ns
Glitch Product ⁴ V _{IN} = 0 V	+25 °C	V		20		pV-s
Hold-to-Track Switching						
Acquisition Time to 0.1% 2 V Output Step	+25 °C	V		7		ns
Acquisition Time to 0.01% 2 V Output Step	+25 °C	IV		11	14	ns
	Full Temp.	IV			16	ns
Power Supply ⁵						
+V _S Voltage	Full Temp, Track Mode	VI		54	65	mA
	Full Temp, Clocked Mode	VI		44	55	mA
-V _S Voltage	Full Temp, Track Mode	VI		54	65	mA
	Full Temp, Clocked Mode	VI		44	55	mA
Power Dissipation	Full Temp, Track Mode	VI		551	663	mW
	Full Temp, Clocked Mode	VI		449	561	mW

¹Time to recover within rated error band from 160% overdrive.

²Sampling bandwidth is defined as the -3 dB frequency response of the input sampler to the hold capacitor when operating in the sampling mode. It is greater than tracking bandwidth because it does not include the bandwidth of the output amplifier.

³Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 3 μV (150 mV/s x 20 ns). This value must be combined with the track mode noise to obtain total noise.

⁴Total energy of worst case track-to-hold or hold-to-track glitch.

Typical thermal impedances: Θ_{JC} (LCC) = +6 °C/W

Θ_{JA} (SOIC) = +85 °C/W in still air at +25 °C ambient.

⁵Clocked mode is specified with a 50% clock duty cycle.

⁶Analog input voltage should be limited ≤0.8 volts to maintain device in linear range.

TEST LEVEL CODES

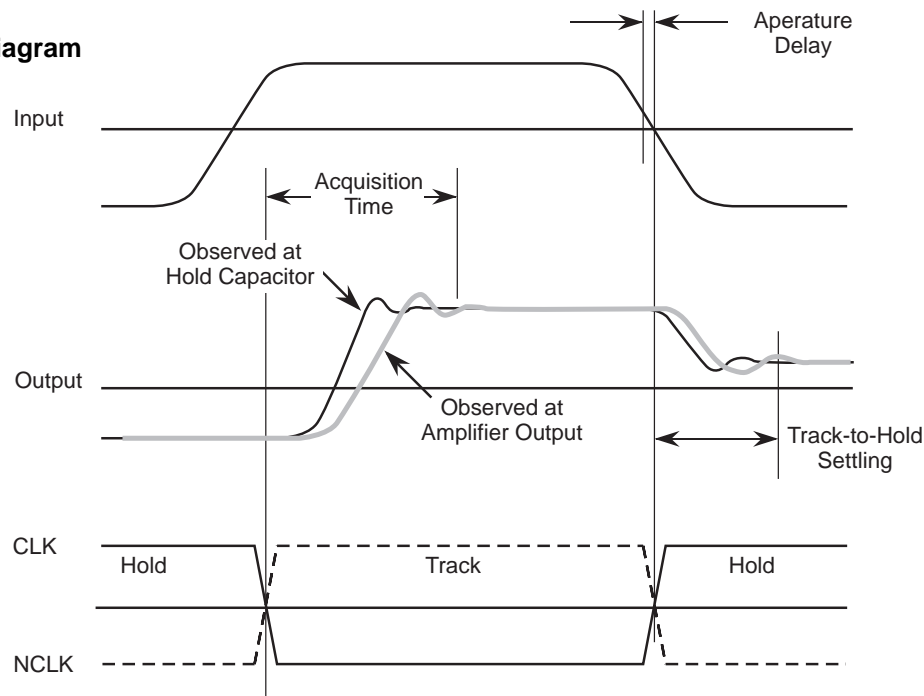
All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL

TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at T _A =25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T _A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



TIMING SPECIFICATION DEFINITIONS

ACQUISITION TIME

This is the time it takes the SPT9101 to acquire the analog signal at the internal hold capacitor when it makes a transition from hold mode to track mode. (See figure 1.) The acquisition time is measured from the 50% input clock transition point to the point when the signal is within a specified error band at the internal hold capacitor (ahead of the output amplifier). It does not include the delay and settling time of the output amplifier. Because the signal is internally acquired and settled at the hold capacitor before the output voltage has settled, the sampler can be put in hold mode before the output has settled.

TRACK-TO-HOLD SETTLING TIME

The time required for the output to settle to within 4 mV of its final value.

APERTURE DELAY

The aperture delay time is the interval between the leading edge transition of the clock input and the instant when the input signal was equal to the held value. It is the difference in time between the digital hold switch delay and the analog signal propagation time. Because the analog propagation time is longer than the digital delay in the SPT9101, the aperture delay is a negative value.

The schematic diagram illustrates the electrical connections for the SPT9101 and SPT, HCMP96850 components. The SPT9101 is a central integrated circuit with pins 1 through 18. It is powered by a -5.2V supply (labeled -A5.2) and a +5V supply (labeled +A5). The input signal V_{IN} is connected to pin 15, and the output signal V_{OUT} is connected to pin 18. The SPT9101 has four pins labeled $-VS$ (pins 12, 13, 17, 18) and four pins labeled $+VS$ (pins 4, 5, 8, 9). The SPT, HCMP96850 is a triangular component with pins 1 through 16. It is powered by a +5V supply (labeled +A5) and a -5.2V supply (labeled -A5.2). The input signal $CLK\ IN$ is connected to pin 3. The output signal V_{OUT} is connected to pin 12. The SPT, HCMP96850 has pins labeled V_{CC} (pin 8), V_{EE} (pin 11), GND (pin 12), and LE (pin 6). The circuit also includes various passive components: a 2.2 μF capacitor connected to the -A5.2 supply, a 330 Ω resistor connected to the +A5 supply, and a 220 Ω resistor connected to the -A5.2 supply. The SPT9101 has pins labeled RTN (pin 1,2), CLK (pin 10), $NCLK$ (pin 11), and GND (pins 6,7,16).

b) ECL: Direct Input

The RTN pin may be tied to an external voltage to generate an offset at the output. V_{Out} must be kept to less than ± 2.7 V typical output swing. V_{Out} , with an external reference voltage at the RTN pin, is represented by the following formula:

$$V_{Out} = 4 V_{IN} - 3 V_{Ref}$$

where V_{Ref} = voltage at RTN pin and $|V_{Out}| \leq 2.7$ V

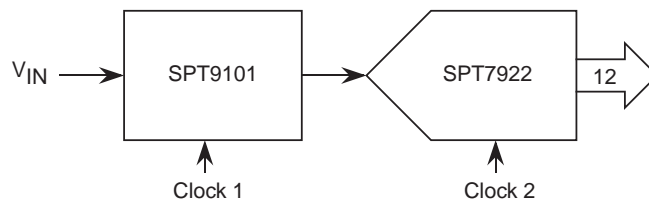
The following options are generally not recommended due to the possibility of degraded noise performance of the device: the RTN pin can also be tied to an external resistor to reduce the gain but performance may degrade due to increased noise from the external resistor. Also RTN can be left open for unity gain mode, however, noise will increase.

In all cases, V_{IN} must be kept to $-0.5 \text{ V} \leq V_{IN} \leq +0.5 \text{ V}$ for rated performance.

SAMPLER FOR 12-BIT ADC APPLICATION

The SPT9101 was specifically designed for applications where improved bandwidth performance is required. Figure 3 shows a simple block diagram of the SPT9101 as a sampler ahead of the SPT7922 12-bit, 30 MSPS ADC.

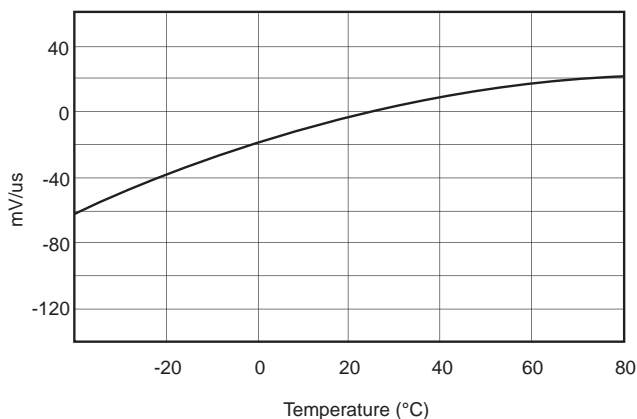
Figure 3 - Sampler for 12-Bit ADC



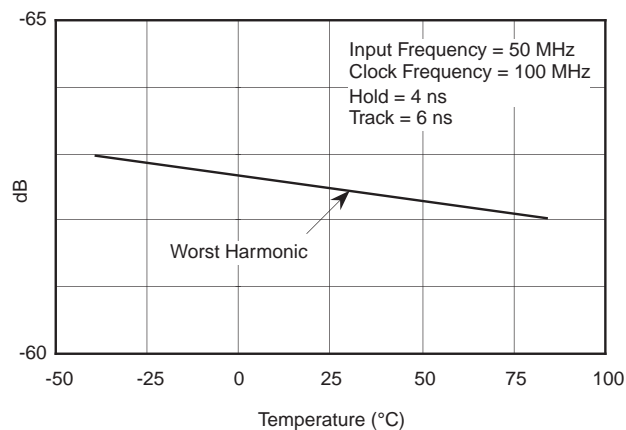
The graph below entitled Improved Dynamic Performance Using the SPT9101 shows the performance with and without the SPT9101. The SPT9101 significantly extends the dynamic performance range of the converter.

PERFORMANCE CHARACTERISTICS

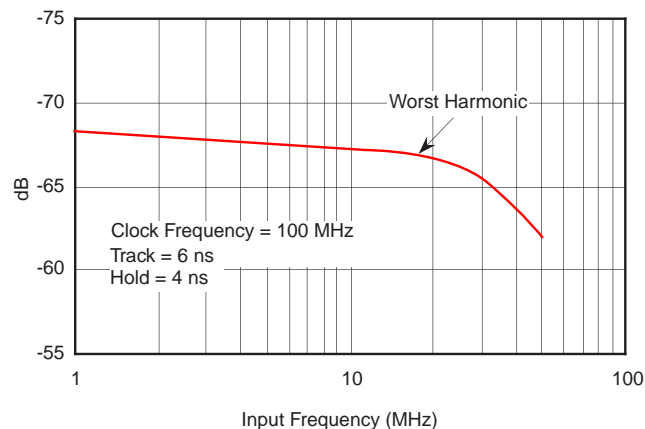
Droop Rate vs Temperature



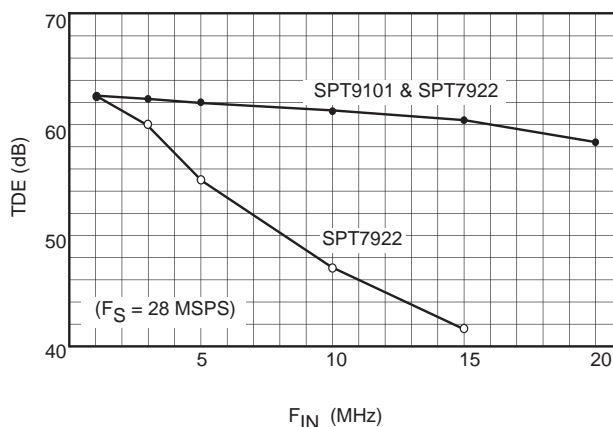
SPT9101 Hold Mode Distortion vs. Temperature



SPT9101 Hold Mode Distortion vs Input Frequency

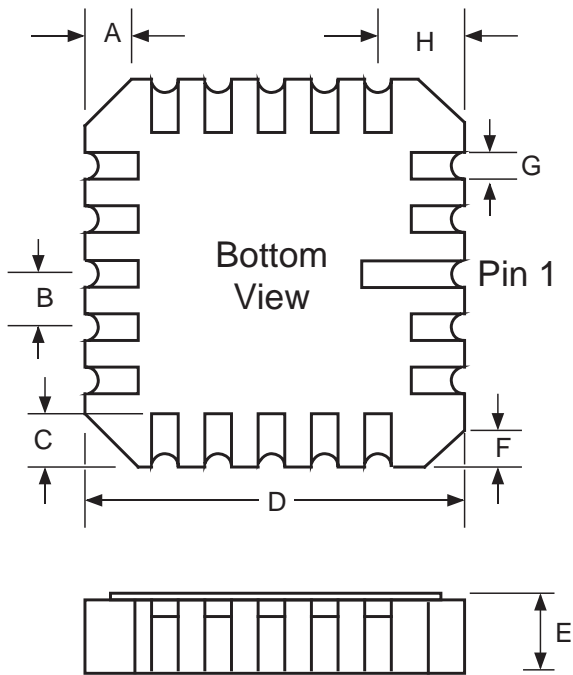


Improved Dynamic Performance Using the SPT9101



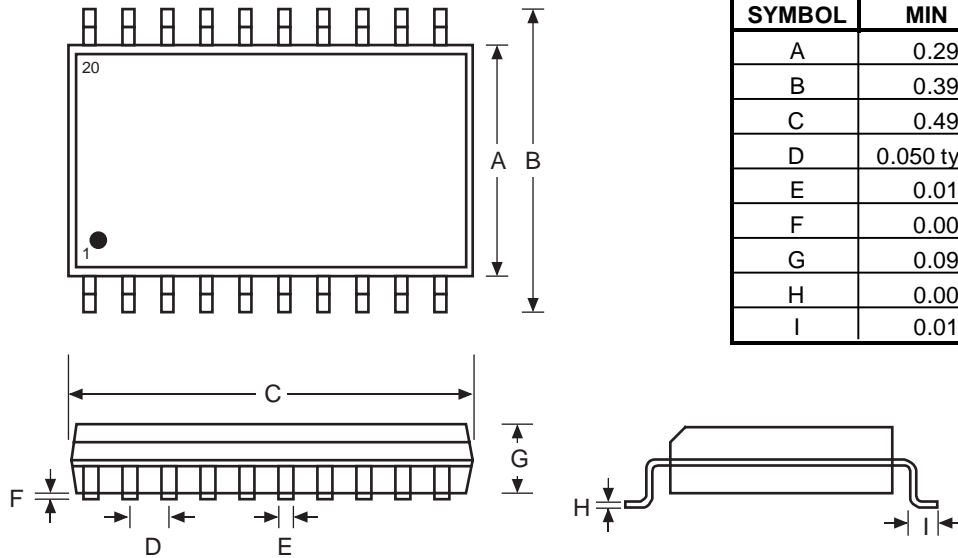
PACKAGE OUTLINES

20-Lead LCC



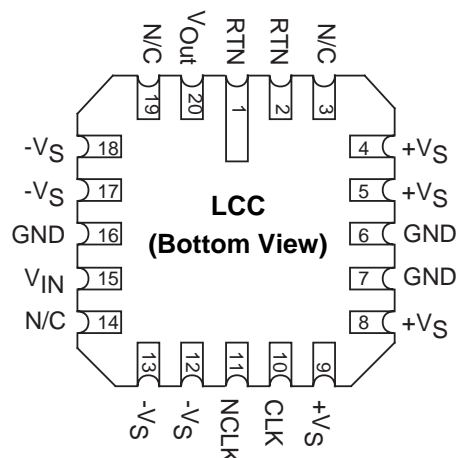
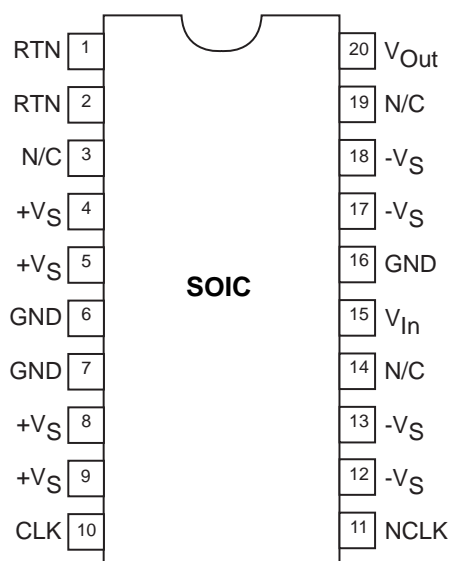
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 typ		1.02
B		.050 typ		1.27
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F		.020 typ		0.51
G	0.022	0.028	0.56	0.71
H		0.075		1.91

20-Lead SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.291	0.299	7.40	7.60
B	0.394	0.419	10.00	10.65
C	0.496	0.512	12.60	13.00
D	0.050 typ		1.27 typ	
E	0.014	0.019	0.35	0.49
F	0.004	0.012	0.10	0.30
G	0.093	0.104	2.35	2.65
H	0.009	0.013	0.23	0.32
I	0.016	0.050	0.40	1.27

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	I/O	Function
RTN	I	Gain Set Resistor Return
+V _S	I	+5 V Power Supply
GND	I	Ground
CLK	I	True ECL T/H Clock
NCLK	I	Complement ECL T/H Clock
-V _S	I	-5.2 V Power Supply
N/C	-	No Connection
V _{IN}	I	Analog Signal Input
V _{OUT}	O	Analog Signal Output

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE
SPT9101SIS	20L SOIC	-40 to +85 °C
SPT9101SIC	20L LCC	-40 to +85 °C
SPT9101SCU	Die*	+25 °C

*Please see die specification for guaranteed electrical performance.

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