DATA SHEET

SA57005

Multiple output low noise, low dropout linear regulator

Product data

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Philips
Semiconductors

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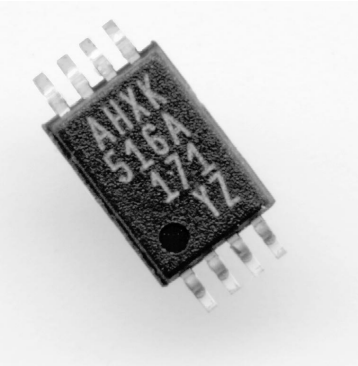
Multiple output low noise, low dropout linear regulator SA57005

GENERAL DESCRIPTION

The SA57005 is a very low dropout, low noise composite voltage regulator with three fixed independent outputs. The output voltages are preset to 2.5 V, 2.8 V and 3.0 V having a common input voltage pin V_{IN}. Two ON/OFF switches allow V_{o1} and V_{o2}/V_{o3} to be turned off when not needed, thus conserving power. Also, three regulators in one package save board space, which is critical in microprocessor systems.

Designed for battery-powered and portable applications the SA57005 achieves unequalled performance in all specifications such as low supply-current, low dropout voltage, low power consumption, small size, fast dynamic response to line and load, precision output and so on. Each of these regulators consists of an internal voltage reference, an error amplifier, resistors, and control switch. The SA57005 is housed in a VSOP-8A 8-lead package.



FEATURES

- Very low dropout voltage: V_{o1}: 0.25 V typ.; V_{o2}: 0.28 V typ.; V_{o3}: 0.30 V typ.
- Low noise: 60 μV_{rms} typ. (f = 10 Hz to 10 kHz; I_O = 30 mA)
- High precision output voltage: ±3%
- Output current capacity: I_{o1} and I_{o2} = 100 mA max; I_{o3} = 150 mA max.
- Low consumption current: I_{IN1} = 250 µA typ., I_{IN2}/I_{IN3} = 500 µA typ. (when not loaded), 3 µA max. (when off)
- Line regulation: 1%/V typ. (I_{OUT} = 30 mA; V_{IN} = 4.0 to 8.0 V)
- Load regulation: 30 mV typ. for I_{OUT} = 0 to 70 mA
- Low temperature drift co-efficient to V_{OUT}: ±100 ppm/°C
- Thermal shutdown
- Wide operating temperature range: –20 °C to +75 °C

APPLICATIONS

- Cellular phones, cordless phones and 2-way radios
- Electronic notebooks, PDAs and Palmtop computers
- Cameras, VCRs and camcorders
- Modems
- Battery-powered or hand-held instruments

SIMPLIFIED DEVICE DIAGRAM

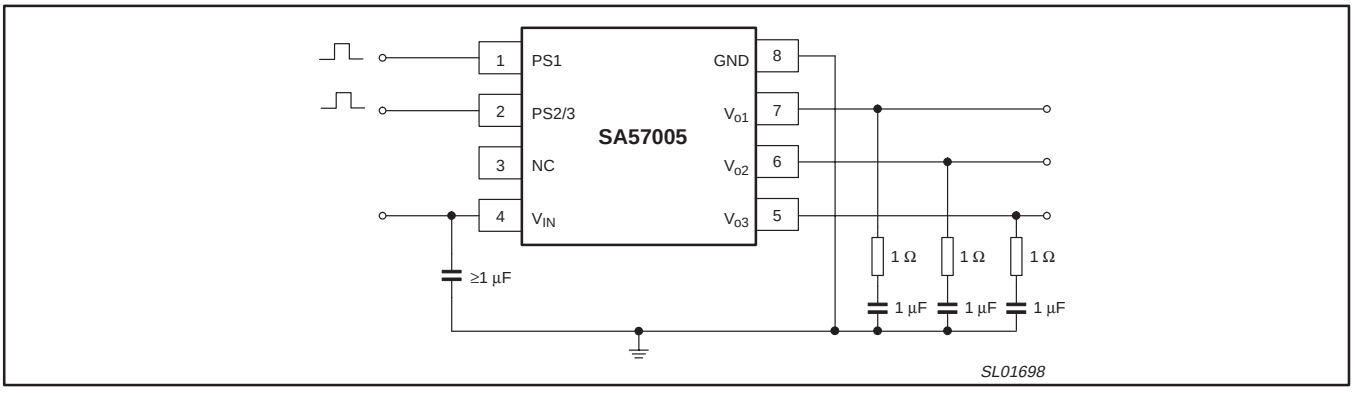


Figure 1. Simplified device diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	TEMPERATURE RANGE
SA57005DH	VSOP-8A	8-pin surface mount small outline package	–20 to +75 °C

Part number marking

Each device is marked with a four letter code on the first line. The first three letters designate the product. The fourth letter, represented by 'x' is a date tracking code. Any other lines contain manufacturing codes.

Part Number	Marking
SA57005DH	AHXx

PIN CONFIGURATION

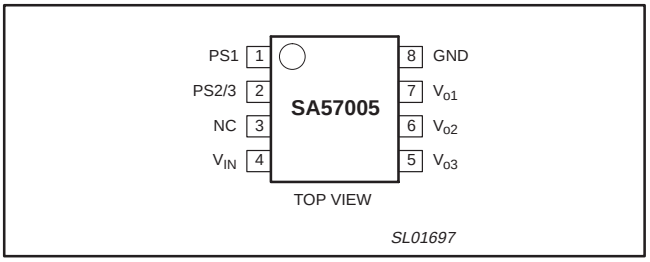


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	PS1	ON/OFF control for V_{o1}; tie to V_{IN} if ON/OFF function is not used.
2	PS2/3	ON/OFF control for V_{o2} and V_{o3}; tie to V_{IN} if ON/OFF function is not used.
3	NC	No connection
4	V_{IN}	Input voltage
5	V_{o3}	Regulated output 3
6	V_{o2}	Regulated output 2
7	V_{o1}	Regulated output 1
8	GND	Ground

MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	UNIT
V_{IN}	Supply voltage		–0.3	+12	V
I_{O1}, I_{O2}	Output current 1, 2		–	100	mA
I_{O3}	Output current 3		–	150	mA
T_{opr}	Operating ambient temperature range		–20	+75	°C
T_{stg}	Storage temperature		–40	+125	°C
P_D	Power dissipation	unmounted	–	300	mW
		when mounted on glass epoxy board ($40 \times 40 \times 1.6$ mm)	–	500	mW

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C; V_{IN} = 4 V; C_{IN} = 2.2 µF; $C_{VO(n)}$ = 2.2 µF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
$I_{IN(OFF)}$	Supply current (OFF)	$V_{PS1} = V_{PS2/3} = 0$ V	–	0	3	µA
I_{IN1}, I_{IN2}, I_{IN3}	Supply current 1, 2, 3	no load				
	I_{IN1}	V_{PS1} = 3 V; $V_{PS2/3}$ = 0 V	–	250	370	µA
	I_{IN2}, I_{IN3}	$V_{PS2/3}$ = 3 V; V_{PS1} = 0 V	–	500	740	µA
V_{o1}						
V_{o1}	Output voltage	I_{O1} = 30 mA	2.42	2.50	2.58	V
$V_{io(dif)(min)1}$	Input/output differential voltage	V_{IN} = 2.3 V; I_{O1} = 30 mA	–	0.1	0.25	V
ΔV_{LO1}	Load regulation	I_{O1} = 0 to 70 mA	–	30	60	mV
ΔV_{LI1}	Line regulation	V_{IN} = 4.0 V to 8.0 V; I_{O1} = 30 mA	–	10	25	mV
$\Delta V_{o1}/\Delta T$	V_O temperature coefficient (Note 1)	T_{amb} = –20 °C to +75 °C; I_{O1} = 30 mA	–	±100	–	ppm/°C
RR1	Ripple rejection (Note 1)	f = 120 Hz; V_{ripple} = 1 V_{p-p}; I_{O1} = 30 mA	50	60	–	dB
V_{n1}	Output noise voltage (Note 1)	f = 10 Hz to 10 kHz; I_{O1} = 30 mA	–	60	90	μV_{rms}
t_{DH1}	Output delay time (Note 1)	I_{O1} = 30 mA; V_{PS1} = 0 V → 4 V; $V_{PS2/3}$ = 0 V	–	0.04	0.15	ms
V_{o2}						
V_{o2}	Output voltage	I_{O2} = 30 mA	2.72	2.80	2.88	V
$V_{io(dif)(min)2}$	Input/output differential voltage	V_{IN} = 2.6 V; I_{O2} = 30 mA	–	0.1	0.25	V
ΔV_{LO2}	Load regulation	I_{O2} = 0 to 70 mA	–	30	60	mV
ΔV_{LI2}	Line regulation	V_{IN} = 4.0 V to 8.0 V; I_{O2} = 30 mA	–	10	25	mV
$\Delta V_{o2}/\Delta T$	V_O temperature coefficient (Note 1)	T_{amb} = –20 °C to +75 °C; I_{O2} = 30 mA	–	±100	–	ppm/°C
RR2	Ripple rejection (Note 1)	f = 120 Hz; V_{ripple} = 1 V_{p-p}; I_{O2} = 30 mA	50	60	–	dB
V_{n2}	Output noise voltage (Note 1)	f = 10 Hz to 10 kHz; I_{O2} = 30 mA	–	60	90	μV_{rms}
t_{DH2}	Output delay time (Note 1)	I_{O2} = 30 mA; $V_{PS2/3}$ = 0 V → 4 V; V_{PS1} = 0 V	–	0.04	0.15	ms
V_{o3}						
V_{o3}	Output voltage	I_{O3} = 80 mA	2.92	3.00	3.08	V
$V_{io(dif)(min)3}$	Input/output differential voltage	V_{IN} = 2.8 V; I_{O3} = 80 mA	–	0.15	0.30	V
ΔV_{LO3}	Load regulation	I_{O3} = 0 to 100 mA	–	30	60	mV
ΔV_{LI3}	Line regulation	V_{IN} = 4.0 V to 8.0 V; I_{O3} = 30 mA	–	10	25	mV
$\Delta V_{o3}/\Delta T$	V_O temperature coefficient (Note 1)	T_{amb} = –20 °C to +75 °C; I_{O3} = 30 mA	–	±100	–	ppm/°C
RR3	Ripple rejection (Note 1)	f = 120 Hz; V_{ripple} = 1 V_{p-p}; I_{O3} = 30 mA	50	60	–	dB
V_{n3}	Output noise voltage (Note 1)	f = 10 Hz to 10 kHz; I_{O3} = 30 mA	–	60	90	μV_{rms}
t_{DH3}	Output delay time (Note 1)	I_{O3} = 30 mA; $V_{PS2/3}$ = 0 V → 4 V	–	0.04	0.15	ms
PS output control pin						
V_{OFF}	LOW-level threshold voltage		–	–	0.4	V
V_{ON}	HIGH-level threshold voltage		1.6	–	–	V
I_{PS1}	PS1 terminal current	V_{PS1} = 1.6 V	–	–	8	µA
$I_{PS2/3}$	PS2/3 terminal current	$V_{PS2/3}$ = 1.6 V	–	–	16	µA

NOTE:
1. Guaranteed by design.

TYPICAL PERFORMANCE CURVES

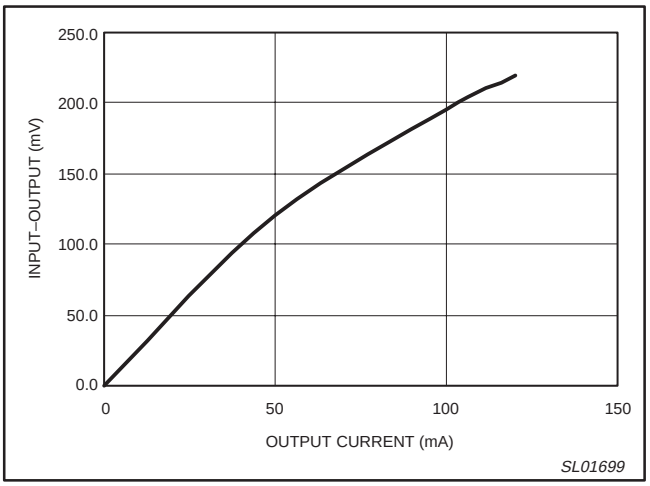


Figure 3. Input-output differential voltage.

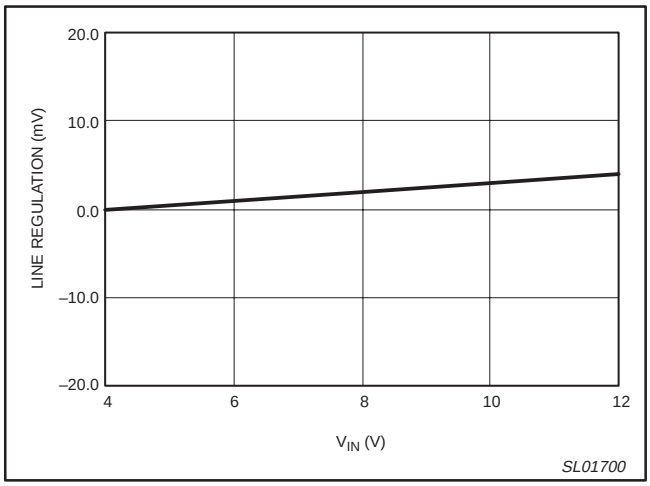


Figure 4. Line regulation.

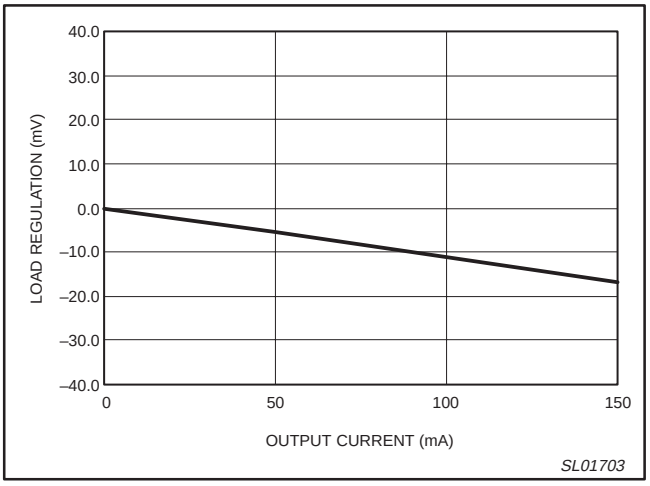


Figure 5. Load regulation.

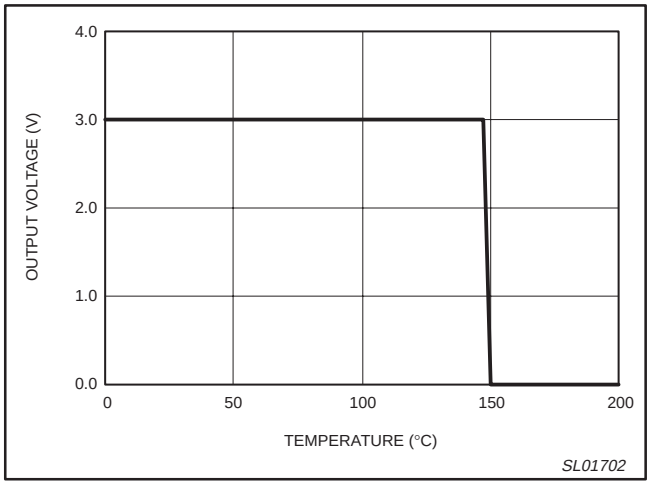


Figure 6. Thermal shutdown.

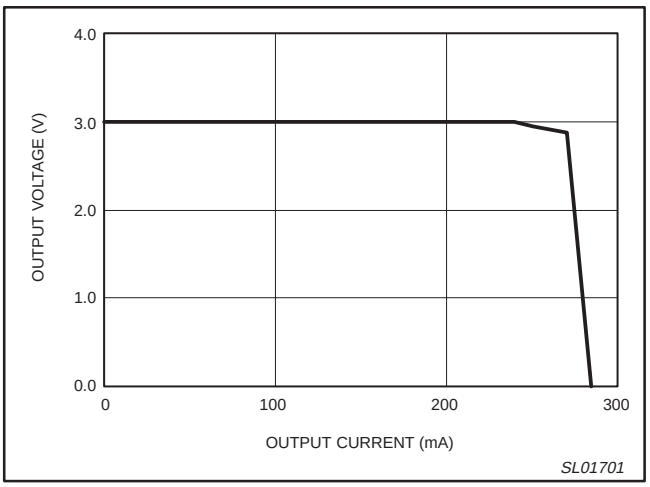


Figure 7. Current limit.

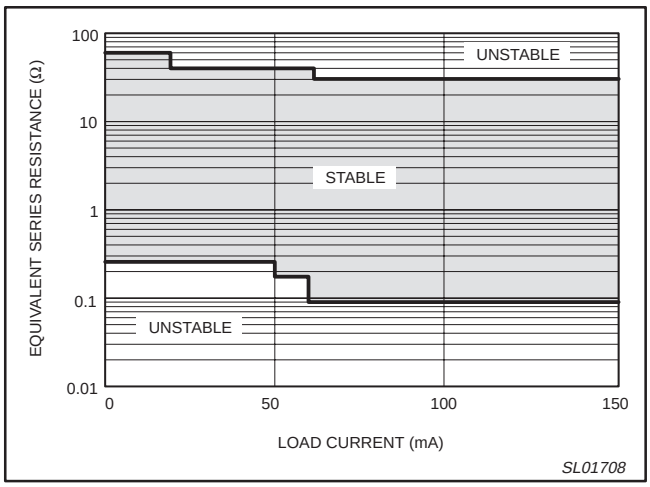


Figure 8. ESR stability.

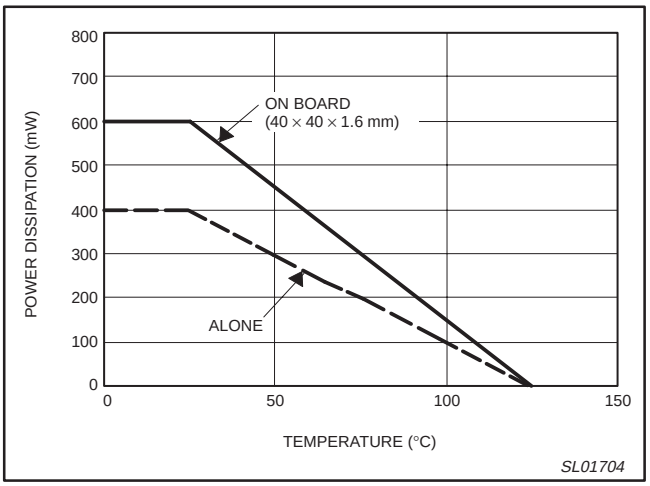


Figure 9. Power dissipation.

TECHNICAL DISCUSSION

As illustrated in the circuit diagram, each of the regulators in the SA57005 consists of a voltage reference, an error amplifier, P-channel pass transistor, current limit circuit and an internal feedback voltage divider. The output voltage is fed back through an internal resistor voltage divider connected to the output voltage pins. The reference will be activated if any of the PS1 and PS2/3 switches is turned on.

The reference is connected to the error amplifier's non-inverting input. The error amplifier compares the reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage the output of the error amplifier goes up, which pulls down the pass transistor's gate. This allows more current to pass to the output and increase the output voltage. On the other hand, if the feedback voltage is too high the pass transistor gate is pulled up, allowing less current to pass to the output, resulting a decrease in output voltage.

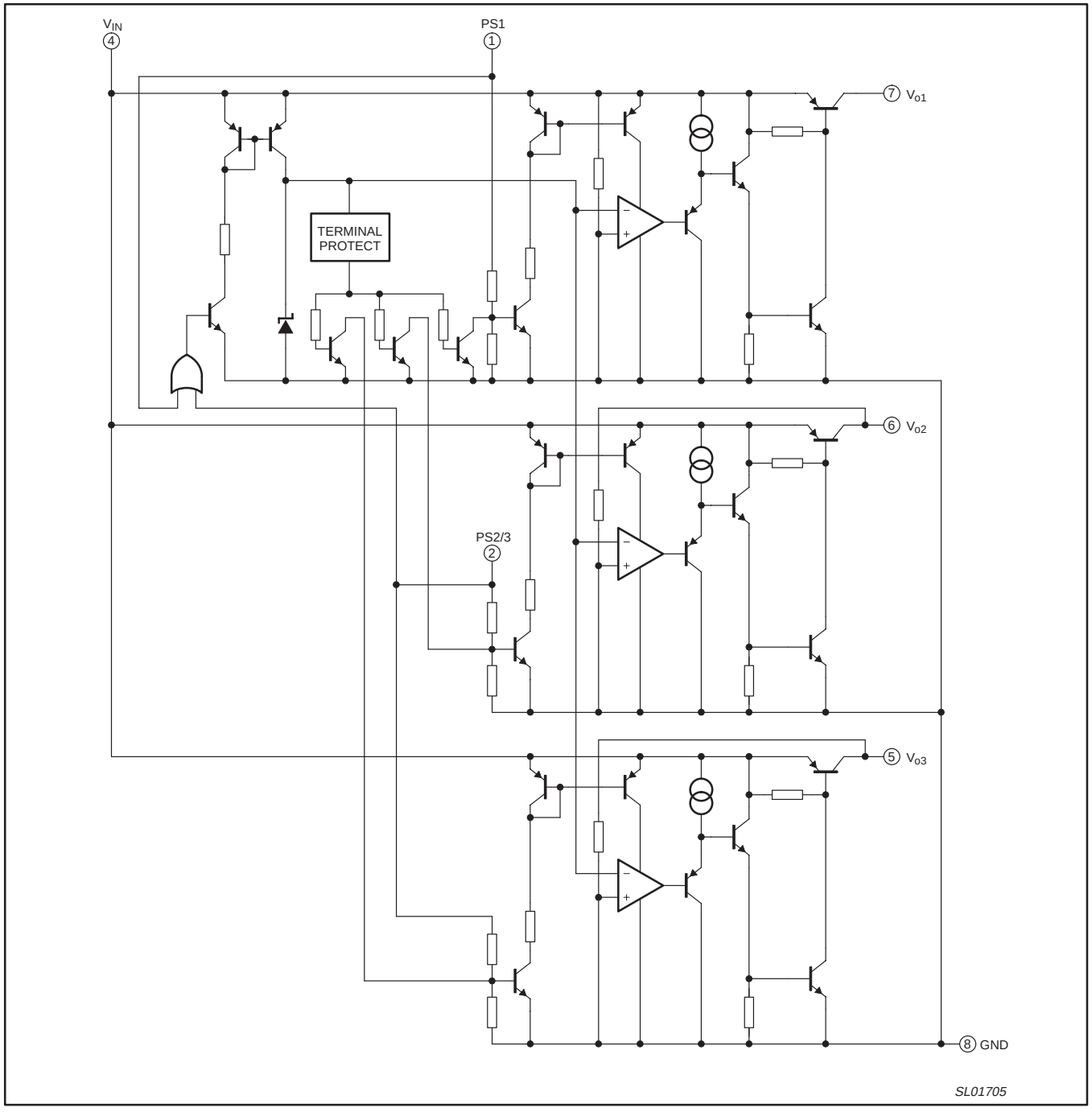


Figure 10. Functional diagram.

APPLICATION INFORMATION

For good performance, the following points must be considered:

Input capacitor

An input capacitor of ≥1 µF is required between the SA57005 input and the ground (the amount of capacitance may be increased without limit).

This capacitor must be located as close as possible to V_{IN} or GND pin (not more than 1 cm) and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitor will work.

Output capacitor

Phase compensation is made for securing stable operation even if the load current varies. For this reason, an output capacitor with good frequency characteristics is needed at each of the three outputs. Set it as close to the circuit as possible and make the wiring as short as possible.

The value of the output capacitance has to be at least 1µF. Also it must have the ESR (Equivalent Series Resistance) value within the stable range shown Figure 8.

PS (Chip Enable) pins

These active-HIGH ON/OFF pins must be actively terminated. If the function is not to be used, the corresponding PS pin should be tied to V_{IN}. PS1 (pin 1) controls V_{o1} while PS2/3 (pin 2) controls V_{o2} and V_{o3} simultaneously. In other words V_{o2} and V_{o3} are always in the same state, either both active or both inactive depending on the input of PS2/3.

Line impedance of V_{IN} and GND

The V_{IN} and GND lines should be sufficiently wide. Otherwise when the impedance of these lines is high, there is a chance to pick-up noise or malfunction.

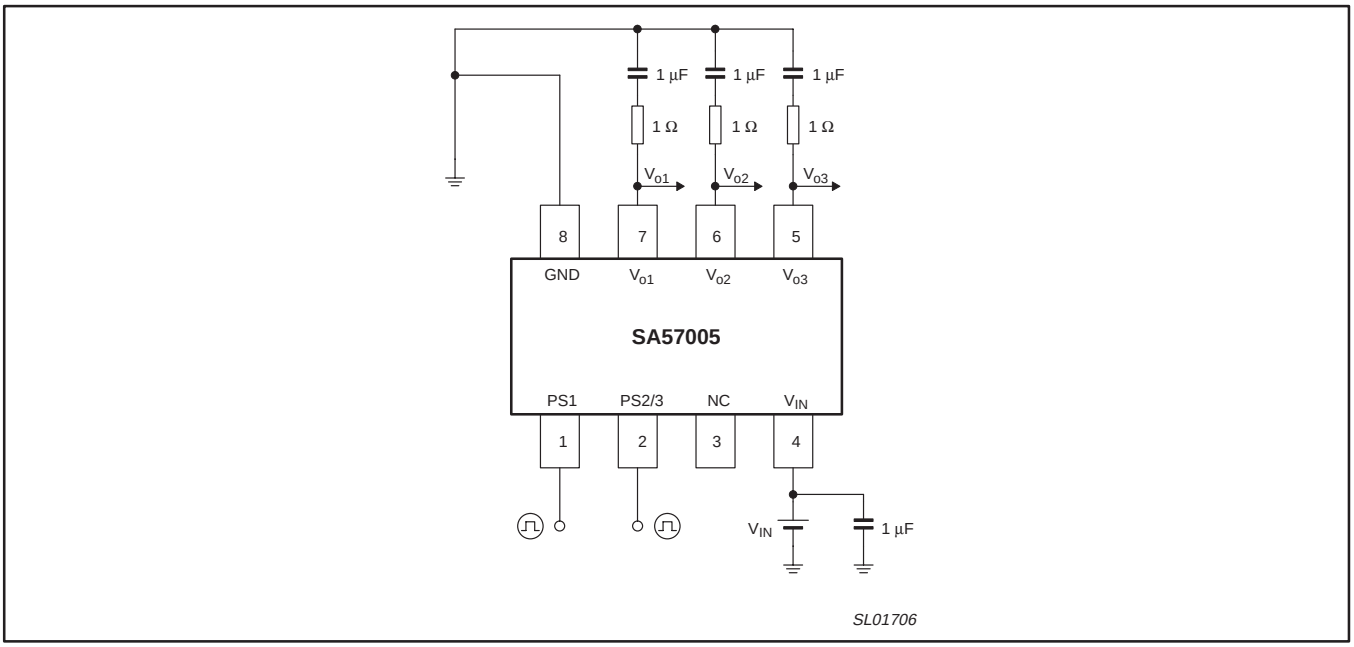


Figure 11. Typical application circuit.

TEST CIRCUIT

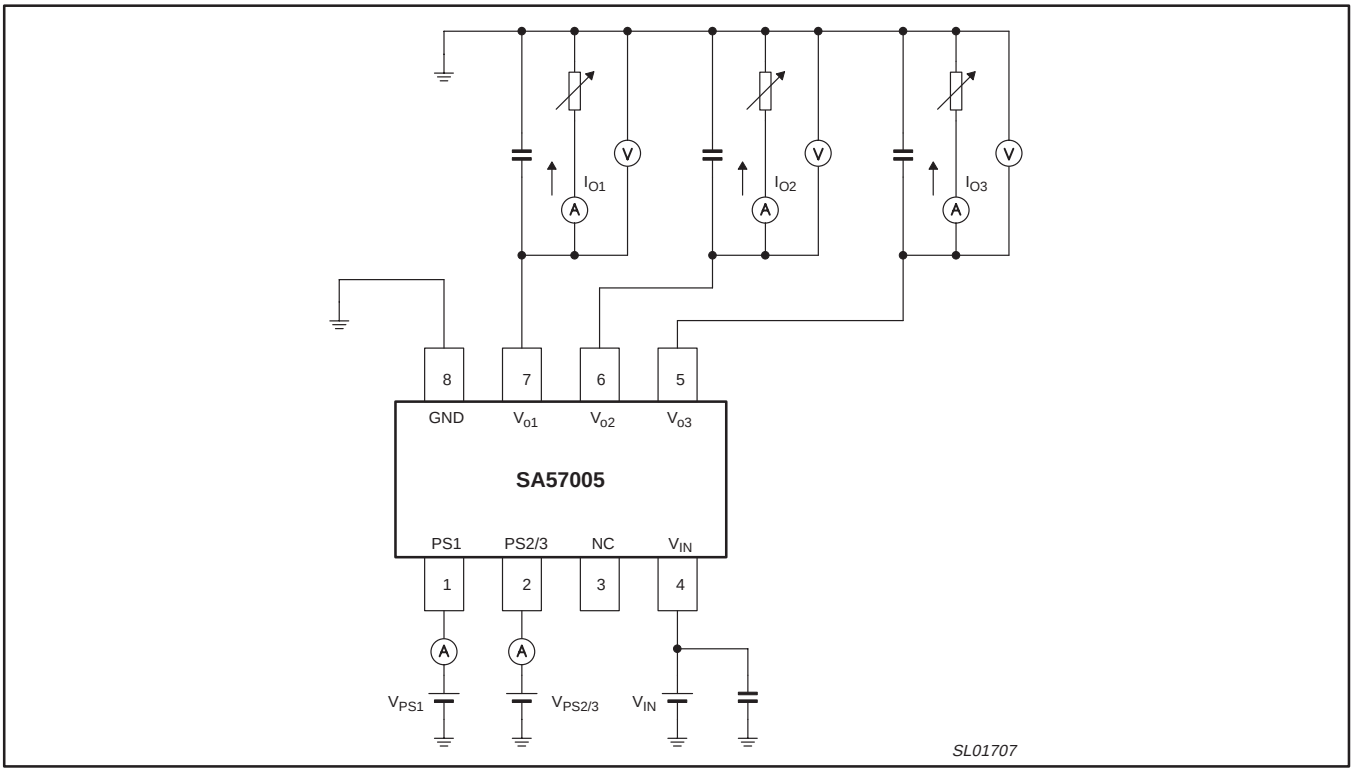


Figure 12. Test circuit.

PACKING METHOD

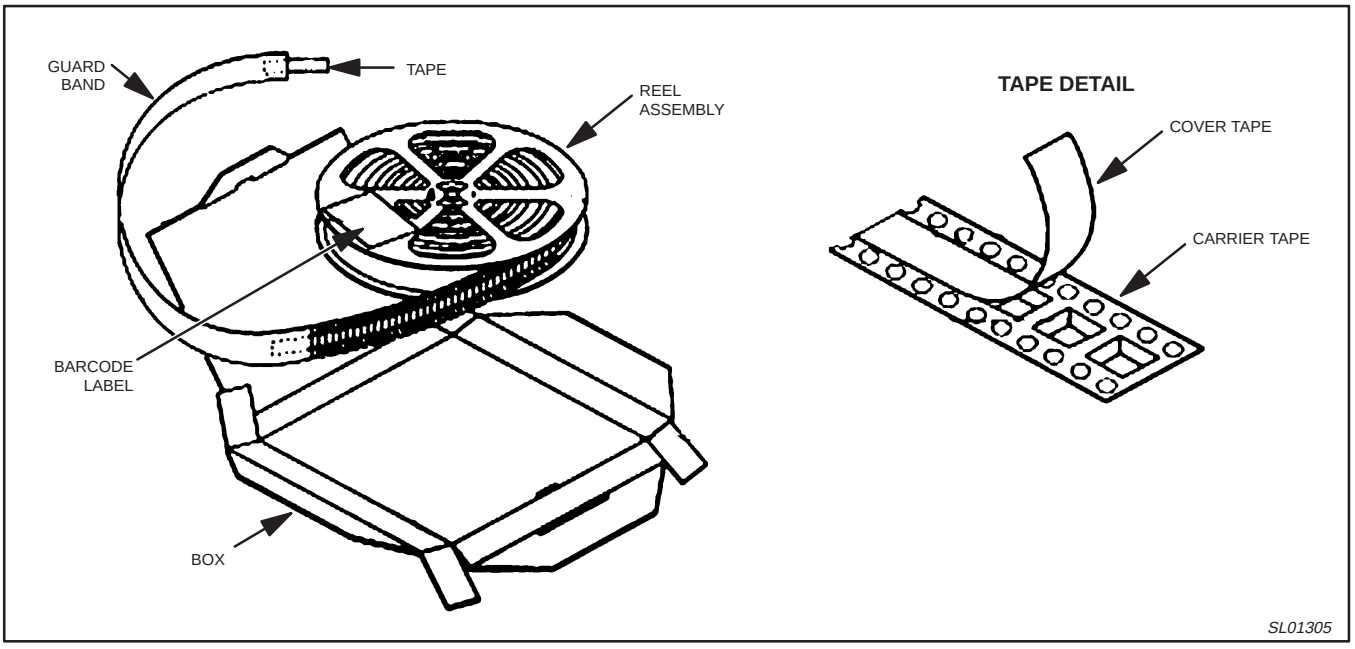
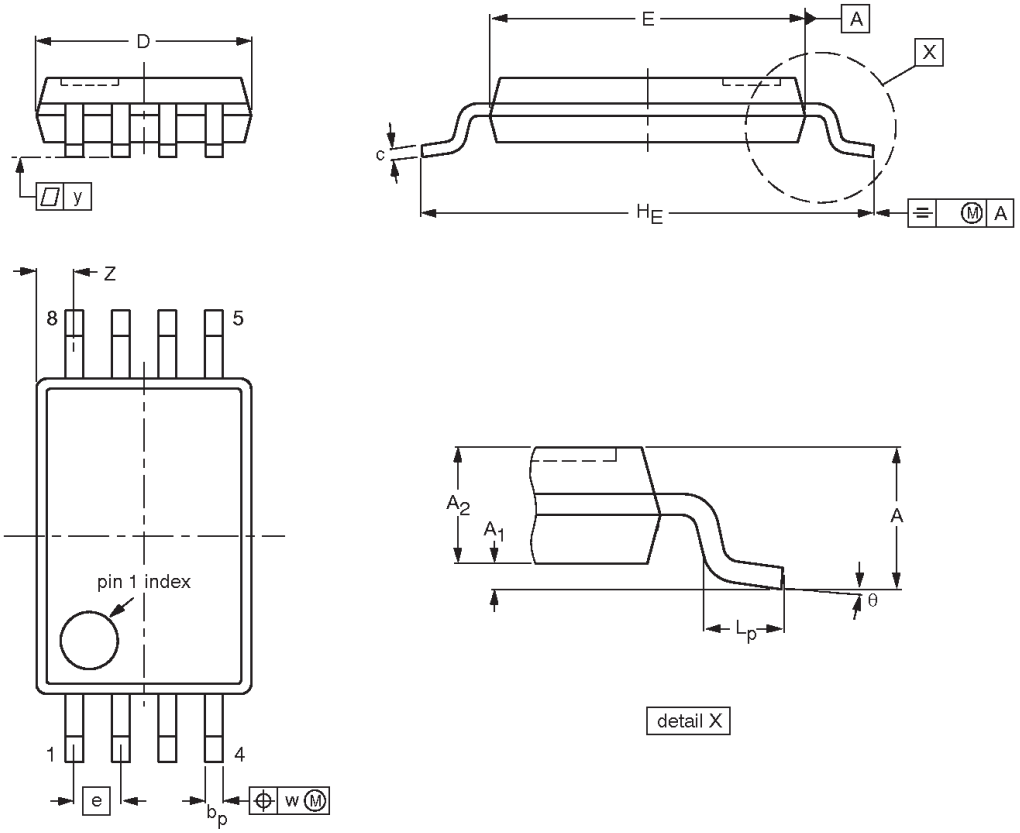


Figure 13. Tape and reel packing method.

VSOP-8A: plastic small outline package; 8 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2		b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E		L_p		w	y	$Z^{(1)}$	θ
mm	1.35 1.15	0.15 0.05	1.15		0.23 0.21	0.16 0.10	3.4 2.8	4.6 4.2	0.65	6.7 6.1		0.7 0.3		0.12	0.10	0.875 max.	10° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION
	IEC	JEDEC	EIAJ		
VSOP-8A					

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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