S3528B

AMI STANDARD PRODUCTS

Programmable Low Pass Filter

February 1993

Features

- Cutoff Frequency Selectable in 64 Steps Via Six Bit Control Word
- Continuously Tuneable Cutoff Frequency Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via Popular 3.58MHz TV Crystal
- Seventh Order Ellipitical Ladder Filter with Cosine Prefiltering Stage
- Passband Ripple: <0.1dB
- Stopband Attenuation: >51dB for $f>1.3f_C$
- Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- Steps May Be Custom Programmed from a Set of 2,048 Discrete Points Via Internal ROM
- Low Power CMOS Technology

Typical Applications for the S3528B and S3529B Programmable Filters

Telecommunications

- PBX and Trunk Line Status Monitoring
- Automatic Answering/Forwarding/Billing Systems
- Anti-Alias Filtering
- Adaptive Filtering

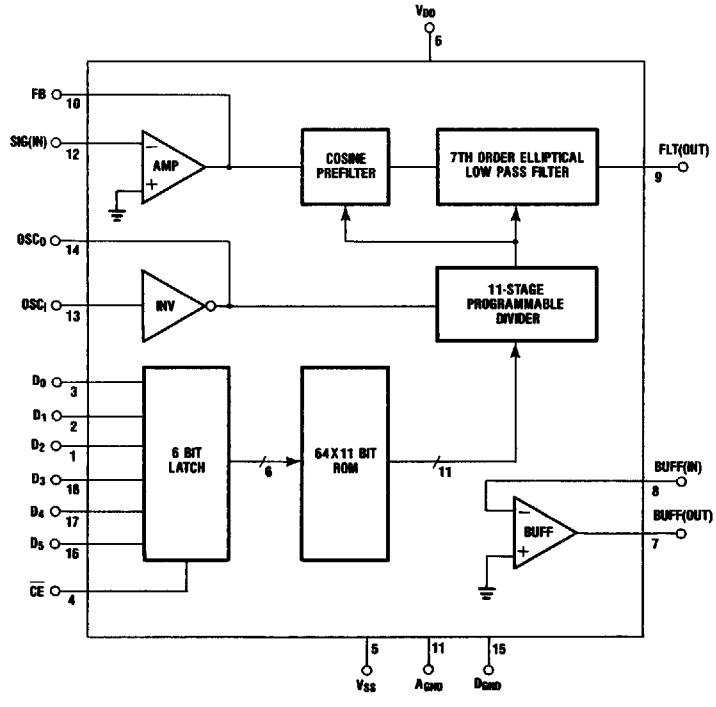
Remote Control

- Alarm Systems
- Heating Systems
- Acoustic Controllers

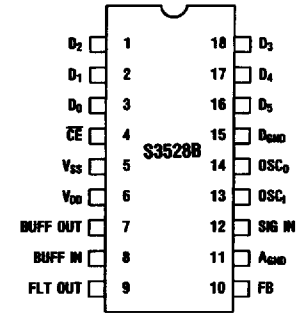
Test Equipment/Instrumentation

- Spectrum Analyzers
- Computer Controlled Analog Circuit Testers
- Medical Telemetry/Filtering
- ECG Signal Filtering
- Automotive Command Selection and Filtering

S3528B Block Diagram



Pin Configuration



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Programmable Low Pass Filter

Typical Applications for the S3528B and S3529B Programmable Filters (Continued)

Audio

- Electronic Organs
- Speech Analysis and Synthesis
- Speaker Crossovers
- Sonabuoys
- Spectrum Selection
- Low Distortion Digitally Tuned Audio Oscillators

General Description

The S3528B's CMOS design using switched-capacitor techniques allows easy programming of the filter's cutoff frequency (f_C) in 64 steps via a six-bit control word. For dynamic control of cutoff frequencies, the S3528B can operate as a peripheral to a microprocessor system with the code for the cutoff frequency being latched in from the data bus. When used with the companion high pass filter, the S3529B, a bandpass or a bandreject filter with a variable center frequency is obtained. For special applications the S3528B's internal ROM can be customized to accommodate a specific set of cutoff frequencies from a choice of 2,048 possibilities.

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	+ 15.0V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Input Voltage, All Pins	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V @13.5V		60 135	110 225	mW mW
R_{IN}	Input Resistance (Pins 1-4, 8, 12, 13, 16-18)	8			MΩ
C_{IN}	Input Capacitance (Pins 1-4, 8, 12, 13, 16-18)			15.0	pF

General Analog Signal Parameters: $(V_{DD} - V_{SS}) = 10V \pm 10\%$, $T_A = 0°C$ to $+70°C$, $f_{clock} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 0.6 f_C	−0.5	0	0.5	dB
V_0	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance FLT OUT, Pin 9	10			kΩ
R_L	Load Resistance BUFF OUT, Pin 7	600			ohms
V_{OUT}	Output Signal Level into R_L for FLT OUT, BUFF OUT, $V_{IN} = 2.1V$	2.0	2.1		VRMS
THD	Total Harmonic Distortion at $.3f_C$		.3		%
WBN	Wideband Noise (to 30kHz) $f_C = 3.2kHz$		.15		mVRMS
WBN	Wideband Noise (to 80kHz) $f_C = 15kHz$		.13		mvRMS
ICN	Idle Channel Noise $f_C = 3200Hz$		8	23	dBrnC0
V_{OS}	Buffer Output (Pin 7) Offset Voltage		±10	±30	mV
V_{OFS}	Filter Output (Pin 9) Offset Voltage		±80	±200	mV

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Filter Performance Specifications

Low Pass Filter Characteristics: $f_{clock} = 3.58MHz$, $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Pass Band Ripple (Ref. 0.6 f_c)	−0.5	±0.05	0.5	dB
Filter Response(1): F_c = 3200Hz (Pin 9)					
	(See Figure 5) (fc) 3200Hz	−0.5	±0.1	0.5	dB
	(1.06fc) 3372Hz	−5.5	−3.0	−0.5	dB
	(1.27fc) 4060		−42		dB
	(1.3fc) 4155		−51	−48	dB
	(1.32fc) 4235		−65	−48	dB
	(1.62fc) 5175		−75	−48	dB
	(1.3fc Upward) 4155 to 100,000Hz		< −51		dB
DR	Dynamic Range (V_{FS} to ICN) [+3.0 to −82 dBm]		85		dB

Digital Electrical Parameters: $V_{DD} = +5V$, $V_{SS} = -5V$, $T_A = 0°C$ to $+70°C$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	Volts
V_{IL}	Input Low Voltage	V_{SS}		0.8	Volts
I_N	Input Leakage Current (V_{IN} = 0 to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF
Digital Timing Characteristics					
t_{CE}	Chip Enable Pulse Width	200	300		nsec
t_{AS}	Address Setup Time		300		nsec
t_{AH}	Address Hold Time		20		nsec
f_{osc}	Crystal Oscillator Frequency(2)		3.58		MHz
t_{SET}	Settling Time from $\overline{CE}$ to Stable f_c (f_c = 3200)(3)		6		msec

1.) Filter Response Referenced to f = 1,920Hz

2.) The tables are based on common TV crystal. See paragraph on "Clock Frequencies" for more detail.

3.) $t_{SET} = \frac{10}{f_c} + 3msec$

Pin Function Description

Pin Name	Number	Function
V_{DD}	6	Positive supply voltage pin. Normally +5V ±10%.
V_{SS}	5	Negative supply voltage pin. Normally −5V ±10%.
A_{GND}	11	Analog ground reference point for analog input and output signals. Normally connected to ground.
D_{GND}	15	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	Control word Inputs: The set of six bits allows selection of one of sixty-four cutoff frequencies. The 6 bit control word is latched on the rising edge of $\overline{CE}$. The high-impedance inputs may be bridged directly across a microprocessor data bus. These inputs are TTL or CMOS compatible. A "1" is 2.0V to V_{DD}, and a "0" is 0.8V to V_{SS}.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	
$\overline{CE}$	4	Chip Enable: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_c changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_c immediately. This is the configuration for a fixed filter; $\overline{CE}$ is at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS}/D_{GRND} depending on the desired f_c.

Pin Function Description (Continued)

Pin Name	Number	Function
OSC_I OSC_O	13 14	Oscillator In and Oscillator Out: Placing a crystal and a 10MΩ resistor across these pins creates the time base oscillator. An inexpensive choice is to use the 3.58MHz TV colorburst crystal.
SIG IN	12	Signal Input: This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback: This is the feedback point for the input op amp. The feedback resistor should be ⩾10kΩ for proper operation.
FLT OUT	9	Filter Out: This is the high impedance output of the programmable low pass filter. Loads must be ⩾10kΩ.
BUFF IN	8	Buffer Input: The inverting input of the buffer amplifier.
BUFF OUT	7	Buffer Out: The buffer amplifier output to drive low impedance loads. This pin may drive as low as 600Ω loads.

Example of Circuit Connection for S3528B
Figure 1. Stand Alone Operation

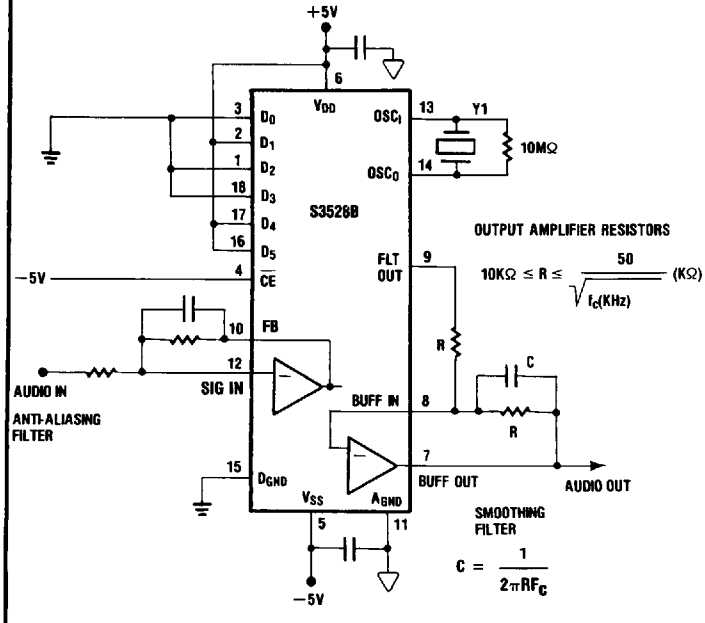
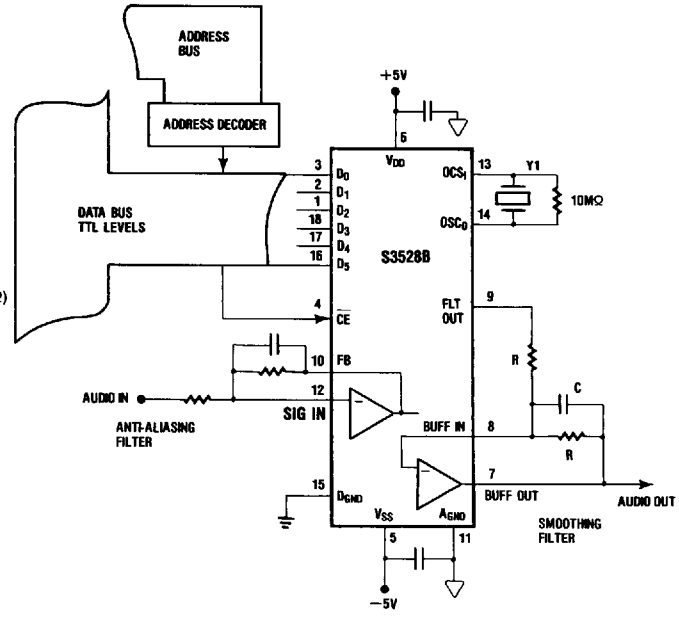


Figure 2. Microprocessor Interface



Operation

S3528B Filter is a CMOS Switched Capacitor Filter device designed to provide a very accurate, very flat, programmable filter that can be used in fixed applications where only one cutoff frequency is used, or in dynamic applications where logic or a microprocessor can select any one of 64 different cutoff frequencies. It is normally clocked by an inexpensive TV color burst crystal and provides the cutoff frequencies seen in Table 1 when the Data Bus pins are programmed.

All that is required for fixed operation is a 10MΩ resistor, the 3.58MHz TV crystal, and some resistors and capacitors around the input and output amplifiers to set the gain, anti-aliasing, and smoothing. The Data Bus pins are programmed from the table to either a "1" (+5V) or a "0" (ground or −5V) for the desired cutoff frequency. The $\overline{CE}$ pin is tied low, to V_{SS}.

Operation (Continued)

The ROM is addressed by the contents of the latch and presents an 11-bit word to the programmable divider which divides f_{CLK}.

The FILTER OUT pin is capable of driving a 10kΩ load directly or, for smoothing and driving a 600Ω load, the output buffer amplifier can be used for impedance matching.

As illustrated in the curves of Figures 3, and 5 through 7, the passband ripple (for fc<18kHz) is less than ±0.1dB and the stop band rejection is better than 50dB, as measured on a network analyzer.

For microprocessor controlled operation, the Data Bus can be bridged across a regular TTL bus and when $\overline{CE}$ is strobed, the data present will be latched in and the filter will settle down to its new cutoff frequency. In CMOS systems, the Data Bus and $\overline{CE}$ can be swung rail-to-rail. A_{GND} and D_{GND} must be at ½ the supply voltage.

The following table illustrates the available cutoff frequencies based on using a 3.58MHz TV crystal for a time base, by approximately 100Hz steps through the voice band from 100Hz to 3900Hz. Note that the hex input code for each frequency in the voice band is one-hundredth of the cutoff frequency. For 3200Hz, the hex code is 32, for 900Hz it is 09. Additional frequencies are listed with their codes on the right side of the Table 1.0.

Table 1.0—Standard Frequency Table: Programmable Filter S3528B. f_{CLOCK} = 3.58MHz

Voice Band

Input Code (HEX) D_5–D_0	Divider Ratio	f_c Actual (Hz)
00	2048	44
01	895	100
02	447	200
03	298	300
04	224	399
05	179	500
06	149	601
07	128	699
08	112	799
09	99	904
10	89	1005
11	81	1105
12	74	1209
13	69	1297
14	64	1398
15	60	1491
16	56	1598
17	53	1688
18	50	1790
19	47	1904
20	45	1989
21	43	2081
22	41	2183
23	39	2295
24	37	2418
25	36	2486
26	34	2632
27	33	2711
28	32	2797
29	31	2887
30	30	2983
31	29	3086
32	28	3196
33	27	3314
34	26	3442
36	25	3579
37	24	3728
39	23	3891

Additional Points Available

Input Code (HEX) D_5–D_0	Divider Ratio	f_c Actual (Hz)
0A	188	476
0B	358	250
0C	90	994
0D	87	1028
0E	85	1053
0F	78	1147
1A	61	1467
1B	58	1542
1C	52	1721
1D	46	1945
1E	44	2034
1F	40	2237
2A	38	2350
2B	35	2557
2C	22	4067
2D	20	4474
2E	18	4971
2F	16	5593
35	15	5965
38	14	6392
3A	12	7457
3B	10	8949
3C	9	9943
3D	6	14915
3E	5	17897
3F	4	22372

$$f_{cutoff} = \frac{f_{CLOCK}}{40\ (\text{Divider Ratio})}$$

$$f_{sampling} = \frac{f_{CLOCK}}{\text{Divider Ratio}}$$

Figure 3. Family of Loss Curves for 4 Different Control Codes

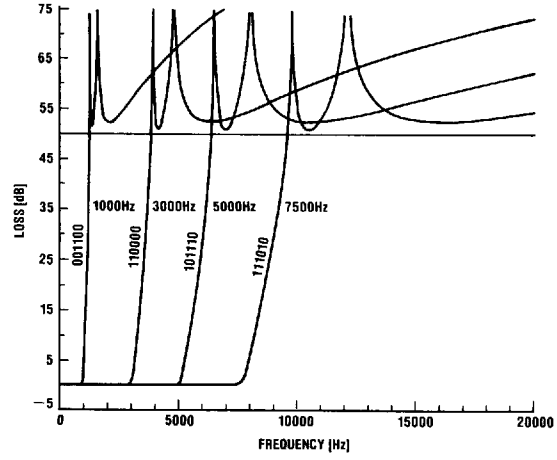


Figure 4. Address and Chip Enable Timing

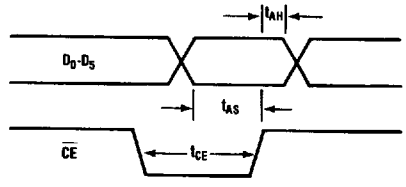


Figure 5. Loss Curve, Control = 110010, f_C = 3200Hz

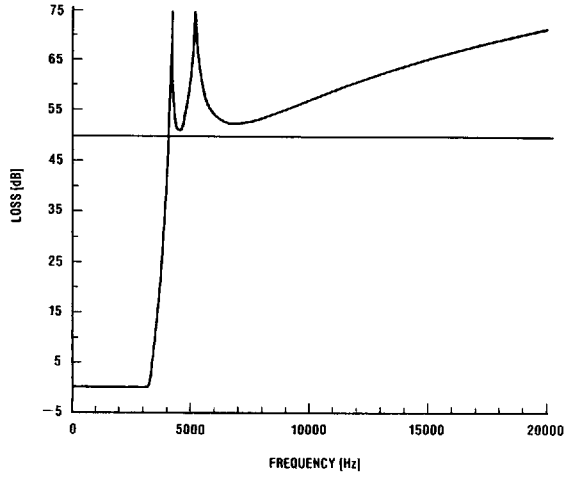


Figure 6. Passband Control Detail, Control = 110010, f_C = 3200Hz

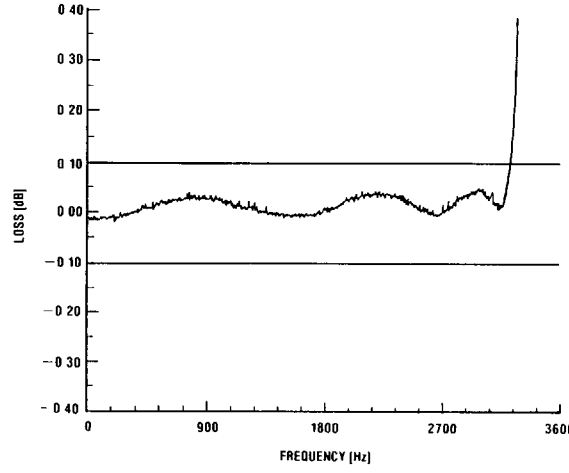


Figure 7. Family of Loss Curves for 4 Different Control Codes

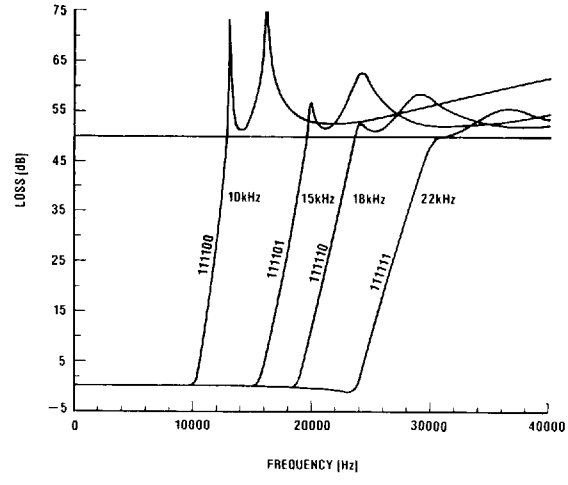


Figure 8. Loss and Group Delay, Fc = 3200Hz

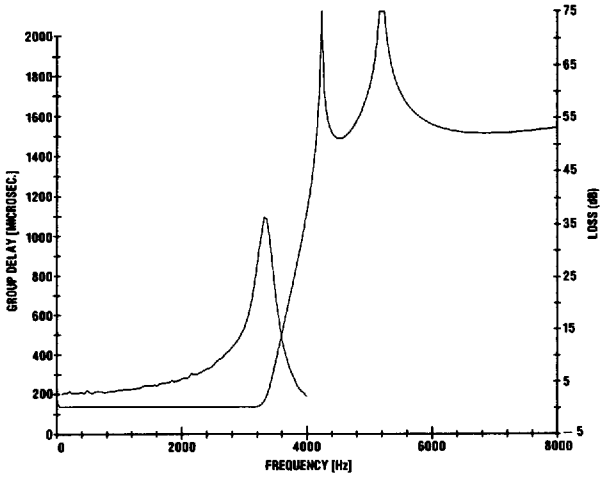
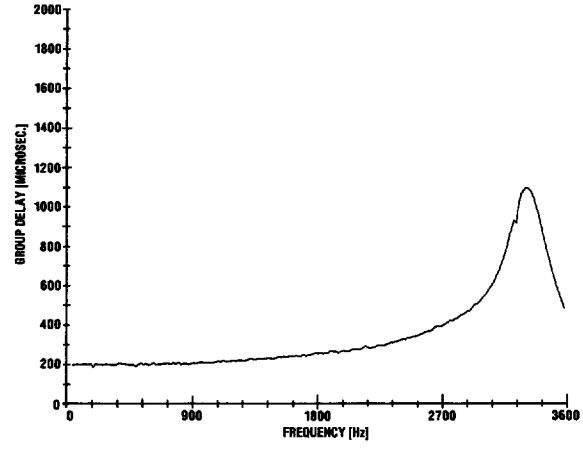


Figure 9. Group Delay, Control = 110010, FC = 3.2kHz

$$GD_{f_C = X} \doteq GD_{f_C = 3.2kHz} \left(\frac{3.2kHz}{X\ kHz}\right)$$



Applications Information

Many filter applications can benefit from the S3528B, particularly if extremely flat passband response with precise, repeatable cutoff frequencies are required. Or, if the same performance is required at different frequencies it can be switched or microprocessor controlled. The circuits (Figures 1 and 2) illustrate how the S3528B might be connected for two different uses. The "stand alone" drawing (Figure 1) shows how it would be programmed as a fixed, 3200Hz low pass filter. The other drawing (Figure 2) shows a microprocessor driven application that lets the cutoff frequency be varied on command.

Some fields that can use such a filter are speech analysis and scrambling, geo-physical instrumentation, under water accoustical instrumentation, two-way radio, telecommunications, electronic music, remotely programmable test equipment, tracking filter, etc.

Anti-Aliasing

In planning an application the basic fundamentals of sampling devices must be considered. For example, aliasing must be taken into consideration. If a frequency close to the sampling frequency is presented to the input it can be aliased or folded back into the passband. Because the S3528B has an input cosine filter the effective sample frequency is twice the filter clock frequency of 40 times the cutoff frequency. If f_C = 1000Hz and a signal of 79,200Hz is put into the filter, it will alias the 80kHz effective sampling frequency of the input cosine filter and appear as an 800Hz signal at the output. This means that for some applications the input op amp must be used to construct a simple one or two pole RC anti-aliasing filter to insure performance. In many situations, however, this will not be necessary since the input signal will already be band-limited.

Smoothing

In addition, all sampling devices will have aliased components near the clock frequency in the output. For example, there will be small components at $f_{clk} \pm f_{in}$ in the output waveform. This can be reduced by constructing a simple smoothing filter around the output buffer amplifier. Because of the sinx/x characteristics of a sample and hold stage the aliasing components are already better than 30dB down. The clock feed through is approximately −50dBV. This means that a simple one pole filter can provide another 20dB of rejection to keep the aliasing below 50dB down. In the case of a 3kHz f_{CUTOFF} and the smoothing filter designed for a 3dB point at $4f_{CUTOFF}$ the smoothing filter will affect

Smoothing (continued)

the 3kHz point by .25dB. If this is not desirable then the smoothing filter might be constructed as a second order filter.

For a fixed application, anti-aliasing and smoothing are straight forward. For a dynamic operation, the desired operating range of frequencies must be considered carefully. It may be necessary to switch in or out additional components in the RC filters to move cutoff frequencies. The S3528B has a ratio of cutoff frequencies of 550:1 and to use the full range would require some switching.

Notch Rejection

The filter is designed to have 51dB of rejection at $1.3f_{CUTOFF}$ and greater. If greater rejection of a specific tone or signal frequency is desired, the cutoff frequency can be selected to position the undesired tone at $1.325f_{CUTOFF}$ or $1.62f_{CUTOFF}$. This will place it in a notch as illustrated in Figure 5.

The S3529B (High Pass Filter) and the S3528B (Low Pass Filter) can be used together to make either Band Pass or Band Reject/Notch filters. The control code selection determines the bandwidth of the resulting filter.

It should be noted that with the S3528B and S3529B data pins connected in parallel and their analog inputs and outputs in series a bandpass filter of approximately 10% bandwidth is created.

Figure 10. S3528B and S3529B in Parallel Notch Configuration—Narrow Bandwidth

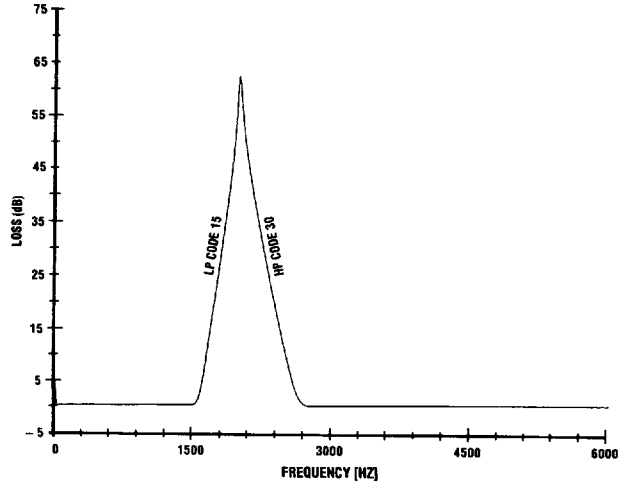


Figure 11. Cascaded S3528B and S3529B Control = 100001 Bandpass Configuration—10% Bandwidth

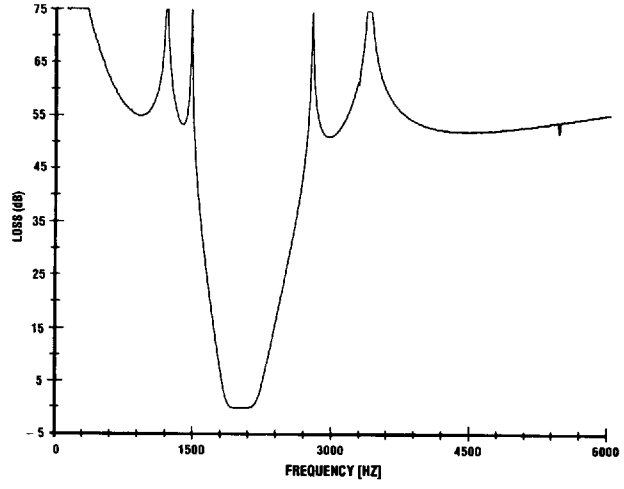
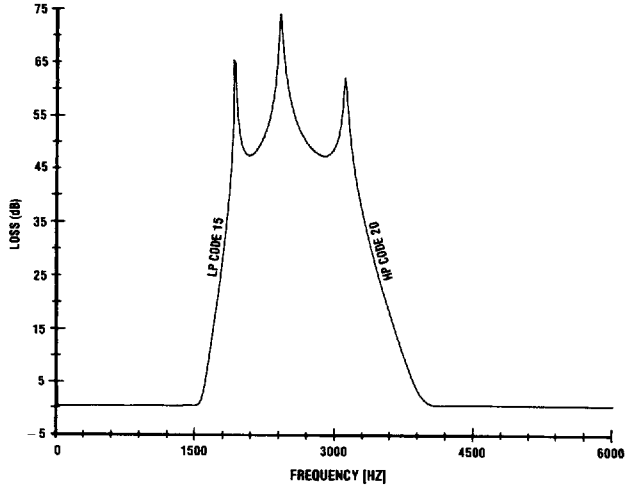


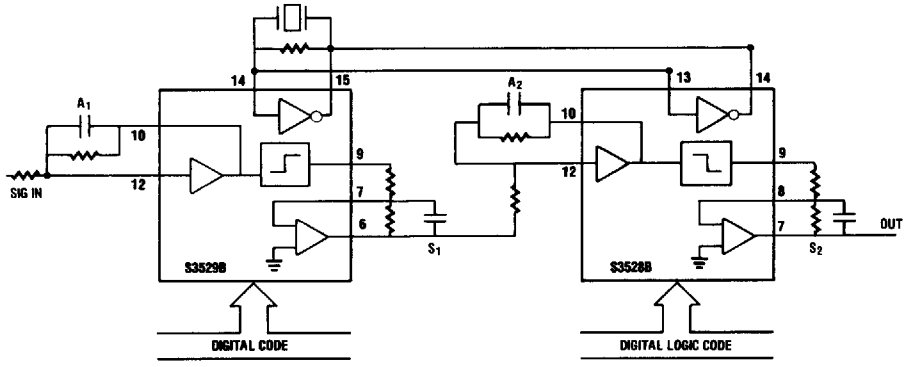
Figure 12. S3528B and S3529B in Parallel Notch Configuration—Wide Bandwidth



Crystal Oscillator

The S3528B crystal oscillator circuit requires a 10 Meg ohm resistor in parallel with a standard 3.58MHz television colorburst crystal. For this application, however, crystals with relaxed tolerances can be used. Specifications can be as follows:

Figure 13. Bandpass Application: General Case Configuration



Note:

— Anti-aliasing and smoothing filters on both chips A1, A2, S1, S2

— Lowpass after highpass to remove higher harmonics, unless cosine input filter of lowpass needed to clean noisy input signal

— For wider band width two different oscillators can be used.

- For same digital logic code
  N = multiple of clock#1 to clock#2

$$f_{cL} = \frac{.9 f_{cu}}{N}$$

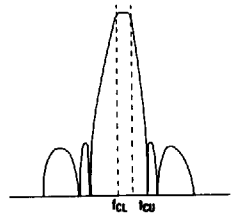


Figure 14. Notch Applications: General Case Configuration

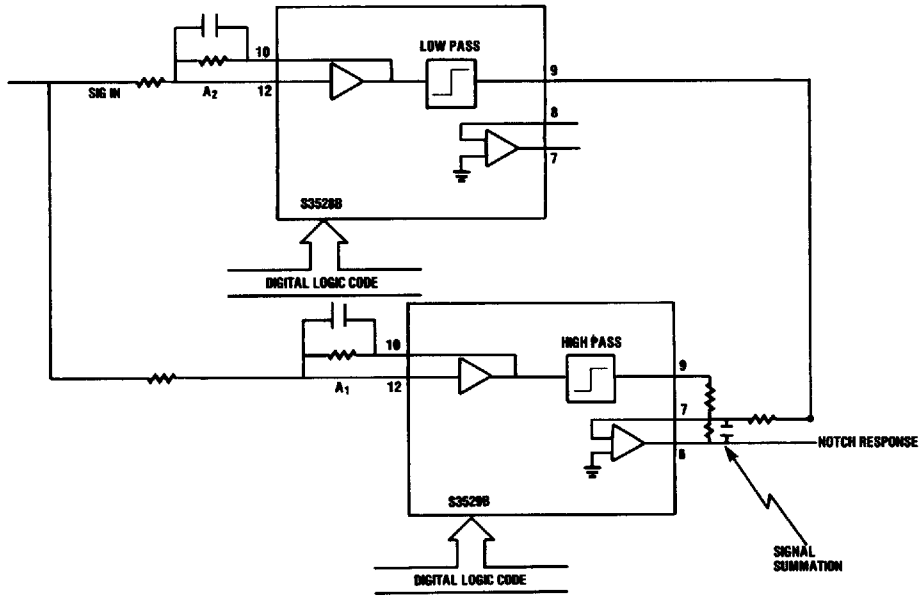
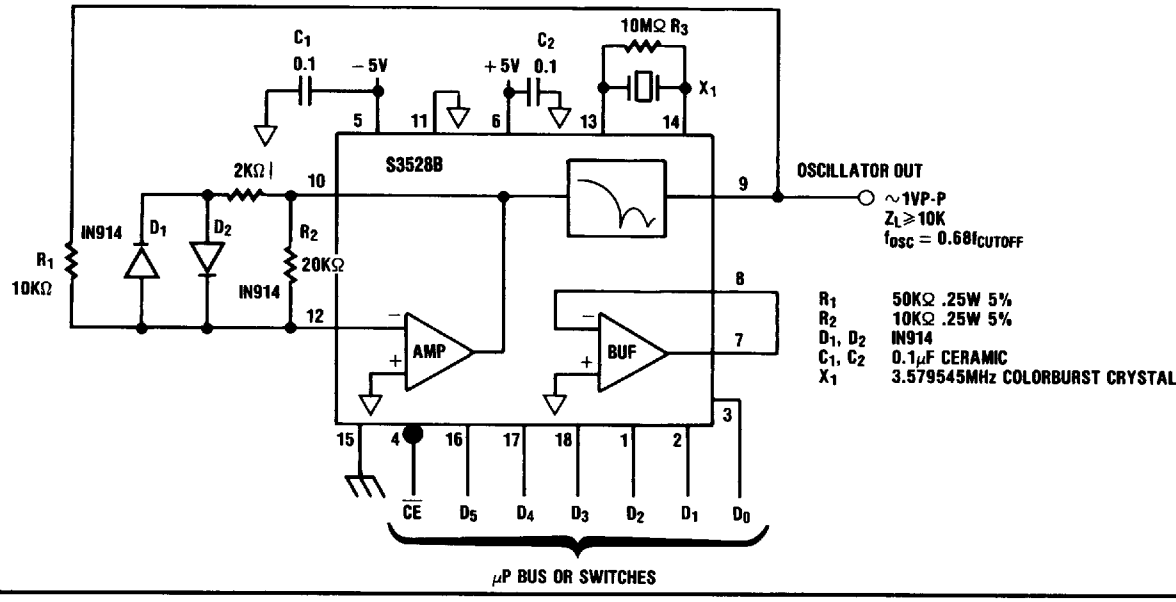


Figure 15. Low Distortion Digitally Tuned Audio Oscillator Application Circuit



Frequency	3.579545 ±.02%
RS≤180Ω	L_M~96MH
C_L = 18pF	C_h = 7pF

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 13). [Max. zero~30% (V_{DD}-V_{SS}), min. one~70% (V_{DD}-V_{SS})]. Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10 Meg ohm feedback resistor is installed as shown in Figure 16.

Although the tables are constructed around the TV colorburst crystal, other clock frequencies can be used from crystals or external clocks to achieve any cutoff frequency in the operating range. For example, by using a rate multiplier and duty-cycle restorer circuit between the system clock and the S3528B, and switching the inputs to the S3528B, almost any cutoff frequency between 40Hz and 35kHz can be selected. The clock input frequency can be anywhere between 500kHz and 5MHz.

In addition to crystals or external clocks the S3528B can be used with ceramic resonators such as the Murata CSA series "Ceralock" devices. All that is required is the resonator and 2 capacitors to V_{SS}. Although the resonators are not quite as accurate as crystals they can be less expensive.

Figure 16. S3528B Driving Additional S3528B or S3529B Devices

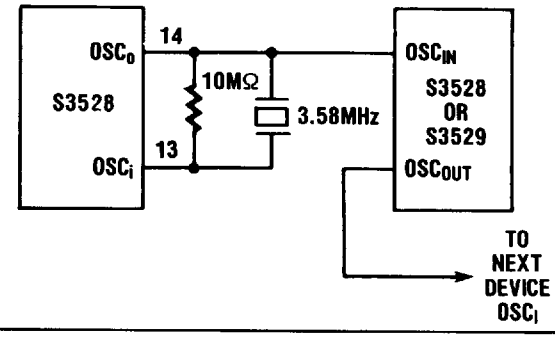


Figure 17. External Driving S3528B Pin OSC_i