PIM_9DTB128
Port Integration Module (PIM)

Block User Guide
V01.03

Original Release Date: 05 Feb 2001
Revised: 2 Aug, 2002

Motorola, Inc

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
1.0	05 FEB 2001			1st release based on pim_9DP256 rev 2.0
01.01	7 Aug 2001			-Capitalized all pin names to match Marlin DUG -Corrected typo in PPSJ description -added full register names in memory map table
01.02	11 Mar 2002			- Changed document order #
01.03	2 Aug 2002			-Corrected some port descriptions in table 2-1, descriptions of WOMS (port S) & PERM (port M) in table 3-1, Port M definitions in fig 3-14 -Added back SPI1 bits for PTH in 3.3.5 -Corrected document order # to match reference name

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Section 1 Introduction

1.1 Overview

The Port Integration Module establishes the interface between the peripheral modules and the I/O pins for all ports except AD0 and AD1.

The two 8-bit ports associated with the ATD are included in the ATD module due to their sensitivity to electrical noise, requiring special care on routing and design.

This section covers port A, B, E, and K related to the core logic and multiplexed bus interface, port T connected to the timer module, the serial port S associated with 2 SCI and 1 SPI module, the multiplex ports M, associated with 3 CAN, 1 ByteFlight and 1 BDLC module, and P, connected to the PWM and 1 SPI module, the standard I/O port H, and finally the port J associated with CAN4 and the IIC interface.[1] Ports P, H and J can also be used as external interrupt sources.

Each I/O pin can be configured by several registers: Input/output selection, drive strength reduction, enable and select of pull resistors, interrupt enable and status flags.

The I/O's of 2 CAN and all 2 SPI modules can be routed from their default location to determined pins.

The Port Integration Module is device dependant which is reflected in its naming.

1.2 Features

A standard port has the following minimum features:

- Input/output selection
- 5V output drive with two selectable drive strength
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-or connections
- Interrupt inputs with glitch filtering

1.3 Block Diagram

Figure 1-1 is a block diagram of the PIM_9DTB128.

NOTES:
1. The port control register addresses are allocated in the order of their most likely occurrence, i. e. almost all STAR12 derivatives will have a timer port, and a very limited number will have a IIC module. This allows best consistency in the address allocation.

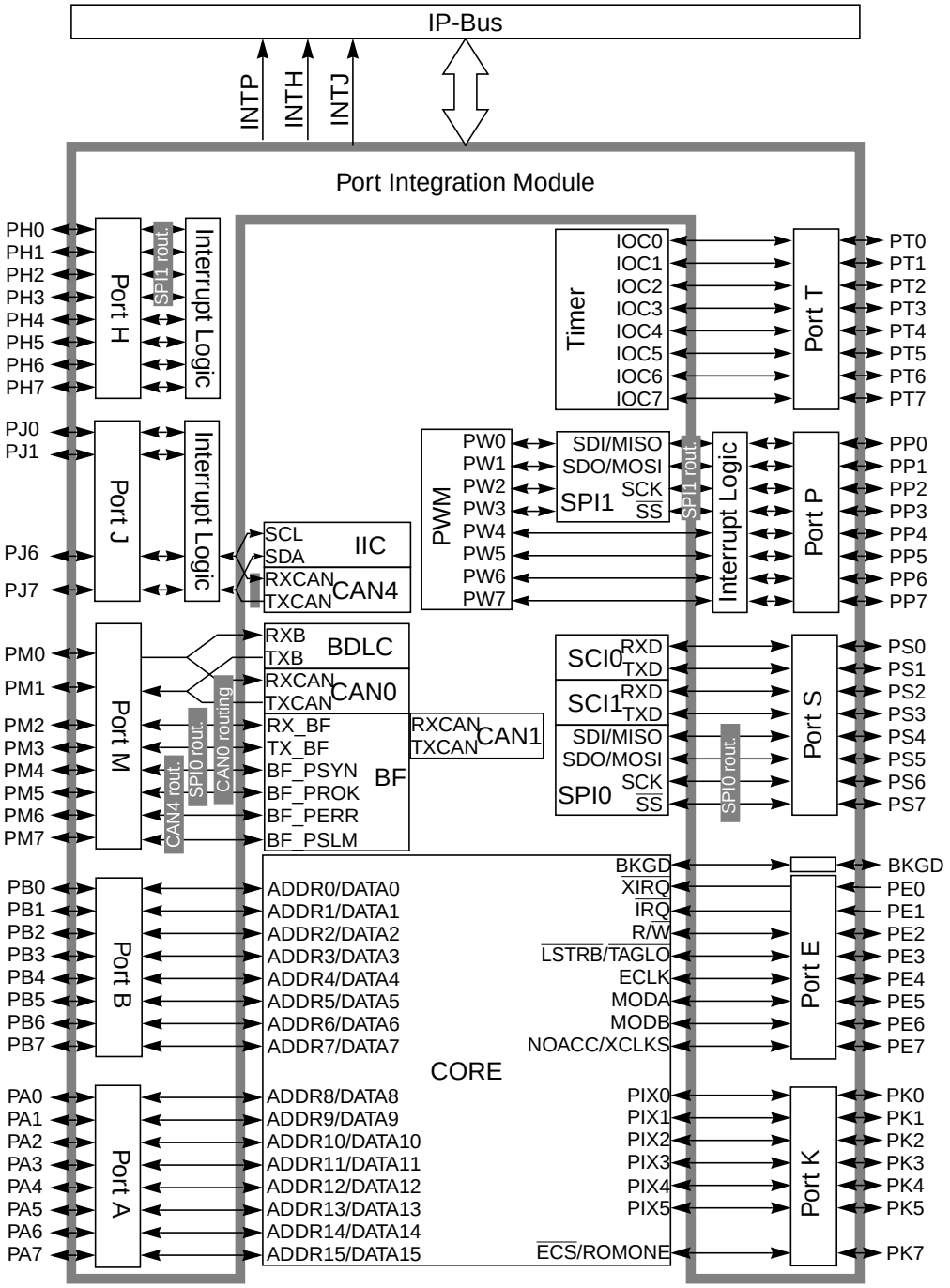

Figure 1-1 PIM_9DTB128 Block Diagram

Section 2 Signal Description

2.1 Overview

This section lists and describes the signals that do connect off chip.

NOTE: *Refer to the Creation Guide and the Integration Guide documentation of the PIM_9DTB128 for a detailed description of the pad control signals.*

2.2 Signal properties

Table 2-1 shows all the pins and their functions that are controlled by the PIM_9DTB128.

Table 2-1 Signal Properties

Pin Name	Port	Pin Function	Description	Reset State	Pull Mode
PT[7:0]	Port T	IOC[7:0]	Capture Timer Channel	input	hiz
PS7	Port S	$\overline{SS0}$	Slave select output for SPI0 master mode, input for slave mode or master mode.	input	pull-up
PS6		SCK0	Serial clock for serial peripheral system 0		
PS5		MOSI0	Master out/slave in pin for serial peripheral interface 0		
PS4		MISO0	Master in/slave out pin for serial peripheral interface 0		
PS3		TXD1	SCI1 transmit pin		
PS2		RXD1	SCI1 receive pin		
PS1		TXD0	SCI0 transmit pin		
PS0		RXD0	SCI0 receive pin		
PM7	Port M	BF_PSLM_TXCAN4	ByteFlight Status / MSCAN4 transmit pin	input	hiz
PM6		BF_PERR_RXCAN4	ByteFlight Error Status / MSCAN4 receive pin		
PM5		BF_PROK_TXCAN0_TXCAN4_SCK0	ByteFlight Status / MSCAN0/MSCAN4 transmit pin / serial clock for serial peripheral system 0		
PM4		BF_PSYN_RXCAN0_RXCAN4_MOSI0	ByteFlight Status / MSCAN0/MSCAN4 receive pin / master out/slave in pin for serial peripheral interface 0		
PM3		TX_BF_TXCAN1_TXCAN0_$\overline{SS0}$	ByteFlight transmit pin / MSCAN1/MSCAN0 transmit pin / slave select output for SPI0 master mode, input for slave mode or master mode.		
PM2		RX_BF_RXCAN1_RXCAN0_MISO0	ByteFlight receive pin / MSCAN1/MSCAN0 receive pin / master in/slave out pin for serial peripheral interface 0		
PM1		TXCAN0_TXB	MSCAN0 transmit pin, shared with BDLC transmit pin		
PM0		RXCAN0_RXB	MSCAN0 receive pin, shared with BDLC receive pin		

Pin Name	Port	Pin Function	Description	Reset State	Pull Mode
PP7	Port P	PWM7_KWP7	Pulse Width Modulator Channel Pins shared interrupt	input	hiz
PP6		PWM6_KWP6			
PP5		PWM5_KWP5			
PP4		PWM4_KWP4			
PP3		PWM3_$\overline{SS1}$_KWP3	Pulse Width Modulator Channel Pins shared with SPI1 and interrupt		
PP2		PWM2SCK1_KWP2			
PP1		PWM1_MOSI1_KWP1			
PP0		PWM0_MISO1_KWP0			
PH7	Port H	KWH7	General Purpose I/O and interrupt	input	hiz
PH6		KWH6			
PH5		KWH5			
PH4		KWH4			
PH3		$\overline{SS1}$_KWH3	SPI1, general Purpose I/O and interrupt		
PH2		SCK1_KWH2			
PH1		MOSI1_KWH1			
PH0		MISO1_KWH0			
PJ7	Port J	TXCAN4_SCL_KWJ7	MSCAN4 transmit pin shared with IIC serial clock line and interrupt	input	pull-up
PJ6		RXCAN4_SDA_KWJ6	MSCAN4 receive pin shared with IIC serial data line and interrupt		
PJ[1:0]		KWJ[1:0]	General Purpose I/O and interrupt		
PA[7:0]	Port A	ADDR[15:8]_DATA[15:8]	External bus pins share function with general-purpose I/O ports A. In single chip modes, the pins can be used for general-purpose I/O. In expanded modes, the pins are used for the external buses.	input	hiz
PB[7:0]	Port B	ADDR[7:0]_DATA[7:0]	External bus pins share function with general-purpose I/O port B. In single chip modes, the pins can be used for general-purpose I/O. In expanded modes, the pins are used for the external address and data buses.	input	hiz

Pin Name	Port	Pin Function	Description	Reset State	Pull Mode
PE7	Port E	NOACC_$\overline{\text{XCLKS}}$	No Access. Indicates free cycles in expanded mode. Selects also external clock or oscillator during reset. Can be used as general purpose I/O pin.	input	pull-up
PE6		IPIPE1_MODB	State of mode select pins during reset determine the initial operating mode of the MCU. After reset, MODB and MODA can be configured as instruction queue tracking signals IPIPE1 and IPIPE0 or as general-purpose I/O pins.	input	1
PE5		IPIPE0_MODA		input	1
PE4		ECLK	E Clock is the output connection for the external bus clock. ECLK is used as a timing reference and for address demultiplexing.	input	pull-up
PE3		PE3_$\overline{\text{LSTRB}}$_TAGLO	Low byte strobe (0 = low byte valid), in all modes this pin can be used as I/O. The low strobe function is the exclusive-NOR of A0 and the internal $\overline{\text{SZ8}}$ signal. (The $\overline{\text{SZ8}}$ internal signal indicates the size 16/8 access.) Pin function $\overline{\text{TAGLO}}$ used in instruction low byte tagging.	input	pull-up
PE2		PE2_R/$\overline{\text{W}}$	Indicates direction of data on expansion bus. Shares function with general-purpose I/O. Read/write in expanded modes.	input	pull-up
PE1		PE1_$\overline{\text{IRQ}}$	Maskable interrupt request input provides a means of applying asynchronous interrupt requests to the MCU. Either falling edge-sensitive triggering or level-sensitive triggering is program selectable (INTCR register).	input	pull-up
PE0		PE0_$\overline{\text{XIRQ}}$	The $\overline{\text{XIRQ}}$ input provides a means of requesting a nonmaskable interrupt after reset initialization. Because it is level sensitive, it can be connected to a multiple-source wired-OR network.	input	pull-up
PK7	Port K	$\overline{\text{ECS}}$/ROMONE	Emulation Chip select/ROMONE function	input	pull-up
PK[5:0]		XADDR[19:14]	Expanded Addresses	input	pull-up
BKGD	-	MODC_TAGHI	Pseudo_open_drain communication pin for the single-wire background debug mode. At the rising edge on RESET, the state of this pin is latched into the MODC bit to set the mode. When instruction tagging is on, a 0 at the falling edge of E tags the high half of the instruction word being read into the instruction queue.	input	pull-up

NOTES:
1. pull-down only while reset asserted

Section 3 Memory Map and Registers

3.1 Overview

This section provides a detailed description of all registers.

3.2 Module Memory Map

Table 3-1 shows the register map of the Port Integration Module.

Table 3-1 PIM_9DTB128 Memory Map

Address offset	Use	Access
$00	Port T I/O Register (PTT)	RW
$01	Port T Input Register (PTIT)	R
$02	Port T Data Direction Register (DDRT)	RW
$03	Port T Reduced Drive Register (RDRT)	RW
$04	Port T Pull Device Enable Register (PERT)	RW
$05	Port T Polarity Select Register (PPST)	RW
$06	Reserved	-
$07	Reserved	-
$08	Port S I/O Register (PTS)	RW
$09	Port S Input Register (PTIS)	R
$0A	Port S Data Direction Register (DDRS)	RW
$0B	Port S Reduced Drive Register (RDRS)	RW
$0C	Port S Pull Device Enable Register (PERS)	RW
$0D	Port S Polarity Select Register (PPSS)	RW
$0E	Port S Wired-Or Mode Register (WOMS)	RW
$0F	Reserved	-
$10	Port M I/O Register (PTM)	RW
$11	Port M Input Register (PTIM)	R
$12	Port M Data Direction Register (DDRM)	RW
$13	Port M Reduced Drive Register (RDRM)	RW
$14	Port M Pull Device Enable Register (PERM)	RW
$15	Port M Polarity Select Register (PPSM)	RW
$16	Port M Wired-Or Mode Register (WOMM)	RW
$17	Module Routing Register (MODRR)	RW
$18	Port P I/O Register (PTP)	RW
$19	Port P Input Register (PTIP)	R
$1A	Port P Data Direction Register (DDRP)	RW
$1B	Port P Reduced Drive Register (RDRP)	RW
$1C	Port P Pull Device Enable Register (PERP)	RW
$1D	Port P Polarity Select Register (PPSP)	RW
$1E	Port P Interrupt Enable Register (PIEP)	RW
$1F	Port P Interrupt Flag Register (PIFP)	RW
$20	Port H I/O Register (PTH)	RW

$21	Port H Input Register (PTIH)	R
$22	Port H Data Direction Register (DDRH)	RW
$23	Port H Reduced Drive Register (RDRH)	RW
$24	Port H Pull Device Enable Register (PERH)	RW
$25	Port H Polarity Select Register (PPSH)	RW
$26	Port H Interrupt Enable Register (PIEH)	RW
$27	Port H Interrupt Flag Register (PIFH)	RW
$28	Port J I/O Register (PTJ)	RW[1]
$29	Port J Input Register (PTIJ)	R
$2A	Port J Data Direction Register (DDRJ)	RW[1]
$2B	Port J Reduced Drive Register (RDRJ)	RW[1]
$2C	Port J Pull Device Enable Register (PERJ)	RW[1]
$2D	Port J Polarity Select Register (PPSJ)	RW[1]
$2E	Port J Interrupt Enable Register (PIEJ)	RW[1]
$2F	Port J Interrupt Flag Register (PIFJ)	RW[1]
$30 – $3F	Reserved	-

NOTES:

1. Write access not applicable for one or more register bits. Please refer to detailed signal description.

NOTE: *Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.*

3.3 Register Descriptions

The following table summarizes the effect on the various configuration bits, data direction (DDR), output level (I/O), reduced drive (RDR), pull enable (PE), pull select (PS) and interrupt enable (IE) for the ports. The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 3-2 Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull Up	Disabled
0	X	X	1	1	0	Input	Pull Down	Disabled
0	X	X	0	0	1	Input	Disabled	falling edge
0	X	X	0	1	1	Input	Disabled	rising edge
0	X	X	1	0	1	Input	Pull Up	falling edge
0	X	X	1	1	1	Input	Pull Down	rising edge
1	0	0	X	X	0	Output, full drive to 0	Disabled	Disabled
1	1	0	X	X	0	Output, full drive to 1	Disabled	Disabled
1	0	1	X	X	0	Output, reduced drive to 0	Disabled	Disabled
1	1	1	X	X	0	Output, reduced drive to 1	Disabled	Disabled
1	0	0	X	0	1	Output, full drive to 0	Disabled	falling edge
1	1	0	X	1	1	Output, full drive to 1	Disabled	rising edge
1	0	1	X	0	1	Output, reduced drive to 0	Disabled	falling edge
1	1	1	X	1	1	Output, reduced drive to 1	Disabled	rising edge

NOTES:
1. Applicable only on port P, H and J.

NOTE: *All bits of all registers in this module are completely synchronous to internal clocks during a register read.*

3.3.1 Port T Registers

Address Offset: $__00

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
ECT:	I/OC7	I/OC6	I/OC5	I/OC4	I/OC3	I/OC2	I/OC1	I/OC0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-1 Port T I/O Register (PTT)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

Address Offset: $__01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-2 Port T Input Register (PTIT)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Address Offset: $__02

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-3 Port T Data Direction Register (DDRT)

Read:Anytime.

Write:Anytime.

This register configures each port T pin as either input or output.
The ECT forces the I/O state to be an output for each timer port associated with an enabled output compare. In these cases the data direction bits will not change.
The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled.
The timer input capture always monitors the state of the pin.

DDRT[7:0] — Data Direction Port T

1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

Address Offset: $__03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-4 Port T Reduced Drive Register (RDRT)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port T output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRT[7:0] — Reduced Drive Port T

1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__04

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-5 Port T Pull Device Enable Register (PERT)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERT[7:0] — Pull Device Enable Port T

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__05

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-6 Port T Polarity Select Register (PPST)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPST[7:0] — Pull Select Port T

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

3.3.2 Port S Registers

Address Offset: $__08

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
SPI/SCI	$\overline{SS0}$	SCK0	MOSI0	MISO0	TXD1	RXD1	TXD0	RXD0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-7 Port S I/O Register (PTS)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The SPI pins (PS[7:4]) configuration is determined by several status bits in the SPI module. *See chapter SPI for details*.
The SCI ports associated with transmit pins 3 and 1 are configured as outputs if the transmitter is enabled. The SCI pins associated with receive pins 2 and 0 are configured as inputs if the receiver is enabled. *See chapter SCI for details*.

Address Offset: $__09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-8 Port S Input Register (PTIS)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

Address Offset:$__0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-9 Port S Data Direction Register (DDRS)

Read:Anytime.

Write:Anytime.

This register configures each port S pin as either input or output
If SPI is enabled, the SPI determines the pin direction. *For details see SPI specification.*
If the associated SCI transmit or receive channel is enabled this register has no effect on the pins. The pin is forced to be an output if a SCI transmit channel is enabled, it is forced to be an input if the SCI receive channel is enabled.
The DDRS bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRS[7:0] — Data Direction Port S
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTS or PTIS registers, when changing the DDRS register.

Address Offset: $__0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-10 Port S Reduced Drive Register (RDRS)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port S output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRS[7:0] — Reduced Drive Port S

1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset:	1	1	1	1	1	1	1	1

= Reserved or unimplemented

Figure 3-11 Port S Pull Device Enable Register (PERS)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERS[7:0] — Pull Device Enable Port S

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-12 Port S Polarity Select Register (PPSS)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSS[7:0] — Pull Select Port S

1 = A pull-down device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input.

0 = A pull-up device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input or as wired-or output.

Address Offset: $__0E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-13 Port S Wired-Or Mode Register (WOMS)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. It applies also to the SPI and SCI outputs and allows a multipoint connection of several serial modules. This bit has no influence on pins used as inputs.

WOMS[7:0] — Wired-Or Mode Port S

1 = Output buffers operate as open-drain outputs.

0 = Output buffers operate as push-pull outputs.

3.3.3 Port M Registers

Address Offset: $__10

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
BF:	BF_PSLM	BF_PERR	BF_PROK	BF_PSYN	TX_BF	RX_BF		
CAN:	TXCAN4	RXCAN4	TXCAN0	RXCAN0	TXCAN1	RXCAN1	TXCAN0	RXCAN0
CAN:			TXCAN4	RXCAN4	TXCAN0	RXCAN0		
SPI			SCK0	MOSI0	SS0	MISO0		
J1850							TXBDLC	RXBDLC
Reset	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-14 Port M I/O Register (PTM)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

The ByteFlight Function takes precedence over general purpose I/O function if the ByteFlight module and the status outputs are enabled. *See Chapter ByteFlight.*
The CAN function (TXCAN and RXCAN) takes precedence over the general purpose I/O function if the associated CAN module is enabled. *See Chapter CAN.*
The BDLC function takes precedence over the general purpose I/O function associated if enabled. *See Chapter BDLC.*
If ByteFlight is enabled it takes highest precedence followed by CAN followed by BDLC.

Address Offset: $__11

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-15 Port M Input Register (PTIM)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Address Offset: $__12

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRM7	DDRM6	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-16 Port M Data Direction Register (DDRM)

Read:Anytime.

Write:Anytime.

This register configures each port M pin as either input or output.
The ByteFlight/CAN/BDLC forces the I/O state to be an output for each port line associated with an enabled output (TX_BF, BF_PSYN, BF_PROK, BF_PERR, BF_SLM, TXCAN[4,1,0], TXBDLC). It also forces the I/O state to be an input for each port line associated with an enabled input (RX_BF, RXCAN[4,1,0], RXBDLC). In those cases the data direction bits will not change.
The DDRM bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRM[7:0] — Data Direction Port M
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTM or PTIM registers, when changing the DDRM register.

Address Offset: $__13

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-17 Port M Reduced Drive Register (RDRM)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port M output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRM[7:0] — Reduced Drive Port M
1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__14

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-18 Port M Pull Device Enable Register (PERM)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset no pull device is enabled.

PERM[7:0] — Pull Device Enable Port M

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__15

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-19 Port M Polarity Select Register (PPSM)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin. If ByteFlight is active a pull-up device can be activated on the RX_BF input but not a pull-down; if CAN is active a pull-up device can be activated on the RXCAN[3:0] inputs, but not a pull-down. If BDLC is active a pull-down device can be activated on the RXBDLC pin but not a pull-up.

PPSM[7:0] — Pull Select Port M

1 = A pull-down device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as a general purpose or BDLC input but not as RXCAN.

0 = A pull-up device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as general purpose, ByteFlight or RXCAN input but not as BDLC.

Address Offset: $__16

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-20 Port M Wired-Or Mode Register (WOMM)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. It applies also to the ByteFlight, CAN and BDLC outputs and allows a multipoint connection of several serial modules. This bit has no influence on pins used as inputs.

WOMM[7:0] — Wired-Or Mode Port M

1 = Output buffers operate as open-drain outputs.

0 = Output buffers operate as push-pull outputs.

Address Offset: $__17

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-21 Module Routing Register (MODRR)

Read:Anytime.

Write:Anytime.

This register configures the re-routing of CAN0, CAN4, SPI0 and SPI1 on defined port pins.

MODRR[1:0] — CAN0 Routing

Table 3-3 CAN0 Routing

MODRR[1]	MODRR[0]	RXCAN0	TXCAN0
0	0	PM0	PM1

Table 3-3 CAN0 Routing

MODRR[1]	MODRR[0]	RXCAN0	TXCAN0
0	1	PM2	PM3
1	0	PM4	PM5
1	1	Reserved	

MODRR[3:2] — CAN4 Routing

Table 3-4 CAN4 Routing

MODRR[3]	MODRR[2]	RXCAN4	TXCAN4
0	0	PJ6	PJ7
0	1	PM4	PM5
1	0	PM6	PM7
1	1	Reserved	

MODRR[4] — SPI0 Routing

Table 3-5 SPI0 Routing

MODRR[4]	MISO0	MOSI0	SCK0	$\overline{SS0}$
0	PS4	PS5	PS6	PS7
1	PM2	PM4	PM5	PM3

MODRR[5] — SPI1 Routing

Table 3-6 SPI1 Routing

MODRR[5]	MISO1	MOSI1	SCK1	$\overline{SS1}$
0	PP0	PP1	PP2	PP3
1	PH0	PH1	PH2	PH3

3.3.4 Port P Registers

Address Offset: $__18

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
PWM:	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
SPI:					SS1	SCK1	MOSI1	MISO1
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-22 Port P I/O Register (PTP)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The PWM function takes precedence over the general purpose I/O function if the associated PWM channel is enabled. While channels 6-0 are output only if the respective channel is enabled, channel 7 can be PWM output or input if the shutdown feature is enabled. *See Chapter PWM.*
The SPI function takes precedence over the general purpose I/O function associated with if enabled. *See Chapter SPI.*
If both PWM and SPI are enabled the PWM functionality takes precedence.

Address Offset: $__19

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-23 Port P Input Register (PTIP)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be also used to detect overload or short circuit conditions on output pins.

Address Offset: $__1A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-24 Port P Data Direction Register (DDRP)

Read:Anytime.

Write:Anytime.

This register configures each port P pin as either input or output.
If the associated PWM channel or SPI module is enabled this register has no effect on the pins.
The PWM forces the I/O state to be an output for each port line associated with an enabled PWM7-0 channel. Channel 7 can force the pin to input if the shutdown feature is enabled.
If a SPI module is enabled, the SPI determines the pin direction. *For details see SPI specification.*
The DDRM bits revert to controlling the I/O direction of a pin when the associated PWM channel is disabled.

DDRP[7:0] — Data Direction Port P

1 = Associated pin is configured as output.

0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTP or PTIP registers, when changing the DDRP register.

Address Offset: $__1B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-25 Port P Reduced Drive Register (RDRP)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port P output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRP[7:0] — Reduced Drive Port P

1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__1C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-26 Port P Pull Device Enable Register (PERP)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERP[7:0] — Pull Device Enable Port P

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__1D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-27 Port P Polarity Select Register (PPSP)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSP[7:0] — Polarity Select Port P

1 = Rising edge on the associated port P pin sets the associated flag bit in the PIFP register.A pull-down device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as input.

0 = Falling edge on the associated port P pin sets the associated flag bit in the PIFP register.A pull-up device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as input.

Address Offset: $__1E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-28 Port P Interrupt Enable Register (PIEP)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port P.

PIEP[7:0] — Interrupt Enable Port P

1 = Interrupt is enabled.

0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__1F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-29 Port P Interrupt Flag Register (PIFP)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSP register. To clear this flag, write “1” to the corresponding bit in the PIFP register. Writing a “0” has no effect.

PIFP[7:0] — Interrupt Flags Port P

1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.

0 = No active edge pending.
Writing a “0” has no effect.

3.3.5 Port H Registers

Address Offset:$__20

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
SPI					$\overline{SS1}$	SCK1	MOSI1	MISO1
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-30 Port H I/O Register (PTH)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

The SPI function takes precedence over the general purpose I/O function associated with if enabled. *Refer to SPI Block Guide for details.*

Address Offset: $__21

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-31 Port H Input Register (PTIH)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Address Offset: $__22

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRH7	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-32 Port H Data Direction Register (DDRH)

Read:Anytime.

Write:Anytime.

This register configures each port H pin as either input or output.

DDRH[7:0] — Data Direction Port H

1 = Associated pin is configured as output.

0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTH or PTIH registers, when changing the DDRH register.

Address Offset: $__23

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-33 Port H Reduced Drive Register (RDRH)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port H output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRH[7:0] — Reduced Drive Port H

1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__24

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-34 Port H Pull Device Enable Register (PERH)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERH[7:0] — Pull Device Enable Port H

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__25

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-35 Port H Polarity Select Register (PPSH)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSH[7:0] — Polarity Select Port H

1 = Rising edge on the associated port H pin sets the associated flag bit in the PIFH register. A pull-down device is connected to the associated port H pin, if enabled by the associated bit in register PERH and if the port is used as input.

0 = Falling edge on the associated port H pin sets the associated flag bit in the PIFH register. A pull-up device is connected to the associated port H pin, if enabled by the associated bit in register PERH and if the port is used as input.

Address Offset: $__26

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-36 Port H Interrupt Enable Register (PIEH)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port H.

PIEH[7:0] — Interrupt Enable Port H

1 = Interrupt is enabled.

0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__27

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-37 Port H Interrupt Flag Register (PIFH)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSH register. To clear this flag, write “1” to the corresponding bit in the PIFH register. Writing a “0” has no effect.

PIFH[7:0] — Interrupt Flags Port H

1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.

0 = No active edge pending.
Writing a “0” has no effect.

3.3.6 Port J Registers

Address Offset: $__28

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTJ7	PTJ6	0	0	0	0	PTJ1	PTJ0
Write:								
CAN:	TXCAN4	RXCAN4						
IIC:	SCL	SDA						
Reset:	0	0	-	-	-	-	0	0

= Reserved or unimplemented

Figure 3-38 Port J I/O Register (PTJ)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The CAN function (TXCAN and RXCAN) takes precedence over the general purpose I/O function if the associated CAN module is enabled. *See Chapter CAN.*

The IIC function takes precedence over the general purpose I/O function associated with if enabled. If both CAN4 and IIC are enabled the CAN functionality takes precedence. *See Chapter IIC.* If the IIC module is enabled the SDA and SCL outputs are configured as open-drain outputs.

Address Offset: $__29

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIJ7	PTIJ6	0	0	0	0	PTIJ1	PTIJ0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-39 Port J Input Register (PTIJ)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be used to detect overload or short circuit conditions on output pins.

Address Offset: $__2A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDRJ7	DDRJ6	0	0	0	0	DDRJ1	DDRJ0
Write:								
Reset:	0	0	-	-	-	-	0	0

= Reserved or unimplemented

Figure 3-40 Port J Data Direction Register (DDRJ)

Read:Anytime.

Write:Anytime.

This register configures each port J pin as either input or output.
The CAN forces the I/O state to be an output on PJ7 (TXCAN4) and an input on pin PJ6 (RXCAN4). The IIC takes control of the I/O if enabled. In these cases the data direction bits will not change. The DDRJ bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRJ[7:6][1:0] — Data Direction Port J

1 = Associated pin is configured as output.

0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTJ or PTIJ registers, when changing the DDRJ register.

Address Offset: $__2B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RDRJ7	RDRJ6	0	0	0	0	RDRJ1	RDRJ0
Write:								
Reset:	0	0	-	-	-	-	0	0

= Reserved or unimplemented

Figure 3-41 Port J Reduced Drive Register (RDRJ)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port J output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRJ[7:6][1:0] — Reduced Drive Port J

1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__2C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PERJ7	PERJ6	0	0	0	0	PERJ1	PERJ0
Write:								
Reset:	1	1	-	-	-	-	1	1

= Reserved or unimplemented

Figure 3-42 Port J Pull Device Enable Register (PERJ)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERJ[7:6][1:0] — Pull Device Enable Port J

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__2D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PPSJ7	PPSJ6	0	0	0	0	PPSJ1	PPSJ0
Write:								
Reset:	0	0	-	-	-	-	0	0

= Reserved or unimplemented

Figure 3-43 Port J Polarity Select Register (PPSJ)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSJ[7:6][1:0] — Polarity Select Port J

1 = Rising edge on the associated port J pin sets the associated flag bit in the PIFJ register. A pull-down device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as input.

0 = Falling edge on the associated port J pin sets the associated flag bit in the PIFJ register. A pull-up device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as general purpose input or as IIC port.

Address Offset: $__2E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PIEJ7	PIEJ6	0	0	0	0	PIEJ1	PIEJ0
Write:								
Reset:	0	0	-	-	-	-	0	0

= Reserved or unimplemented

Figure 3-44 Port J Interrupt Enable Register (PIEJ)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port J.

PIEJ[7:6][1:0] — Interrupt Enable Port J

1 = Interrupt is enabled.

0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__2F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PIFJ7	PIFJ6	0	0	0	0	PIFJ1	PIFJ0
Write:								
Reset:	0	0	-	-	-	-	0	0

= Reserved or unimplemented

Figure 3-45 Port J Interrupt Flag Register (PIFJ)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSJ register. To clear this flag, write “1” to the corresponding bit in the PIFJ register. Writing a “0” has no effect.

PIFJ[7:6][1:0] — Interrupt Flags Port J

1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.

0 = No active edge pending.
Writing a “0” has no effect.

Section 4 Functional Description

4.1 General

Each pin can act as general purpose I/O. In addition the pin can act as an output from a peripheral module or an input to a peripheral module. **Table 4-1** summarizes the priority in case of multiple enabled modules trying to control a shared port.

Table 4-1 Summary of Functional Priority

Port	Priority[1]
T	ECT > GPIO
S	SCI, SPI > GPIO
M	ByteFlight > CAN0 > BDLC > GPIO ByteFlight > CAN1 > (routed) CAN0 > (routed) SPI0 > GPIO ByteFlight > (routed) CAN0 > (routed) CAN4 > (routed) SPI0 > GPIO
P	PWM > SPI > GPIO
H	SPI > GPIO
J	CAN4 > IIC > GPIO
A	Refer to section Bus Control and Input/Output
B	
E	
K	
BKGD pin	

NOTES:
1. Highest priority >... > lowest priority

A set of configuration registers is common to all ports. All registers can be written at any time, however a specific configuration might not become active.

Example:

Selecting a pull-up resistor. This resistor does not become active while the port is used as a push-pull output.

4.1.1 I/O register

This register holds the value driven out to the pin if the port is used as a general purpose I/O.

Writing to this register has only an effect on the pin if the port is used as general purpose output. When reading this address, the value of the pins is returned if the data direction register bits are set to 0.

If the data direction register bits are set to 1, the contents of the I/O register is returned. This is independent of any other configuration (**Figure 4-1**).

4.1.2 Input register

This is a read-only register and always returns the value of the pin (**Figure 4-1**).

4.1.3 Data direction register

This register defines whether the pin is used as an input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (**Figure 4-1**).

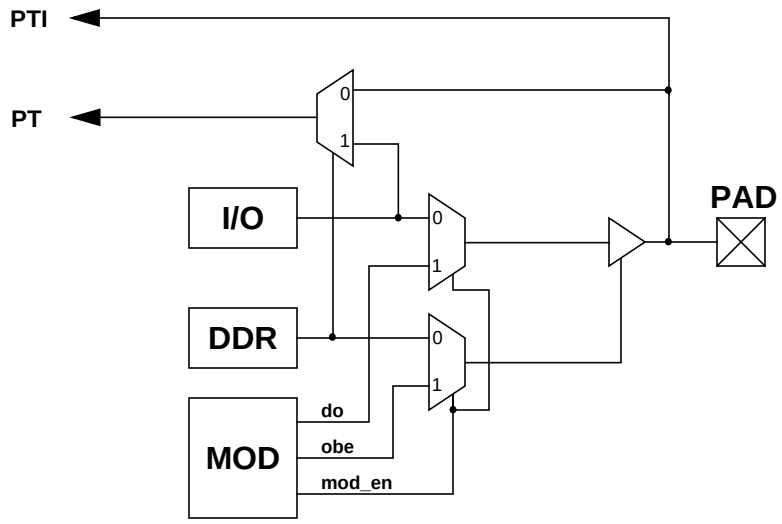

Figure 4-1 Illustration of I/O pin functionality

4.1.4 Reduced drive register

If the port is used as an output the register allows the configuration of the drive strength.

4.1.5 Pull device enable register

This register turns on a pull-up or pull-down device.

It becomes only active if the pin is used as an input or as a wired-or output.

4.1.6 Polarity select register

This register selects either a pull-up or pull-down device if enabled.

It becomes only active if the pin is used as an input. A pull-up device can be activated if the pin is used as a wired-or output.

4.2 Port T

This port is associated with the Enhanced Capture Timer module.

In all modes, port T pins PT[7:0] can be used for either general-purpose I/O, or with the channels of the Enhanced Capture Timer.

During reset, port T pins are configured as high-impedance inputs.

4.3 Port S

This port is associated with the serial SCI and SPI modules.

In all modes, port S pins PS[7:0] can be used either for general-purpose I/O, or with the SCI and SPI subsystems.

During reset, port S pins are configured as inputs with pull-up.

The SPI pins can be re-routed. Refer to **4.4.1**.

4.4 Port M

This port is associated with the Byteflight, J1850 and 3 CAN modules.

In all modes, port M pins PM[7:0] can be used for either general purpose I/O, or with the CAN and J1850 subsystems.

By default, pins PM0 and PM1 are shared between the CAN0 and the BDLC (J1850) module. If CAN0 is enabled the pins become CAN transmit and receive pins. If BLDC is enabled and CAN0 is disabled, pins become active BDLC transmit and receive pins. Pins PM2-7 are shared amongst ByteFlight, CAN0, 1 and 4, and SPI0.

During reset, port M pins are configured as high-impedance inputs.

The CAN pins can be re-routed. Refer to **4.4.1**.

4.4.1 Module Routing Register

This register allows to re-route the CAN0, CAN4, SPI0 and SPI1 pins to predefined pins.

NOTE: *The purpose of the Module Routing Register is to provide maximum flexibility for future derivatives of the MC9S12DT128 with a lower number of MSCAN12 and SPI modules.*

Table 4-2 Implemented modules on derivatives

Number of modules	MSCAN modules			SPI modules	
	CAN0	CAN1	CAN4	SPI0	SPI1
3	X	X	X	X	X
2	X	-	X	X	X
1	X	-	-	X	-

The ByteFlight module has highest priority if enabled. The CAN0 transmit and receive pin can be routed to PM[3:2] or PM[5:4] if ByteFlight and CAN1 are disabled, respectively. PM[5:4] or PM[7:6] can be taken by CAN4, if ByteFlight is disabled. CAN0 has priority over CAN4 if both modules are trying to access PM[5:4] at the same time.

The SPI0 pins can be routed to PM[5:2] if no other module uses these pins. If the SPI0 module is routed on PM[5:4] and used in bidirectional master mode with disabled $\overline{SS}$ output, PM[3:2] are free to be used with ByteFlight, CAN or GPIO.

The SPI1 pins can be routed to PH[3:0].

4.5 Port P

This port is associated with the PWM and one SPI modules.

In all modes, port P pins PP[7:0] can be used for either general purpose I/O, or with the PWM and SPI subsystems.

The pins are shared between the PWM channels and the SPI1 module. If the PWM is enabled the pins become PWM output channels with the exception of pin 7 which can be PWM input or output. If SPI1 is enabled and PWM is disabled, the respective pin configuration is determined by several status bits in the SPI module.

During reset, port P pins are configured as high-impedance inputs.

The SPI pins can be re-routed. Refer to **4.4.1**.

Port P offers 8 I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All 8 bits/pins share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. This external interrupt feature is capable to wake up the CPU when it is in STOP or WAIT mode.

A digital filter on each pin prevents pulses (**Figure 4-3**) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (**Figure 4-2** and **Table 4-3**).

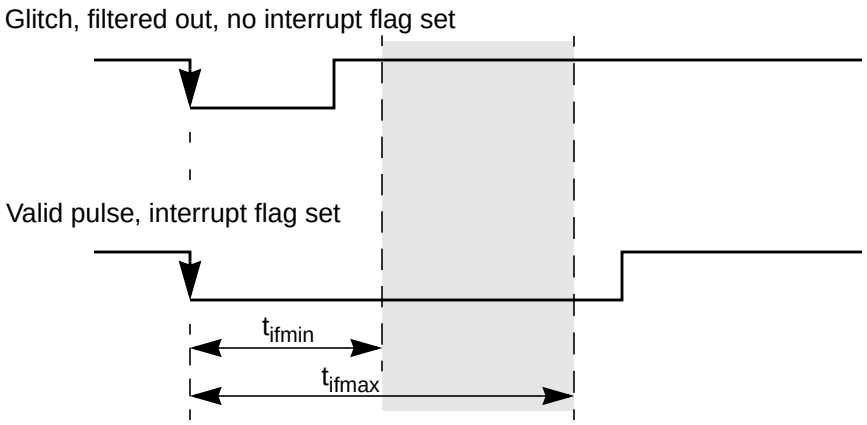

Figure 4-2 Interrupt Glitch Filter on Port P, H and J (PPS=0)

Table 4-3 Pulse Detection Criteria

Pulse	Mode			
	$\overline{STOP}$		STOP[1]	
		Unit		Unit
Ignored	t_{pulse} <= 3	bus clocks	t_{pulse} <= 3.2	µs
Uncertain	3 < t_{pulse} < 4	bus clocks	3.2 < t_{pulse} < 10	µs
Valid	t_{pulse} >= 4	bus clocks	t_{pulse} >= 10	µs

NOTES:
1. These values include the spread of the oscillator frequency over temperature, voltage and process.

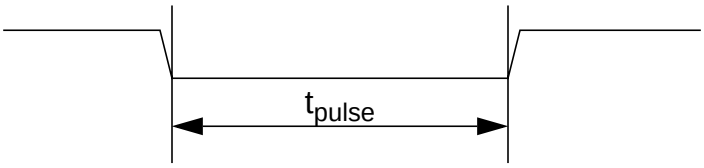

Figure 4-3 Pulse Illustration

A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level directly or indirectly.

The filters are continuously clocked by the bus clock in RUN and WAIT mode. In STOP mode the clock is generated by a single RC oscillator in the Port Integration Module. To maximize current saving the RC oscillator runs only if the following condition is true on any pin:

Sample count <= 4 and port interrupt enabled (PIE=1) and port interrupt flag not set (PIF=0).

4.6 Port H

Port H offers 8 I/O ports with the same interrupt features as port P.

During reset, port H pins are configured as high-impedance inputs.

Port H pins can be used with the routed SPI1 module. Refer to **4.4.1**.

4.7 Port J

This port is associated with the CAN4 and the IIC module.

In all modes, port J pins PJ[7:6] and PJ[1:0] can be used for either general purpose I/O, or with the CAN and IIC subsystems.

By default, pins PJ6 and PJ7 are shared between the CAN4 and the IIC module. If CAN4 is enabled the pins become CAN transmit and receive pins. If IIC is enabled and CAN4 is disabled, the pins become IIC open-drain output pins.

During reset, port J pins are configured as inputs with pull-up.

The CAN pins can be re-routed. Refer to **4.4.1**.

Port J offers 4 I/O ports with the same interrupt features as port P.

4.8 Port A, B, E, K, and BKGD pin

All port and pin logic is located in the core module. Refer to section Bus Control and Input/Output.

4.9 80 Pin QFP bond-out versions

In case the port pins are not bonded out in the chosen package the user should initialize the registers to be inputs with enabled pull resistance to avoid excess current consumption. This applies to the following pins:

- All port K and H.
- Port PP6, PJ1-0,
- PM7-4, Port PS7-2 depending on the package option.
- PAD15-8. The A/D converter associated with those pins (ATD1) should be disabled.

4.10 External Pin Descriptions

All ports start up as general purpose inputs on reset.

4.11 Low Power Options

4.11.1 Run Mode

No low power options exist for this module in run mode.

4.11.2 Wait Mode

No low power options exist for this module in wait mode.

4.11.3 Stop Mode

All clocks are stopped. There are however asynchronous paths to generate interrupts from STOP on port P, H and J.

Section 5 Resets

5.1 General

The reset values of all registers are given in the Register Description in section **3.3**.

5.2 Reset Initialization

All registers including the data registers get set/reset asynchronously. **Table 5-1** summarizes the port properties after reset initialization.

Table 5-1 Port Reset State Summary

Port	Reset States				
	Data Direction	Pull Mode	Red. Drive	Wired-Or Mode	Inter-rupt
T	input	hiz	disabled	n/a	n/a
S	input	pull-up	disabled	disabled	n/a
M	input	hiz	disabled	disabled	n/a
P	input	hiz	disabled	n/a	disabled
H	input	hiz	disabled	n/a	disabled
J	input	pull-up	disabled	n/a	disabled
A	Refer to section Bus Control and Input/Output				
B					
E					
K					
BKGD pin					

Section 6 Interrupts

6.1 General

Port P, H and J generate a separate edge sensitive interrupt if enabled.

6.2 Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Port P	PIFP[7:0]	PIEP[7:0]	I Bit
Port H	PIFH[7:0]	PIEH[7:0]	I Bit
Port J	PIFJ[7:6] PIFJ[1:0]	PIFJ[7:6] PIFJ[1:0]	I Bit

Table 6-1 Port Integration Module Interrupt Sources

NOTE: *Vector addresses and their relative interrupt priority are determined at the MCU level.*

6.3 Recovery from STOP

This module can generate wake-up interrupts from STOP on port P, H and J. For other sources of external interrupts refer to the respective module specification.

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