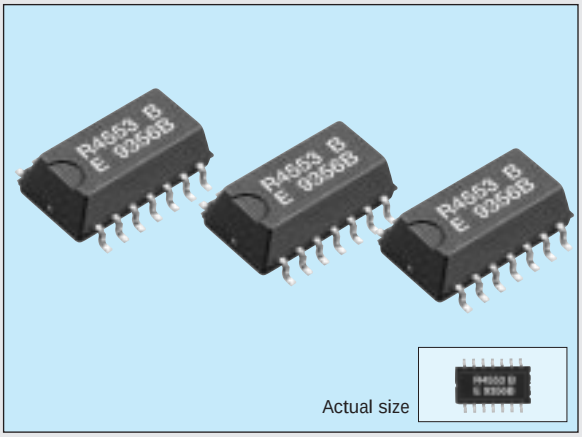
SERIAL-INTERFACE REAL TIME CLOCK MODULE WITH SRAM

RTC-4553

Product number (please refer to page 2)

Q4145535xxxxx00

- Built-in crystal unit allows adjustment-free efficient operation.
- Automatic calendar function (year, month, day, day of the week, hour, minute, second).
- Automatic leap year correction.
- Builtin 30 x 4-bit S-RAM.
- Reference pulse output. (1024 Hz, 1/10 Hz)



The details are mentioned in the application manual.

http://www.epsondevice.com

Specifications (characteristics)

Absolute Max. rating

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V_{DD}	V_{DD}-GND	-0.3	+6.0	V
Input voltage	V_{IN}	S_{IN}, $\overline{SCK}$, $\overline{WR}$, $\overline{CS_0}$, CS_1		V_{DD}+0.3	
Output voltage	V_{OUT}	S_{OUT}, $\overline{T_{POUT}}$			
Storage temperature	T_{STG}	Stored as bare product after unpacking	-55	+125	°C

Operating range

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}	—	2.7	5.0	5.5	V
Clock voltage	V_{CLK}	—	2.0	—	5.5	V
Operating temperature	T_{OPR}	No condensation	-30	—	+70	°C

Frequency characteristics

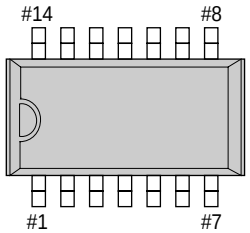
Item	Symbol	Condition		Range	Unit
Frequency tolerance	Δf/fo	Ta=+25 °C, V_{DD}=5 V	AA	5±5	x 10^{-6}
			A	5±10	
			B	5±20	
Oscillation start-up time	T_{sta}	Ta=+25 °C		3.0 Max.	s
Frequency temperature characteristics	T_{op}	Ta=-10 °C to +70 °C, V_{DD}=5 V Reference at +25 °C		+10 -120	x 10^{-6}
Frequency voltage characteristics	f/v	Ta=Fix, V_{DD}=2 V to 5.5 V Reference at 5 V		±5	
Aging	fa	Ta=+25 °C, V_{DD}=5 V, first year			x 10^{-6}/year

DC characteristics

(GND=0 V, V_{DD}=5 V ± 10 %, Ta=-30 °C to +70 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	I_{DD1}	$\overline{SCK}$=500 kHz	—	—	100	µA
	I_{DD2}	$\overline{SCK}$=O Hz		1.0	3.0	
Output voltage	V_{OH}	I_{OH}=-400 µA	V_{DD}-04	—	—	V
	V_{OL}	I_{OL}=1.6 mA	—	—	0.4	
Off leak current	I_{OZH}	V_{OUT}=5.5 V	-2.0	—	2.0	µA
	I_{OZL}	V_{OUT}=0 V				
Input voltage	V_{IH}	—	4/5 V_{DD}	—	—	V
	V_{IL}		—	—	1/5 V_{DD}	
Input current	I_{IH}	V_{IN}=5.5 V	-2.0	—	2.0	µA
	I_{IL}	V_{IN}=0 V				

Terminal connection



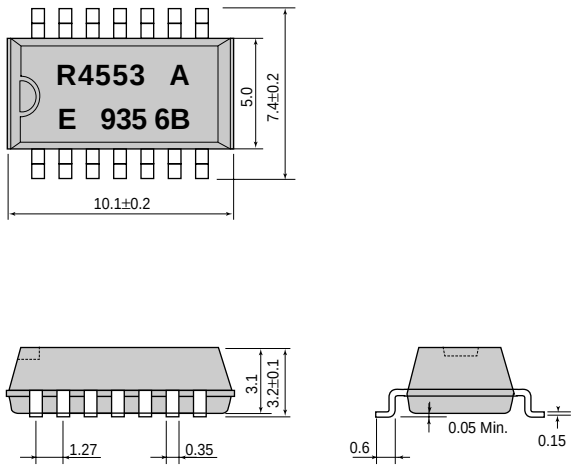
No.	Pin terminal	No.	Pin terminal
1	GND	14	$\overline{TP_{OUT}}$
2	$\overline{WR}$	13	S_{OUT}
3	S_{IN}	12	CS_1
4	$\overline{SCK}$	11	$\overline{CS_0}$
5	L1	10	L5
6	L2	9	L4
7	L3	8	V_{DD}

L1 to L5 are test pin. Do not connect them to any terminals.

External dimensions

(Unit: mm)

● **RTC-4553** (SOP 14-pin)



Metal may be exposed on the top or bottom of this product. This won't affect any quality, reliability or electrical spec.

Register table

	Address				MODE 0						MODE 1				MODE 2			
					Register symbol	Counter control register					User RAM Domain 1				User RAM Domain 2			
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0	Register name	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	1-second digit register	RA_3	RA_2	RA_1	RA_0	RA_{63}	RA_{62}	RA_{61}	RA_{60}
1	0	0	0	1	S_{10}	0	S_{40}	S_{20}	S_{10}	10-second digit register	RA_7	RA_6	RA_5	RA_4	RA_{67}	RA_{66}	RA_{65}	RA_{64}
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	1-minute digit register	RA_{11}	RA_{10}	RA_9	RA_8	RA_{71}	RA_{70}	RA_{69}	RA_{68}
3	0	0	1	1	MI_{10}	0	mi_{40}	mi_{20}	mi_{10}	10-minute digit register	RA_{15}	RA_{14}	RA_{13}	RA_{12}	RA_{75}	RA_{74}	RA_{73}	RA_{72}
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	1-hour digit register	RA_{19}	RA_{18}	RA_{17}	RA_{16}	RA_{79}	RA_{78}	RA_{77}	RA_{76}
5	0	1	0	1	H_{10}	PM/AM	0	h_{20}	h_{10}	10-hour digit register	RA_{23}	RA_{22}	RA_{21}	RA_{20}	RA_{83}	RA_{82}	RA_{81}	RA_{80}
6	0	1	1	0	W	0	w_4	w_2	w_1	Day of the week digit register	RA_{27}	RA_{26}	RA_{25}	RA_{24}	RA_{87}	RA_{86}	RA_{85}	RA_{84}
7	0	1	1	1	D_1	d_8	d_4	d_2	d_1	1-day digit register	RA_{31}	RA_{30}	RA_{29}	RA_{28}	RA_{91}	RA_{90}	RA_{89}	RA_{88}
8	1	0	0	0	D_{10}	0	0	d_{20}	d_{10}	10-day digit register	RA_{35}	RA_{34}	RA_{33}	RA_{32}	RA_{95}	RA_{94}	RA_{93}	RA_{92}
9	1	0	0	1	MO_1	mo_8	mo_4	mo_2	mo_1	1-month digit register	RA_{39}	RA_{38}	RA_{37}	RA_{36}	RA_{99}	RA_{98}	RA_{97}	RA_{96}
A	1	0	1	0	MO_{10}	0	0	0	mo_{10}	10-month digit register	RA_{43}	RA_{42}	RA_{41}	RA_{40}	RA_{103}	RA_{102}	RA_{101}	RA_{100}
B	1	0	1	1	Y_1	y_8	y_4	y_2	y_1	1-year digit register	RA_{47}	RA_{46}	RA_{45}	RA_{44}	RA_{107}	RA_{106}	RA_{105}	RA_{104}
C	1	1	0	0	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	10-year digit register	RA_{51}	RA_{50}	RA_{49}	RA_{48}	RA_{111}	RA_{110}	RA_{109}	RA_{108}
D	1	1	0	1	C_1	TPS	30ADJ	CNTR	24/12	Control register 1	RA_{55}	RA_{54}	RA_{53}	RA_{52}	RA_{115}	RA_{114}	RA_{113}	RA_{112}
E	1	1	1	0	C_2	BUSY	PONC	—	*	Control register 2	RA_{59}	RA_{58}	RA_{57}	RA_{56}	RA_{119}	RA_{118}	RA_{117}	RA_{116}
F	1	1	1	1	C_3	SYSR	TEST	MS_1	MS_0	Control register 3	Same as MODE 0				Same as MODE 0			

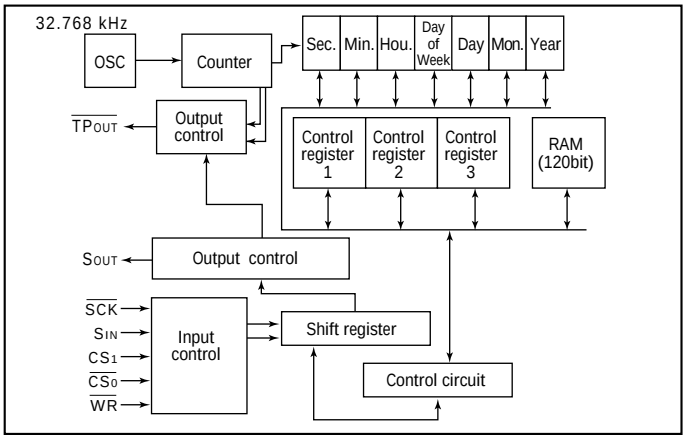
Note: * TEST bit should be "0".

AC characteristics

(Ta=-30 °C to +70 °C, V_{DD}=5 V±10 %, GND=0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
$\overline{SCK}$ input frequency	f_{CLK}	—	—	—	500	kHz
$\overline{SCK}$ "L" time	t_{WCKL}	—	1.0	—	—	µs
$\overline{SCK}$ "H" time	t_{WCKH}					
$\overline{SCK}$ pause time	t_{PS}				—	
$\overline{CS_0}$ setup time	t_{SCS}	—	0	—		
$\overline{CS_0}$ hold time	t_{HCS}		0.5			
S_{IN} data setup time	t_{SD}		0.2			
S_{IN} data Hold time	t_{HD}					
$\overline{WR}$ setup time	t_{SWR}		1.0			
$\overline{WR}$ hold time	t_{HWR}		0.5			
S_{OUT} delay time	t_{DSO}	C_L=100 pF	—	150	500	ns
$\overline{CS_0}$, and CS_1 enable to S_{OUT} output	t_{DSZ1}			—	100	
$\overline{CS_0}$ disable to S_{OUT} high Z	t_{DSZ2}					
CS_1 enable to S_{OUT} output	t_{DPZ1}					
CS_1 enable to S_{OUT} high Z	t_{DPZ2}					

Block diagram



Timing chart