

PHP/PHB/PHD66NQ03LT

TrenchMOS™ logic level FET

Rev. 04 — 9 September 2002

Product data

1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP66NQ03LT in SOT78 (TO-220AB)

PHB66NQ03LT in SOT404 (D²-PAK)

PHD66NQ03LT in SOT428 (D-PAK).

2. Features

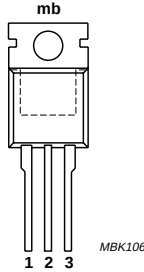
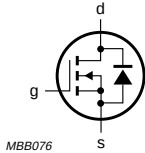
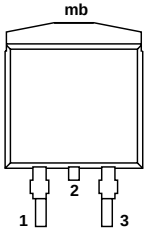
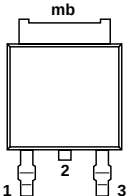
- Low on-state resistance
- Fast switching.

3. Applications

- High frequency computer motherboard DC to DC converters.

4. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 MBK106	 MBB076
2	drain (d)		
3	source (s)		
mb	mounting base, connected to drain (d)	 MBK116	 Top view MBK091
		SOT78 (TO-220AB)	SOT404 (D ² -PAK)
		SOT428 (D-PAK)	

[1] It is not possible to make connection to pin 2 of the SOT404 and SOT428 packages.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	66	A
		$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	57	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	93	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	9.1	12	mΩ
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	12.3	16	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

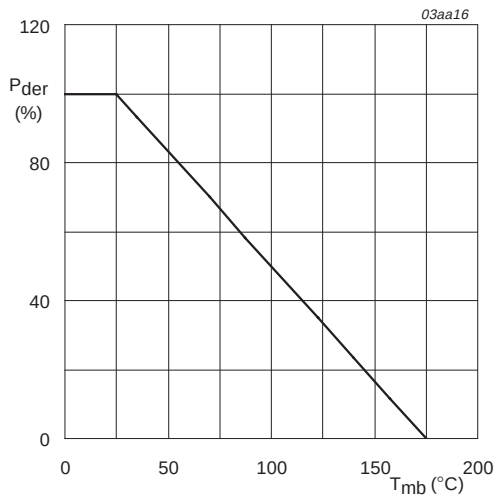
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	25	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}; \text{Figure 2 and 3}$	-	57	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V}; \text{Figure 2}$	-	40	A
		$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	66	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V}$	-	45	A
V_{GS}	gate-source voltage		-	±20	V
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}; \text{Figure 3}$	-	228	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Figure 1}$	-	93	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	57	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}; \text{pulsed}; t_p \leq 10\text{ }\mu\text{s}$	-	228	A

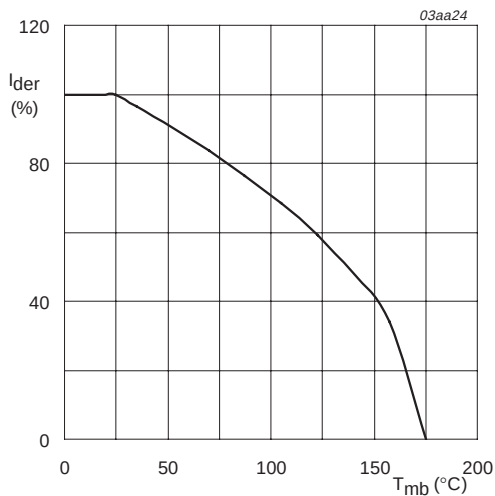
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}; t_p = 0.15\text{ ms}; V_{DD} \leq 15\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V}; \text{starting } T_j = 25\text{ °C}$	-	90	mJ
---------------	--	--	---	----	----



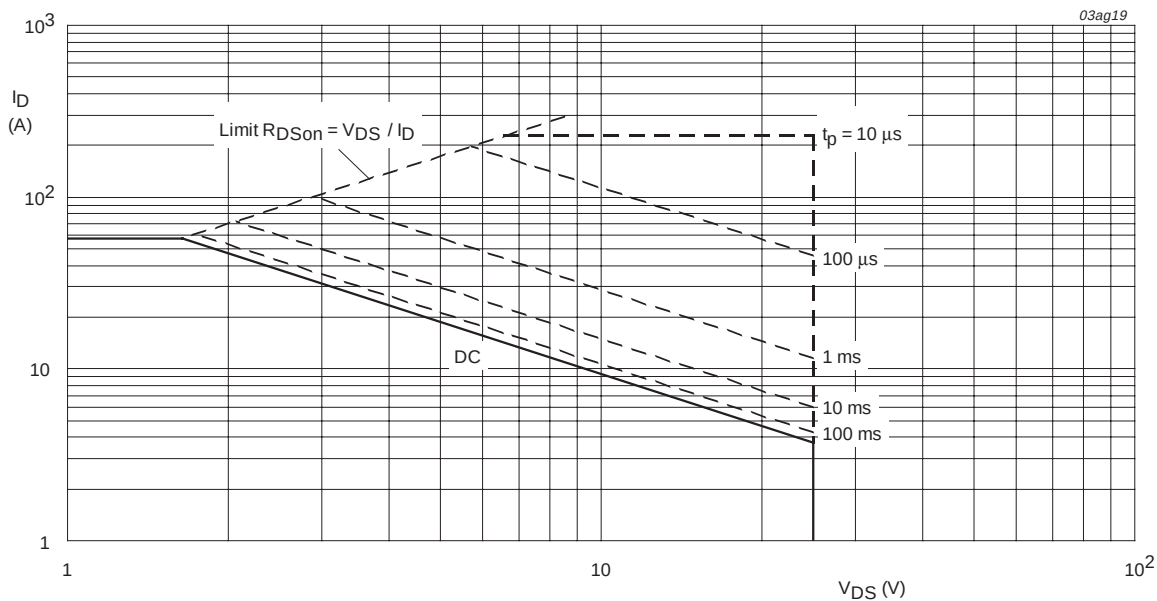
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 5 V$.

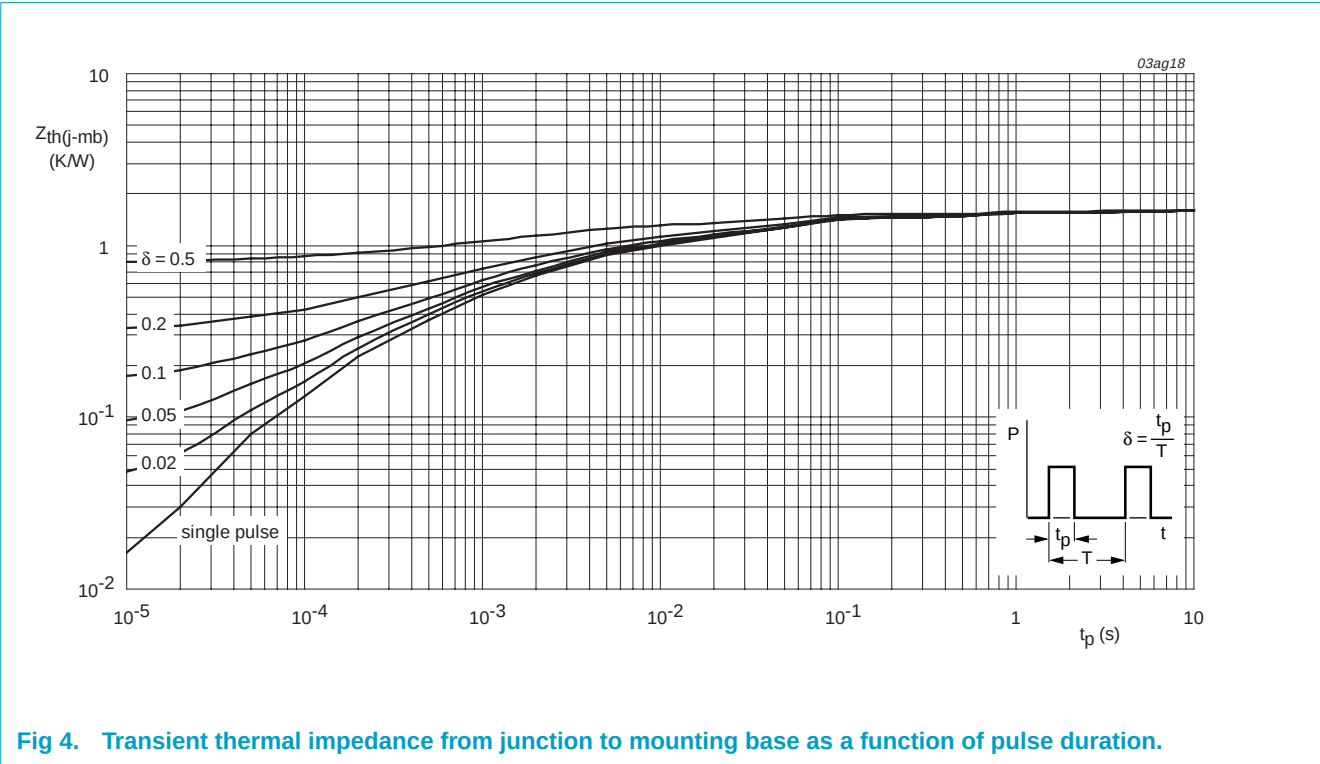
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT428	SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
	SOT404 and SOT428	SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

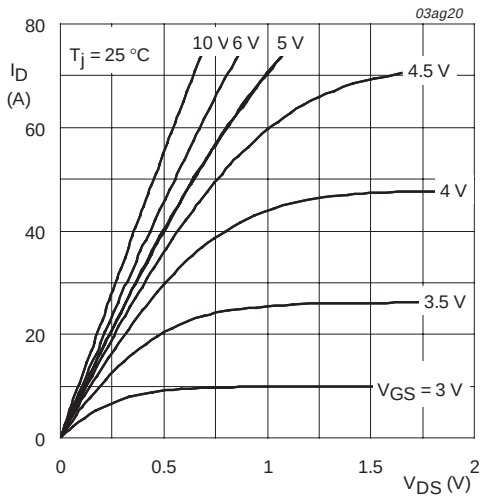
7.1 Transient thermal impedance



8. Characteristics

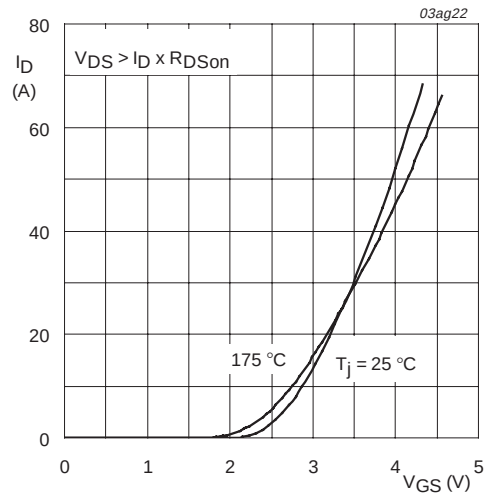
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	25	-	-	V
		$T_j = -55\text{ °C}$	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.05	10	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 5\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	12.3	16	m Ω
		$T_j = 175\text{ °C}$	-	22.1	28.8	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$				
		$T_j = 25\text{ °C}$	-	9.1	12	m Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 25\text{ V}$; $I_D = 30\text{ A}$	-	40	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 50\text{ A}$; $V_{DD} = 15\text{ V}$; $V_{GS} = 5\text{ V}$; Figure 13	-	12	-	nC
Q_{gs}	gate-source charge		-	4.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	860	-	pF
C_{oss}	output capacitance		-	330	-	pF
C_{rss}	reverse transfer capacitance		-	145	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\text{ V}$; $I_D = 25\text{ A}$; $V_{GS} = 5\text{ V}$; $R_G = 5.6\text{ }\Omega$; resistive load	-	15	25	ns
t_r	rise time		-	90	135	ns
$t_{d(off)}$	turn-off delay time		-	25	40	ns
t_f	fall time		-	25	40	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.95	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$	-	32	-	ns
Q_r	recovered charge		-	20	-	nC



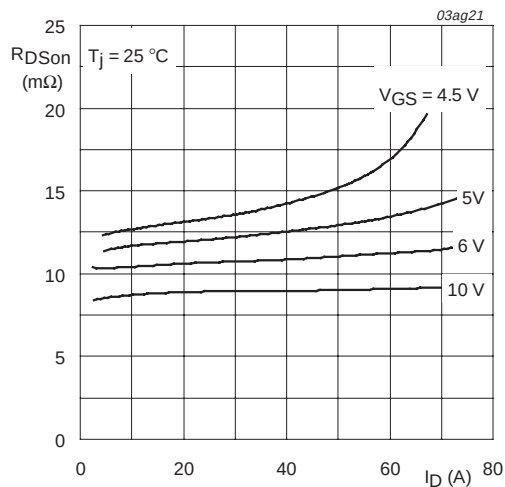
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



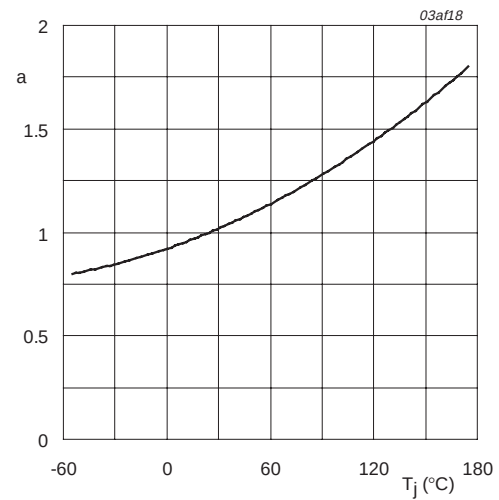
$T_j = 25\text{ }^{\circ}\text{C}$ and $175\text{ }^{\circ}\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



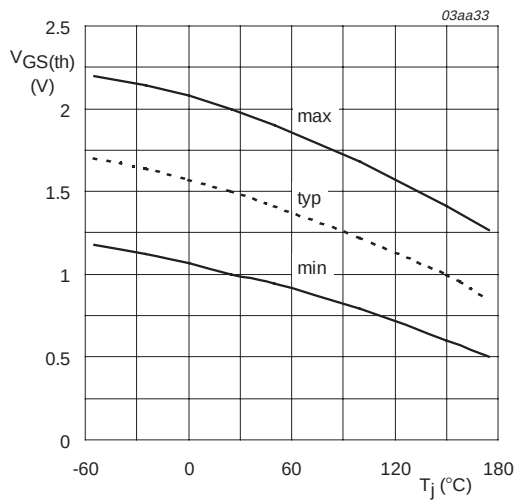
$T_j = 25\text{ }^{\circ}\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



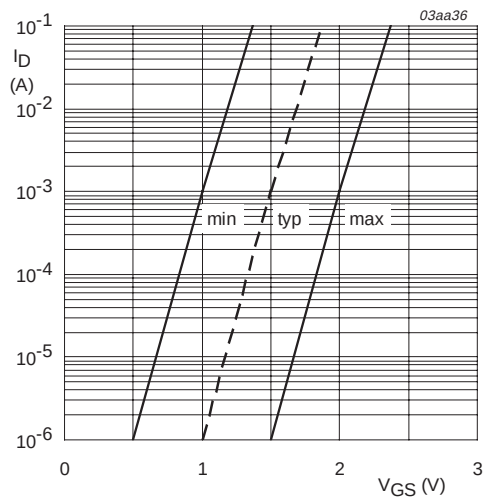
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^{\circ}\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



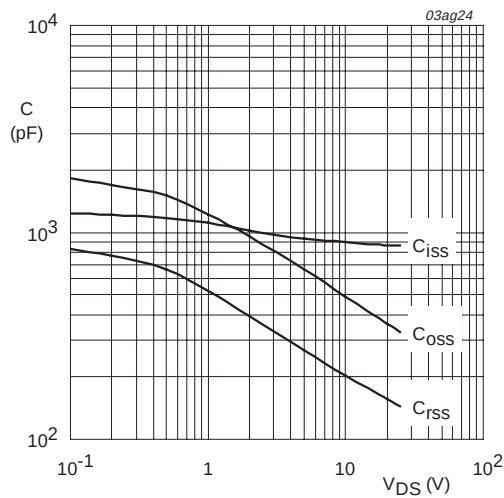
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



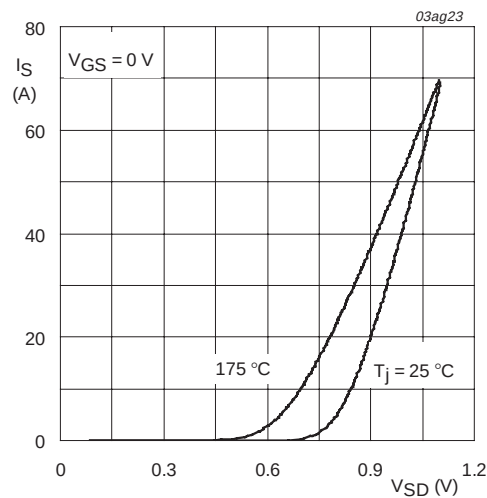
$T_j = 25 \text{ °C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



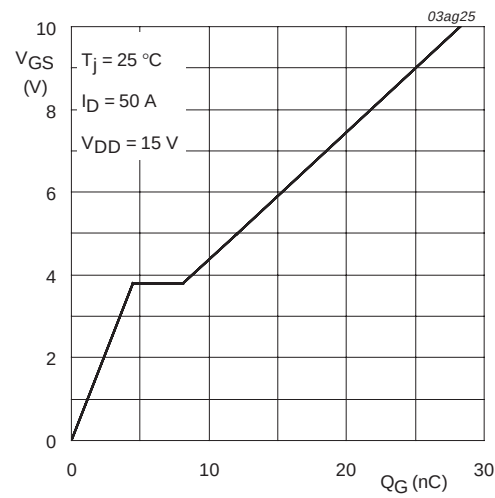
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



Tj = 25 °C and 175 °C; VGS = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



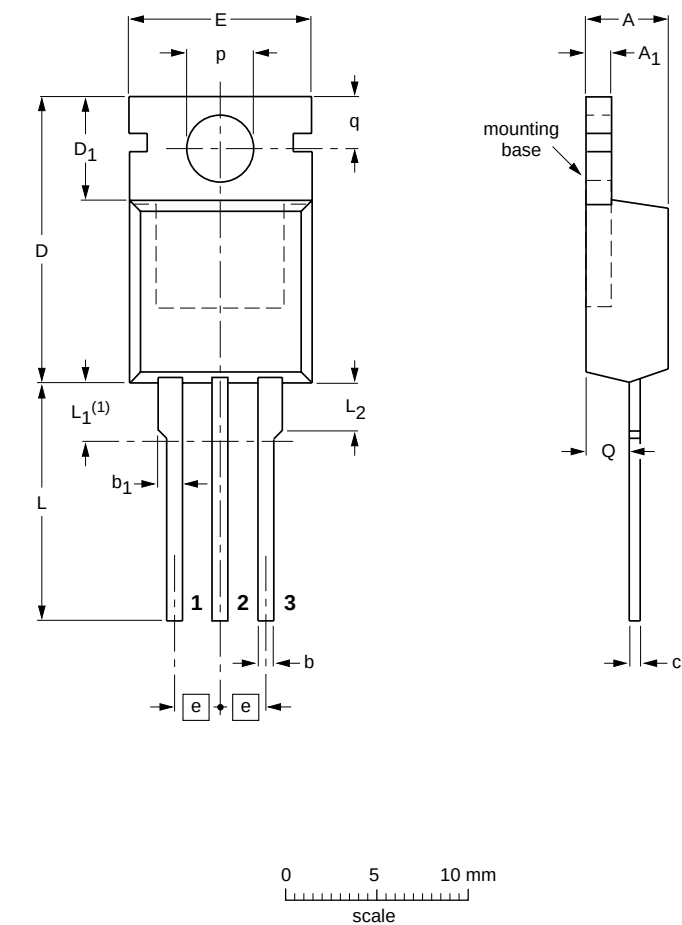
ID = 50 A; VDD = 15 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁ ⁽¹⁾	L ₂ max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

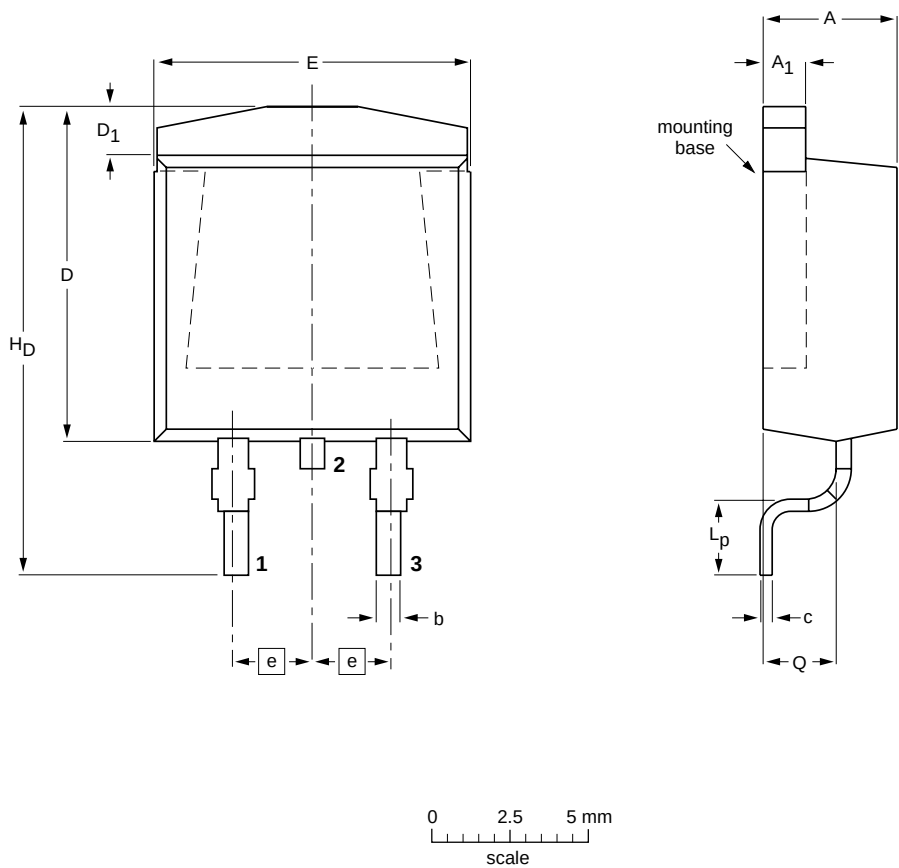
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07 01-02-16

Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						-99-06-25 01-02-12

Fig 15. SOT404 (D²-PAK).

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

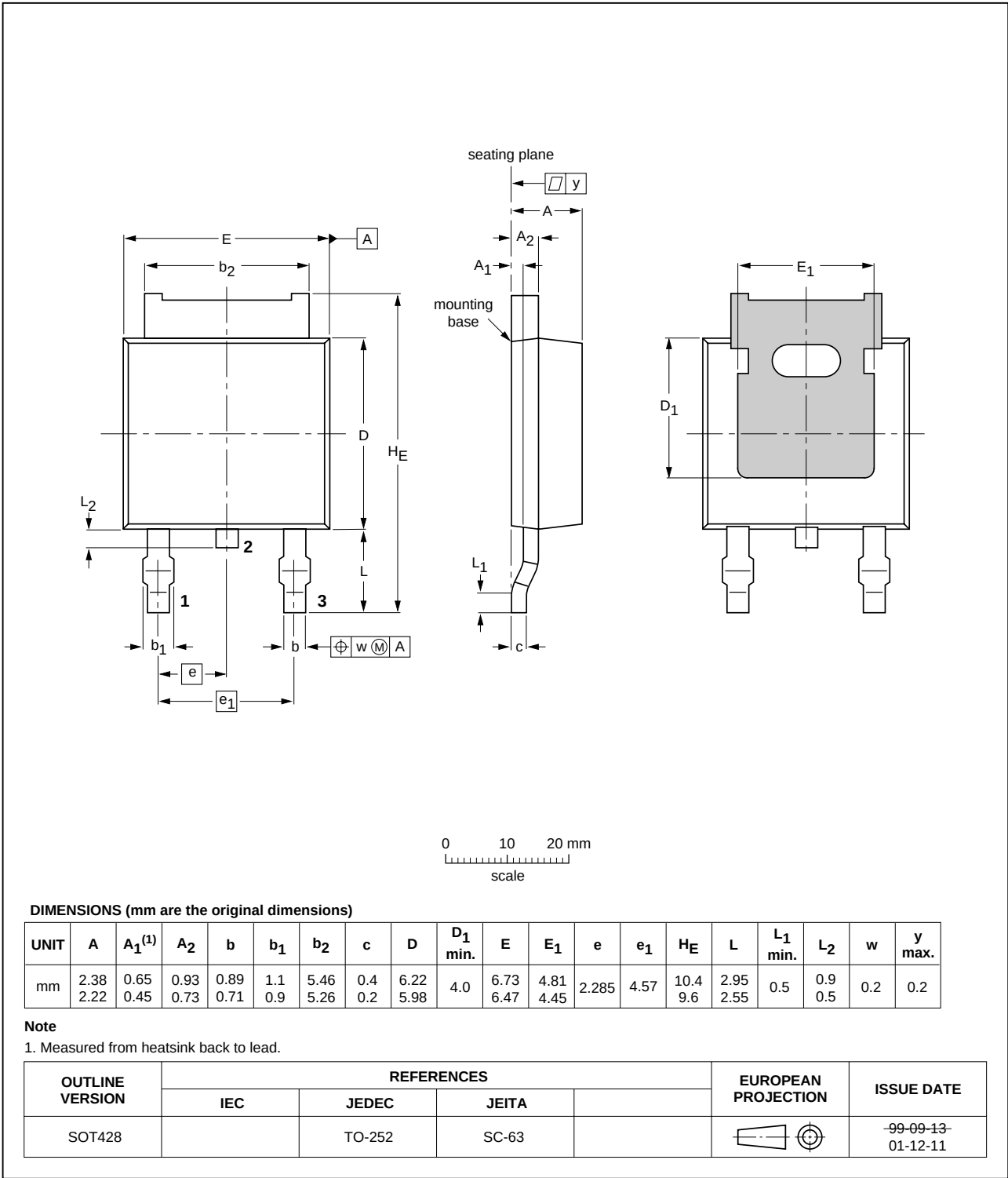


Fig 16. SOT428 (D-PAK)

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
04	20020909	-	Product data; fourth version; supersedes version of 12 March 2002. Section 6 "Limiting values" Addition of $E_{DS(AL)S}$. Graphs updated to latest standard.
03	20020312	-	Product data; third version; supersedes version of 10 December 2001. Section 6 "Limiting values" Standardized V_{GS} rating. Section 7 "Thermal characteristics" Clarification of thermal resistances table. Section 8 "Characteristics" Improved Gate charge and Capacitance.
02	20011210	-	Includes product data; second version; supersedes initial version 12 October 2001. Section 1 "Description" Correction to typing mistake in name.
01	20011012	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

13. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

14. Trademarks

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

Contents

1 Description 1

2 Features 1

3 Applications 1

4 Pinning information 1

5 Quick reference data 2

6 Limiting values 2

7 Thermal characteristics 4

7.1 Transient thermal impedance 4

8 Characteristics 5

9 Package outline 9

10 Revision history 12

11 Data sheet status 13

12 Definitions 13

13 Disclaimers 13

14 Trademarks 13



PHILIPS

Let's make things better.