MOTOROLA
SEMICONDUCTOR
PRODUCT BRIEF

MPC561PB/D
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MPC561/MPC562
MPC563/MPC564

Product Brief

MPC561/MPC562 / MPC563/MPC564 RISC MCU Including Peripheral Pin Multiplexing with Flash and Code Compression Options

Features

The MPC561/MPC562 / MPC563/MPC564 are members of the Motorola MPC500 RISC Microcontroller family. As shown in the block diagram, they are composed of:

- High performance CPU system
  - — High performance core
    - Single issue integer core
    - Compatible with PowerPC instruction set architecture
    - Precise exception model
    - Floating point
    - Extensive system development support
      - — On-chip watchpoints and breakpoints
      - — Program flow tracking
      - — Background debug mode (BDM)
      - — IEEE-ISTO Nexus 5001-1999 Class 3 Debug Interface
  - — MPC500 system interface (USIU, BBC, L2U)
  - — Fully static design
  - — Four major power saving modes
    - On, doze, sleep, deep-sleep and power-down
  - — 32-Kbyte static RAM (CALRAM)
  - — 512-Kbyte flash (UC3F) on MPC563/MPC564
  - — General-purpose I/O support
    - On address (24) and data (32) pins
    - 16 GPIO in MIOS14
    - Many peripheral pins can be used as GPIO when not used as primary functions
    - 2.6-V outputs on external bus pins
- PPM (peripheral pin multiplexing with parallel-to-serial driver) module
- Available in package or die
  - — Plastic ball grid array (PBGA) packaging

Key Feature Details

MPC500 System Interface (USIU)

- System configuration and protection features:
  - — Periodic-interrupt timer
  - — Bus monitor
  - — Software watchdog timer
  - — Real-time clock (RTC)

  — Decrementer
  — Time base
- Clock synthesizer
- Power management
- Reset controller
- External bus interface that tolerates 5-V inputs, provides 2.6-V outputs and supports multiple-master designs
- Enhanced interrupt controller that supports up to eight external and 40 internal interrupts, simplifies the interrupt structure and decreases interrupt processing time
- USIU supports dual mapping to map part of one internal/external memory to another external memory
- USIU supports dual mapping of flash on MPC563 and MPC564 to move part of internal flash memory to external bus for development
- External bus, supporting non-wraparound burst for instruction fetches, with up to 8 instructions per memory cycle

Burst Buffer Controller (BBC) Module

- Support for enhanced interrupt controller (EIC)
- Support for enhanced exception table relocation feature
- Branch target buffer
- Contains 2-Kbytes of decompression RAM (DECRAM) for code compression. This RAM may also be used as general-purpose RAM when code compression feature not used.

Flexible Memory Protection Unit

- Flexible memory protection units (MPU) in BBC and L2U
- Default attributes available in one global entry
- Attribute support for speculative accesses
- Up to eight memory regions are supported, four for data and four for instructions

Memory Controller

- Four flexible chip selects via memory controller
- 24-bit address and 32-bit data buses
- 4-Kbyte to one 16-Mbyte (data) or four-Gbyte (instruction) region size support
- Supports enhanced external burst
- Up to eight-beat transfer bursts, two-clock minimum bus transactions
- Use with SRAM, EPROM, flash and other peripherals
- Byte selects or write enables
- 32-bit address decodes with bit masks
- Four regions

512-Kbytes of CDR3 Flash EEPROM Memory (UC3F) – MPC563 Only

- One 512-Kbyte module
- Page read mode
- Block (64 Kbytes) erasable
- External 4.75- to 5.25-V VFLASH power supply for program, erase, and read operations

32-Kbyte static RAM (CALRAM)

- Composed of one 32-Kbyte CALRAM module
  — 28-Kbyte static RAM
  — 4-Kbyte calibration (overlay) RAM feature that allows calibration of flash-based constants
- Eight 512-byte overlay regions
- One clock fast accesses
- Two-clock cycle access option for power saving
- Keep-alive power (VDDSRAM) for data retention

General-Purpose I/O Support

- 24 Address pins and 32 data pins can be used for general-purpose I/O in single-chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 2.6-V outputs on external bus pins
- 5-V outputs with slew rate control

NEXUS Debug Port (Class 3)

- Compliant with Class 3 of the IEEE-ISTO Nexus 5001-1999
- Program trace via branch trace messaging (BTM)
- Data trace via data write messaging (DWM) and data read messaging (DRM)
- Ownership trace via ownership trace messaging (OTM)
- Run-time access to on-chip memory map and MPC5xx special purpose registers (SPRs) via the READI read/write access protocol
- Watchpoint messaging via the auxiliary port
- Reduced-port mode (1 MDI, 2 MDO) or full-port mode (2 MDI. 8 MDO)
- All features configurable and controllable via the auxiliary port
- Security features for production environment
- Supports the RCPU debug mode via the auxiliary port
- READI module can be reset independent of system reset

Integrated I/O System

Two Time Processor Units (TPU3)

- True 5-V I/O
- Two time processing units (TPU3) with16 channels each
- Each TPU3 is a micro-coded timer subsystem
- Eight-Kbytes of dual port TPU RAM (DPTRAM) shared by two TPU3 modules for TPU micro-code

22-Channel Modular I/O System (MIOS14)

- Six modulus counter sub-modules (MCSM)
- 10 double-action sub-modules (DASM)
- 12 dedicated PWM sub-modules (PWMSM)
- One MIOS14 16-bit parallel port I/O sub-modules (MPIOSM)

Two Enhanced Queued Analog-to-Digital Converter Modules (QADC64E)

- Two queued analog-to-digital converter modules (QADC64_A, QADC64_B) providing a total of 32 analog channels
- 16 analog input channels on each QADC64E module using internal multiplexing
- Directly supports up to four external multiplexers
- Up to 41 total input channels on the two QADC64E modules with external multiplexing
- Software configurable to operate in Enhanced or Legacy (MPC555 compatible) mode
- Unused analog channels can be used as digital input/output pins
  - — GPIO on all channels in Enhanced mode
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of less than 5 µs (>200 K samples/second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
  - — External edge trigger
  - — Software command
  - — Periodic/interval timer within QADC64E module, that can be assigned to both queue 1 and 2
  - — External Gated trigger (queue 1only)
- 64 result registers
  - — Output data is right- or left-justified, signed or unsigned

• Alternate reference input (ALTREF), with control in the conversion command word (CCW)

Three CAN 2.0B Controller (TouCAN) Modules

• Three TouCAN modules (TOUCAN_A, TOUCAN_B, TOUCAN_C)
• Each TouCAN provides the following features:
  — 16 message buffers each, programmable I/O modes
  — Maskable interrupts
  — Independent of the transmission medium (external transceiver is assumed)
  — Open network architecture, multi-master concept
  — High immunity to EMI
  — Short latency time for high-priority messages
  — Low-power sleep mode, with programmable wake-up on bus activity
  — TOUCAN_C pins are shared with MIOS14 GPIO or QSMCM

Queued Serial Multi-Channel Module (QSMCM)

• One queued serial module with one queued SPI and two SCIs (QSMCM)
• QSMCM matches full MPC555 QSMCM functionality
• Queued SPI
  — Provides full-duplex communication port for peripheral expansion or inter-processor communication
  — Up to 32 preprogrammed transfers, reducing overhead
  — Synchronous serial interface with baud rate of up to system clock / 4
  — Four programmable peripheral-selects pins:
  — Support up to 16 devices with external decoding
  — Support up to eight devices with internal decoding
  — Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
• SCI
  — UART mode provides NRZ format and half- or full-duplex interface
  — 16 register receive buffers and 16 register transmit buffers on one SCI
  — Advanced error detection and optional parity generation and detection
  — Word-length programmable as eight or nine bits
  — Separate transmitter and receiver enable bits, and double buffering of data
  — Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

Peripheral Pin Multiplexing (PPM) PPM

• Synchronous serial interface between the microprocessor and an external device
• Four internal parallel data sources can be multiplexed through the PPM
  — TPU3_A: 16 channels
  — TPU3_B: 16 channels
  — MIOS14: 12 PWM channels, 4 MDA channels
  — Internal GPIO: 16 general-purpose inputs, 16 general-purpose outputs
• Software configurable stream size
• Software configurable clock (TCLK) based on system clock
• Software selectable clock modes (SPI mode and TDM mode)
• Software selectable operation modes
  — Continuous mode
  — Start-transmit-receive (STR) mode
• Software configurable internal modules interconnect (shorting)

MPC561/MPC562 / MPC563/MPC564 Optional Features

The following are optional features of the MPC561/MPC562 / MPC563/MPC564:

- 56-MHz operation (40 MHz is default)
- Code compression supported on the MPC562 and the MPC564
  - — Compression reduces instruction memory requirements by 40-50%
  - — Compression optimized for automotive (non-cached) applications
- 512 Kbytes flash (available on the MPC563/MPC564 only)
  - — Single array
  - — Page mode read
  - — Block (64 Kbytes) erasable
  - — External 4.75- to 5.25-V VFLASH program, erase, and read power supply

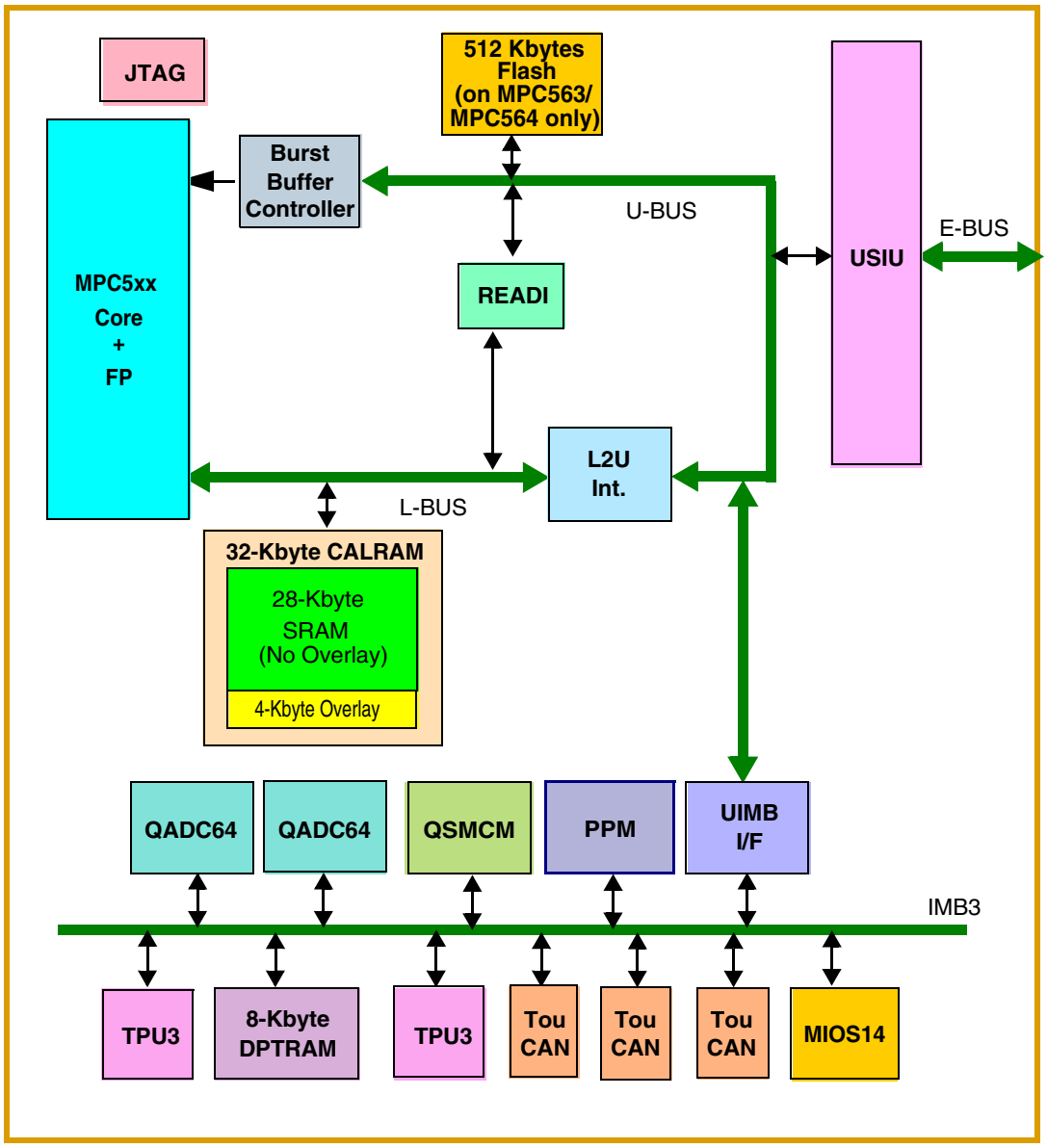
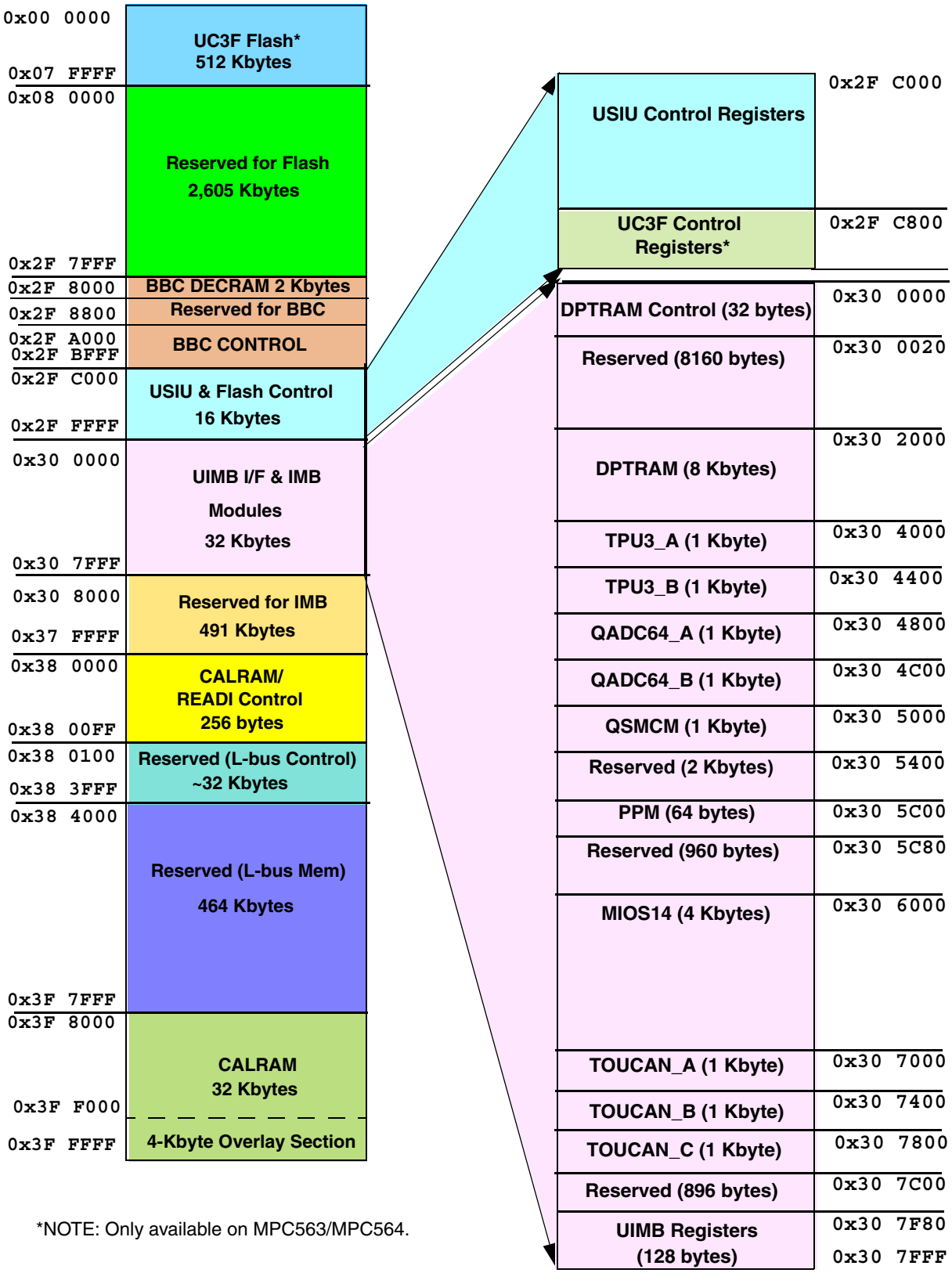
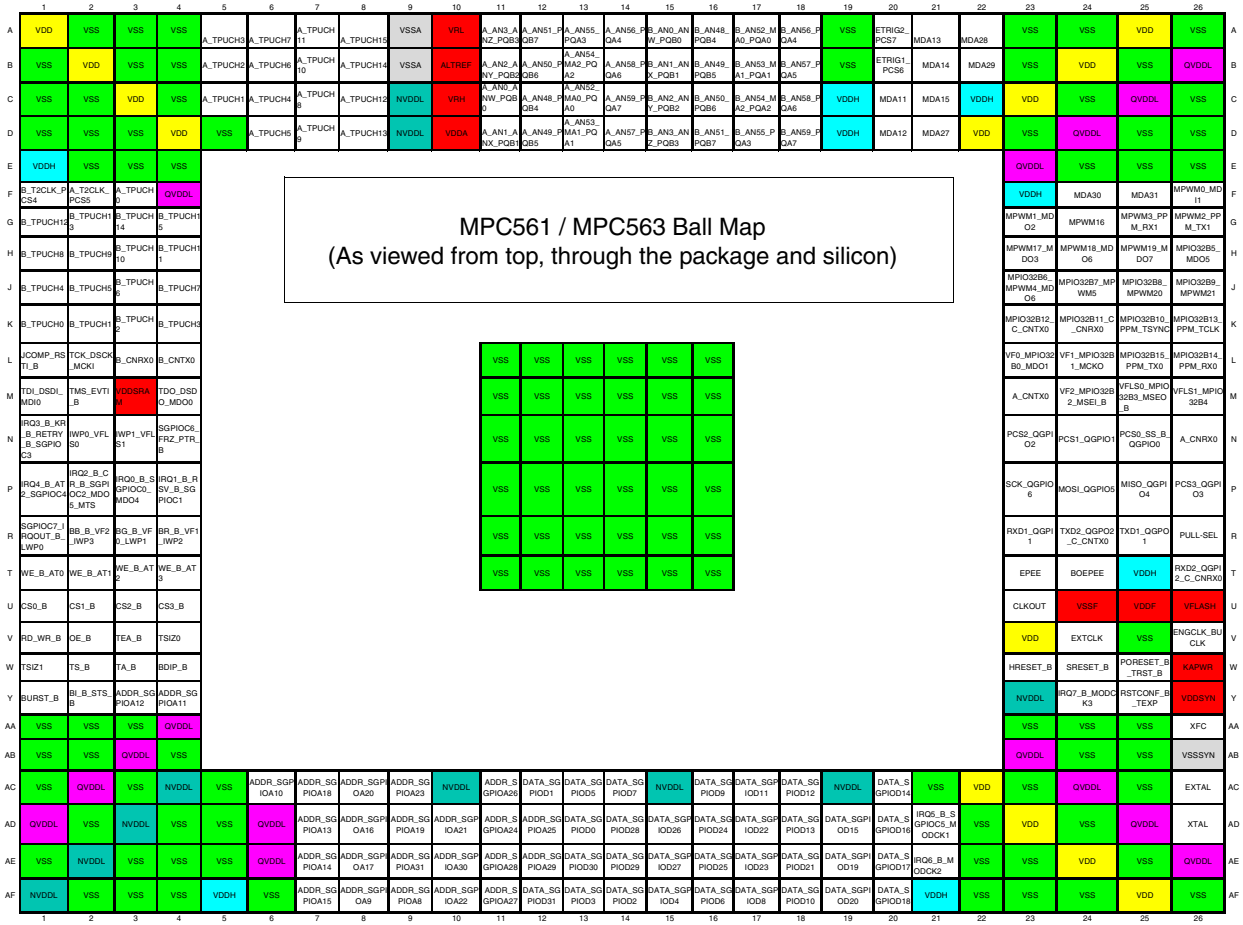


Figure 1 MPC561/MPC562 / MPC563/MPC564 Block Diagram



*NOTE: Only available on MPC563/MPC564.

Figure 2 MPC561 / MPC563 Internal Memory Map



NOTE: The flash balls are only available on the MPC563 and MPC564. These are no connect balls on the MPC561 and MPC562. Flash supplies and inputs are located on the following balls: T23, T24, U24, U25. U26.

Figure 3 MPC561 / MPC563 Ball Map

Ordering Information

Table 1 MPC561/562 / MPC563/564

Device Name	Order Part Number[1]	Package Info	Temperature Range	Maximum Frequency	Code Compression
MPC561	MPC561MZP40	388 PBGA	-40 – 125° C	40 MHz	No
MPC561	MPC561CZP40	388 PBGA	-40 – 85° C	40 MHz	No
MPC561	MPC561MZP56	388 PBGA	-40 – 125° C	56 MHz	No
MPC561	MPC561CZP56	388 PBGA	-40 – 85° C	56 MHz	No
MPC562	MPC562MZP40	388 PBGA	-40 – 125° C	40 MHz	Yes
MPC562	MPC562CZP40	388 PBGA	-40 – 85° C	40 MHz	Yes
MPC562	MPC562MZP56	388 PBGA	-40 – 125° C	56 MHz	Yes
MPC562	MPC562CZP56	388 PBGA	-40 – 85° C	56 MHz	Yes
MPC563	MPC563MZP40	388 PBGA	-40 – 125° C	40 MHz	No
MPC563	MPC563CZP40	388 PBGA	-40 – 85° C	40 MHz	No
MPC563	MPC563MZP56	388 PBGA	-40 – 125° C	56 MHz	No
MPC563	MPC563CZP56	388 PBGA	-40 – 85° C	56 MHz	No
MPC564	MPC564MZP40	388 PBGA	-40 – 125° C	40 MHz	Yes
MPC564	MPC564CZP40	388 PBGA	-40 – 85° C	40 MHz	Yes
MPC564	MPC564MZP56	388 PBGA	-40 – 125° C	56 MHz	Yes
MPC564	MPC564CZP56	388 PBGA	-40 – 85° C	56 MHz	Yes

NOTES:
1. Add R2 suffix for parts shipped in tape and reel media.

Table 2 lists the documents that provide a complete description of the MPC561/563 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola Semiconductor documentation page on the Internet (the source for the latest information).

Table 2 Available Documentation

Document Number	Title
MPC561_3RM/AD	*MPC561/MPC563 Reference Manual*
AN1821/D	*Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family*
AN2109/D	*MPC555 Interrupts.*
AN2127/D	*EMC Guidelines for MPC500-Based Automotive Powertrain Systems*

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Order Number MPC561PB/D