

ML6554

3A Bus Termination Regulator

Features

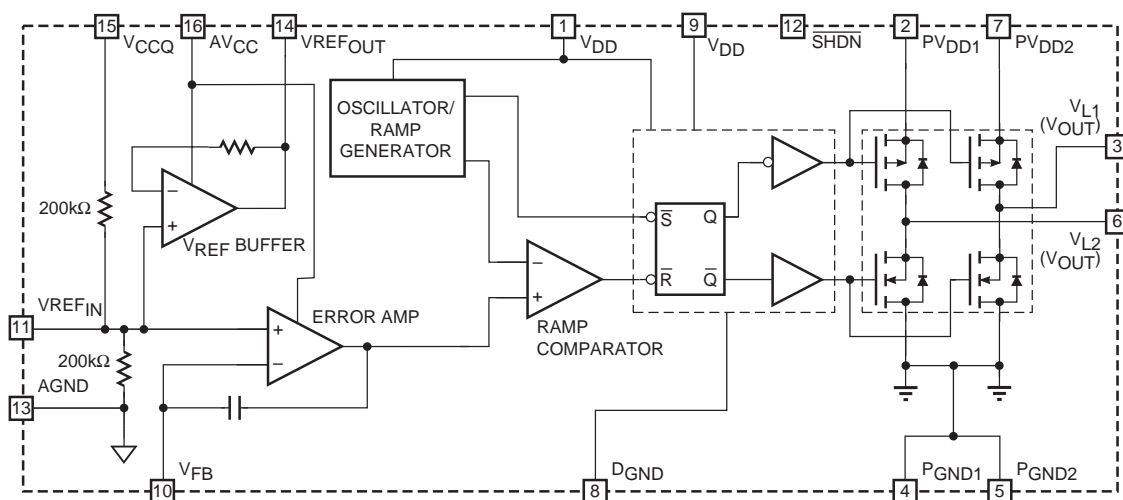
- Can source and sink up to 3A, no heat sink required
- Integrated Power MOSFETs
- Generates termination voltages for DDR SDRAM, SSTL-2 SDRAM, SGRAM, or equivalent memories
- Generates termination voltages for active termination schemes for DDR SDRAM, GTL+, Rambus, VME, LV-TTL, HSTL, PECL and other high speed logic
- V_{REF} input available for external voltage divider
- Separate voltages for V_{CCQ} and PV_{DD}
- Buffered V_{REF} output
- V_{OUT} of $\pm 3\%$ or less at 3A
- Minimum external components
- Shutdown for standby or suspend mode operation
- 0° to $+70^\circ\text{C}$ and -40° to $+85^\circ\text{C}$ temperature ranges available
- Thermal Shutdown $\approx 130^\circ\text{C}$

Description

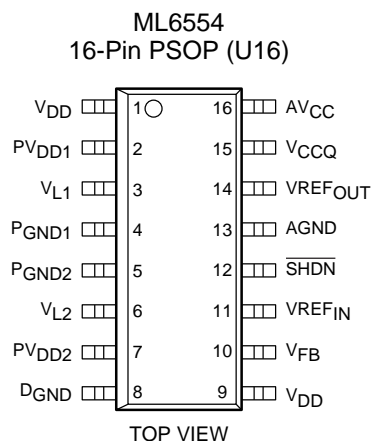
The ML6554 switching regulator is designed to convert voltage supplies ranging from 2.3V to 4V into a desired output voltage or termination voltage for various applications. The ML6554 can be implemented to produce regulated output voltages in two different modes. In the default mode, when the V_{REF} pin is open, the ML6554 output voltage is 50% of the voltage applied to V_{CCQ} . The ML6554 can also be used to produce various user-defined voltages by forcing a voltage on the V_{REFIN} pin. In this case, the output voltage follows the input V_{REFIN} voltage. The switching regulator is capable of sourcing or sinking up to 3A of current while regulating an output V_{TT} voltage to within 3% or less.

The ML6554, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs. The voltage output of the regulator can be used as a termination voltage for other bus interface standards such as DDR SDRAM, SSTL, CMOS, Rambus™, GTL+, VME, LV-CMOS, LV-TTL, HSTL and PECL.

Block Diagram



Pin Configuration



Pin Description

| Pin | Name | Function |
|-----|---------------------|--|
| 1 | V _{DD} | Digital supply voltage |
| 2 | PV _{DD1} | Voltage supply for internal power transistors |
| 3 | V _{L1} | Output voltage/ inductor connection |
| 4 | P _{GND1} | Ground for output power transistors |
| 5 | P _{GND2} | Ground for output power transistors |
| 6 | V _{L2} | Output voltage/inductor connection |
| 7 | PV _{DD2} | Voltage supply for internal power transistors |
| 8 | D _{GND} | Digital ground |
| 9 | V _{DD} | Digital supply voltage |
| 10 | V _{FB} | Input for external compensation feedback |
| 11 | VREF _{IN} | Input for external reference voltage |
| 12 | SHDN | Shutdown active low. CMOS input level |
| 13 | AGND | Ground for internal reference voltage divider |
| 14 | VREF _{OUT} | Reference voltage output |
| 15 | V _{CCQ} | Voltage reference for internal voltage divider |
| 16 | AV _{CC} | Analog voltage supply |

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

| Parameter | Min. | Max. | Units |
|--|-----------|----------------|-------|
| PV_{DD} | | 4.5 | V |
| Voltage on Any Other Pin | GND – 0.3 | $V_{IN} + 0.3$ | V |
| Average Switch Current (I_{AVG}) | | 3.0 | A |
| Junction Temperature | | 150 | °C |
| Storage Temperature Range | -65 | 150 | °C |
| Lead Temperature (Soldering, 10 sec) | | 150 | °C |
| Thermal Resistance (θ_{JC})(Note 2) | | 2 | °C/W |
| Output Current, Source or Sink | | 3.0 | A |

Operating Conditions

| Parameter | Min. | Max. | Units |
|------------------------------|------|------|-------|
| Temperature Range, CU suffix | 0 | 70 | °C |
| Temperature Range, IU suffix | -40 | +85 | °C |
| PV_{DD} Operating Range | 2.0 | 4.0 | V |
| V_{CCQ} Operating Range | 1.4 | 4.0 | V |

Electrical Characteristics

Unless otherwise specified, $AV_{CC} = V_{DD} = PV_{DD} = 3.3V \pm 10\%$, T_A = Operating Temperature Range (Note 1)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Units |
|----------------------|--|--|-------------------------|-------|------|-------|-------|
| Switching Regulator | | | | | | | |
| V _{TT} | Output Voltage, SSTL_2 (See Figure 1) | I _{OUT} = 0, V _{REF} = open | V _{CCQ} = 2.3V | 1.12 | 1.15 | 1.18 | V |
| | | | V _{CCQ} = 2.5V | 1.22 | 1.25 | 1.28 | V |
| | | | V _{CCQ} = 2.7V | 1.32 | 1.35 | 1.38 | V |
| | | I _{OUT} = ±3A, V _{REF} = open | V _{CCQ} = 2.3V | 1.09 | 1.15 | 1.21 | V |
| | | | V _{CCQ} = 2.5V | 1.19 | 1.25 | 1.31 | V |
| | | | V _{CCQ} = 2.7V | 1.28 | 1.35 | 1.42 | V |
| VREF _{OUT} | Internal Resistor Divider | I _{OUT} = 0 | V _{CCQ} = 2.3V | 1.139 | 1.15 | 1.162 | V |
| | | | V _{CCQ} = 2.5V | 1.238 | 1.25 | 1.263 | V |
| | | | V _{CCQ} = 2.7V | 1.337 | 1.35 | 1.364 | V |
| Z _{IN} | V _{REF} Reference Pin Input Impedance | | V _{CCQ} = 0 | | 100 | | kΩ |
| | Switching Frequency | | | | 650 | | kHz |
| ΔV _{OFFSET} | Offset Voltage V _{TT} – VREF _{OUT} | AV _{CC} = 2.5V No Load | V _{CCQ} = 2.5 | –20 | | 20 | mV |
| Supply | | | | | | | |
| I _Q | Quiescent Current | I _{OUT} = 0, no load V _{CCQ} = 2.5V | I _{VCCQ} | | 6 | 10 | μA |
| | | | I _{AVCC} | | 0.5 | 1.0 | mA |
| | | | I _{AVCC} SD | | 0.2 | 0.5 | mA |
| | | | I _{VDD} | | 0.25 | 1.0 | mA |
| | | | I _{VDD} SD | | 0.2 | 1.0 | mA |
| | | | I _{PVDD} | | 100 | 250 | μA |
| Buffer | | | | | | | |
| I _{REF} | Output Load Current | | | 3 | | | mA |

Notes

- Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
- Infinite heat sink

Functional Description

This switching regulator is capable of sinking and sourcing 3A of current without an external heatsink. The ML6554 uses a power surface mount package (PSOP) that includes an integrated heat slug. The heat can be piped through the bottom of the device and onto the PCB (Figure 1).

The ML6554 integrates two power MOSFETs that can be used to source and sink 3A of current while maintaining a tight voltage regulation. Using the external feedback, the output can be regulated well within 3% or less, depending on the external components chosen. Separate voltage supply inputs have been added to accommodate applications with various power supplies for the databus and power buses, see Figure 2.

Outputs

The output voltage pins (V_{L1} , V_{L2}) are tied to the databus, address, or clock lines via an external inductor. See the Applications section for recommendations. Output voltage is determined by the V_{CCQ} or $VREF_{IN}$ inputs.

Inputs

The input voltage pins (V_{CCQ} or $VREF_{IN}$) determine the output voltages (V_{L1} or V_{L2}). In the default mode, where the $VREF_{IN}$ pin is floating, the output voltage is 50% of the V_{CCQ} input. V_{CCQ} can be the reference voltage for the databus.

Output voltage can also be selected by forcing a voltage at the $VREF_{IN}$ pin. In this case, the output voltage follows the voltage at the $VREF_{IN}$ input. Simple voltage dividers can be used in this case to produce a wide variety of output voltages between 0.7V and $V_{DD}-0.7V$.

VREF Input and Output

The $VREF_{IN}$ input can be used to force a voltage at the outputs (Inputs section, above). The $VREF_{OUT}$ pin is an output pin that is driven by a small output buffer to provide the $VREF$ signal to other devices in the system. The output buffer is capable of driving several output loads. The output buffer can handle 3mA.

Other Supply Voltages

Several inputs are provided for the supply voltages: PV_{DD1} , PV_{DD2} , AV_{CC} , and V_{DD} .

The PV_{DD1} and PV_{DD2} provide the power supply to the power MOSFETs. V_{DD} provides the voltage supply to the digital sections, while AV_{CC} supplies the voltage for the analog sections. Again, see the Applications section for recommendations.

Feedback Input

The V_{FB} pin is an input that can be used for closed loop compensation. This input is derived from the voltage output. See application section for recommendation.

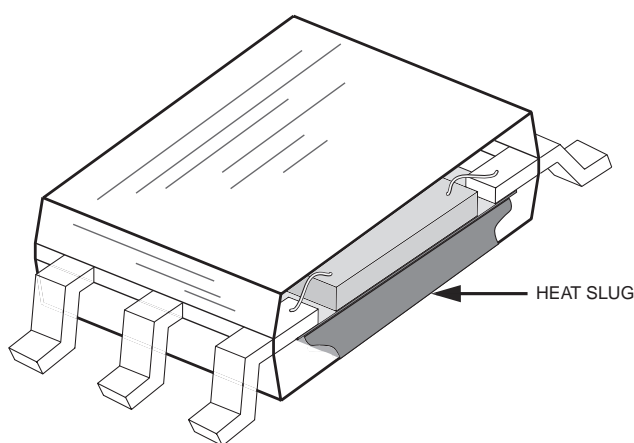


Figure 1. Cutaway view of PSOP Package

Applications

Using the ML6554 for SSTL Bus Termination

The circuit schematic in Figure 2 shows a recommended approach for constructing a bus terminating solution for an SSTL-2 bus. This circuit can be used in PC memory and Graphics memory applications as shown in Figures 4 and 5. Note that the ML6554 can provide the voltage reference (V_{REF}) and terminating voltages (V_{TT}). Using the layout as shown in Figures 6, 7, and 8, and measuring the V_{TT} performance using the test setup as described in Figure 9, the ML6554 delivered a $V_{TT} \pm 20\text{mV}$ for 1A to 3A loads (see Figure 10). Table 1 provides a recommended parts list for the circuit in Figure 2.

Power Handling Capability of the PSOP Package

Using the board layout shown in Figures 6, 7, and 8; soldering the ML6554 to the board at zero LFPM the temperature around the package measured 55°C for 3A loads. Note that a 1 ounce copper plane was used in the board construction.

Airflow is not likely to be needed in the operation of this device (assuming a board layout similar to that described above). The power handling performance of the PSOP package is shown by a study of the package manufacturer for various airflow vs. θ_{JA} conditions in Figure 11.

Bus Termination Solutions for Others Buses

Table 3 provides a summary of various bus termination V_{REF} & V_{TT} requirements. The ML6554 can be used for those applications.

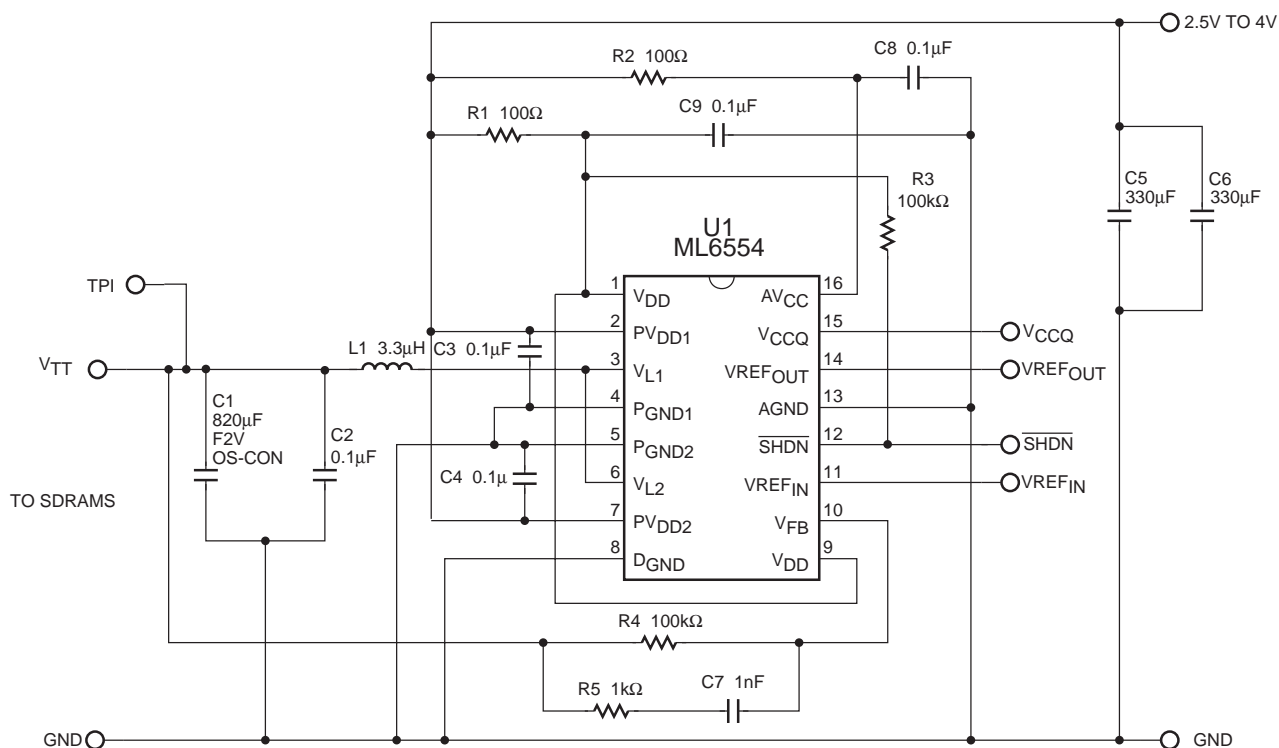


Figure 2.

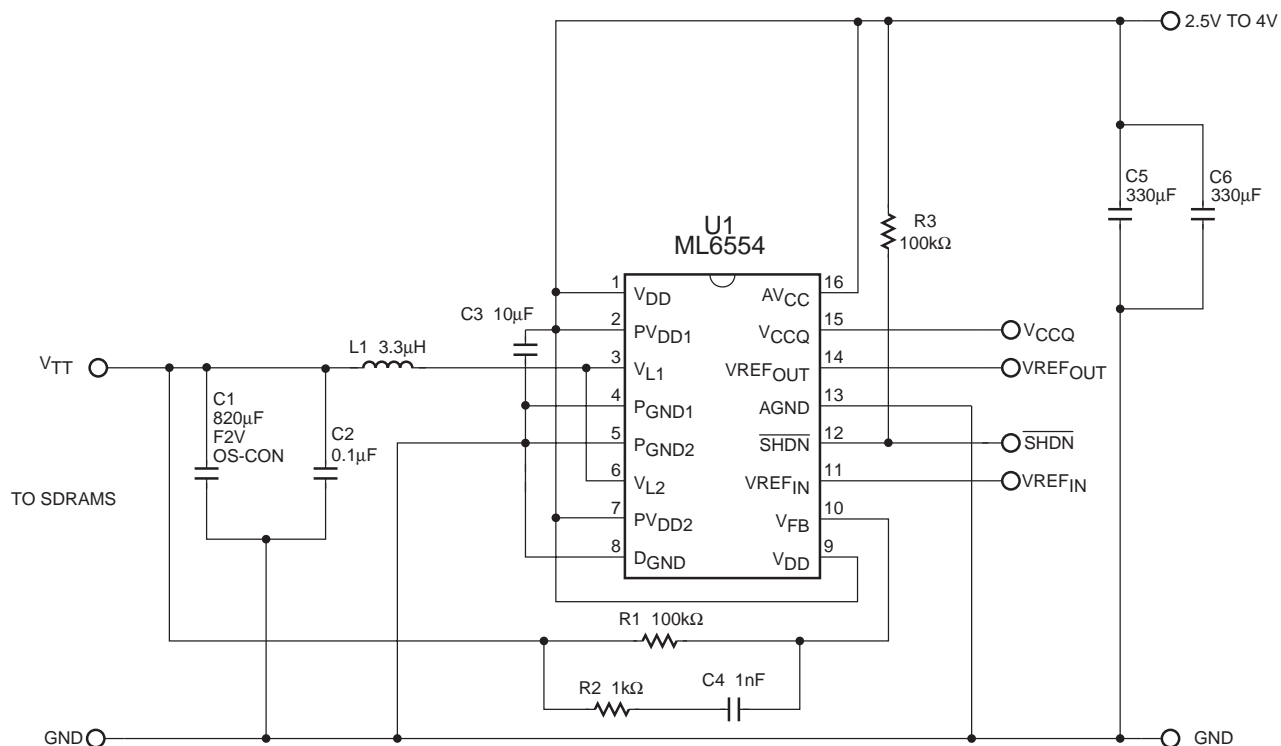


Figure 3. Alternate Application Circuit

An alternate application circuit for the ML6554 is shown in Figure 3. The number of external components is reduced compared to the circuit in Figure 2. This is achieved by replacing four, 0.1µF bypass capacitors with one, low ESR, 10µF ceramic capacitor placed right next to U1. Two 100Ω resistors are also eliminated. High value, surface-mount

MLC capacitors were not available when the original application circuit (Figure 2) was developed. Both application circuits offer the same electrical performance but that shown in Figure 2 has a reduced bill-of-materials. Table 2 shows the recommended parts list for the circuit of Figure 3.

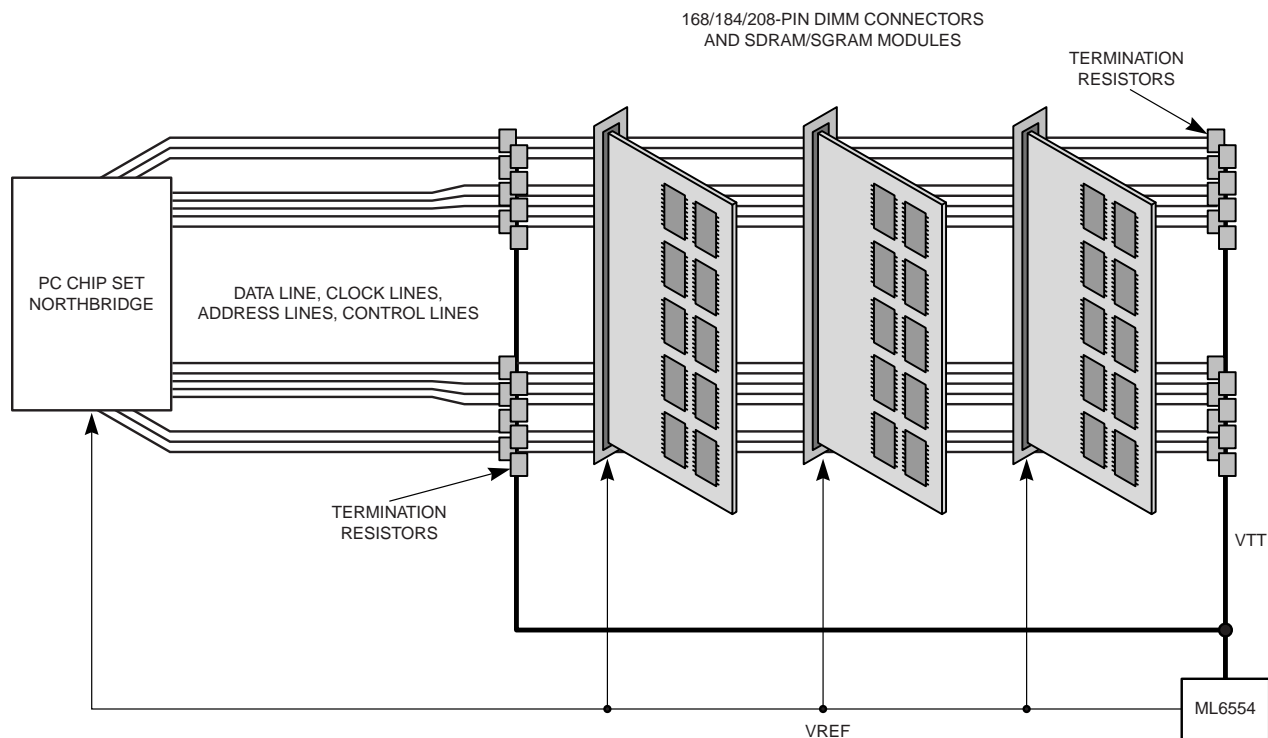


Figure 4. Complete Termination Solution PC Main Memory (PC Motherboard)

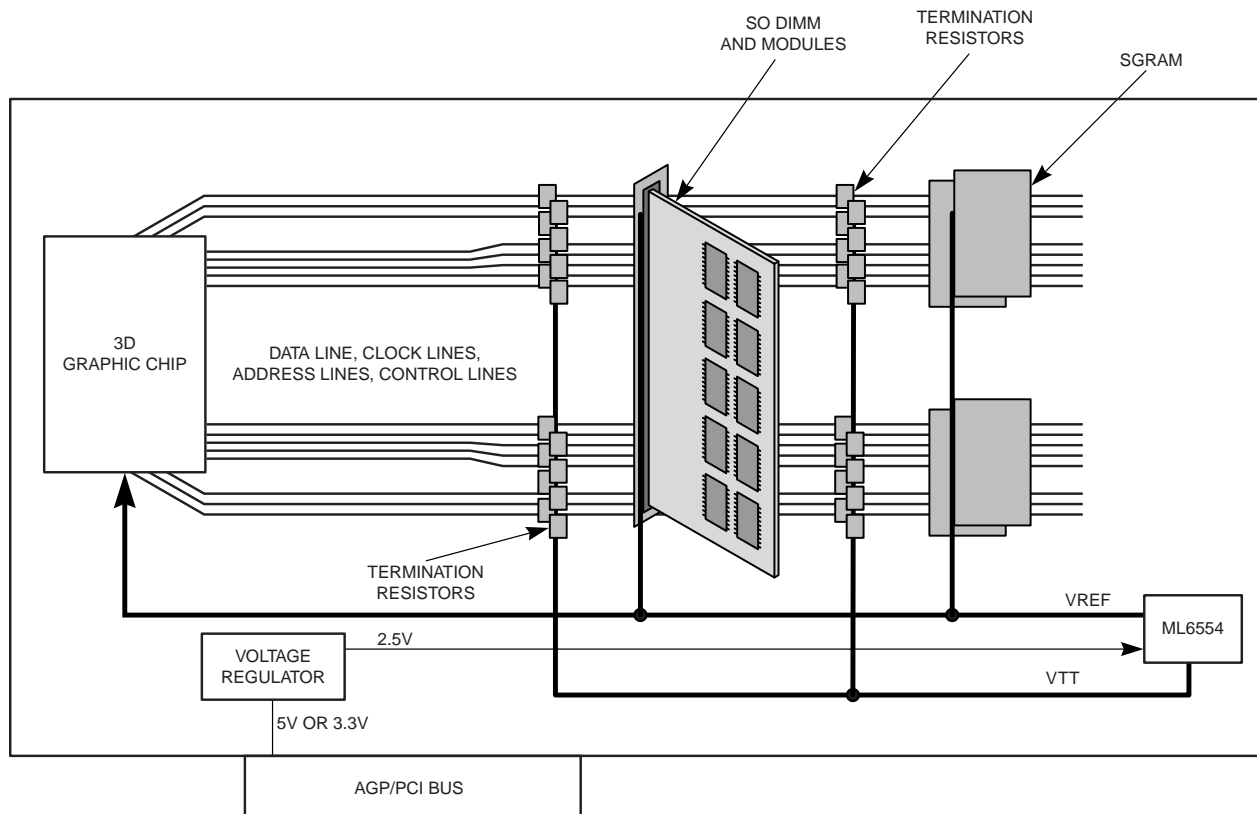


Figure 5. Complete Termination Solution Graphics Memory Bus – AGP Graphics Cards

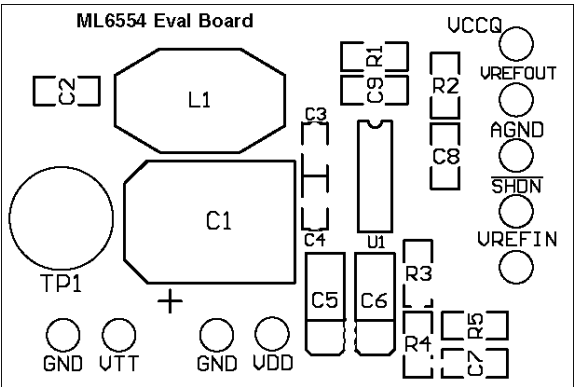


Figure 6. Top Silk

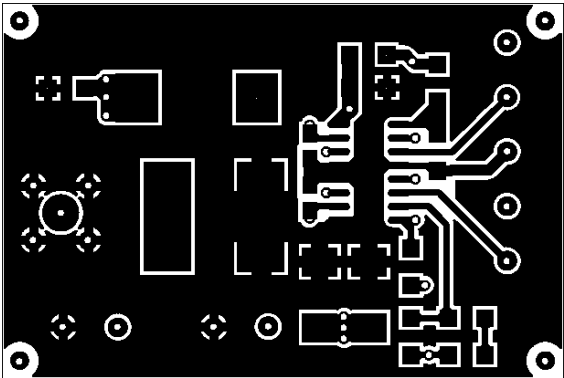


Figure 7. Top Layer

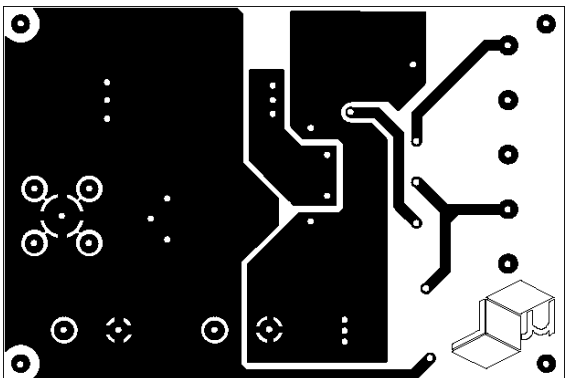


Figure 8. Bottom Layer

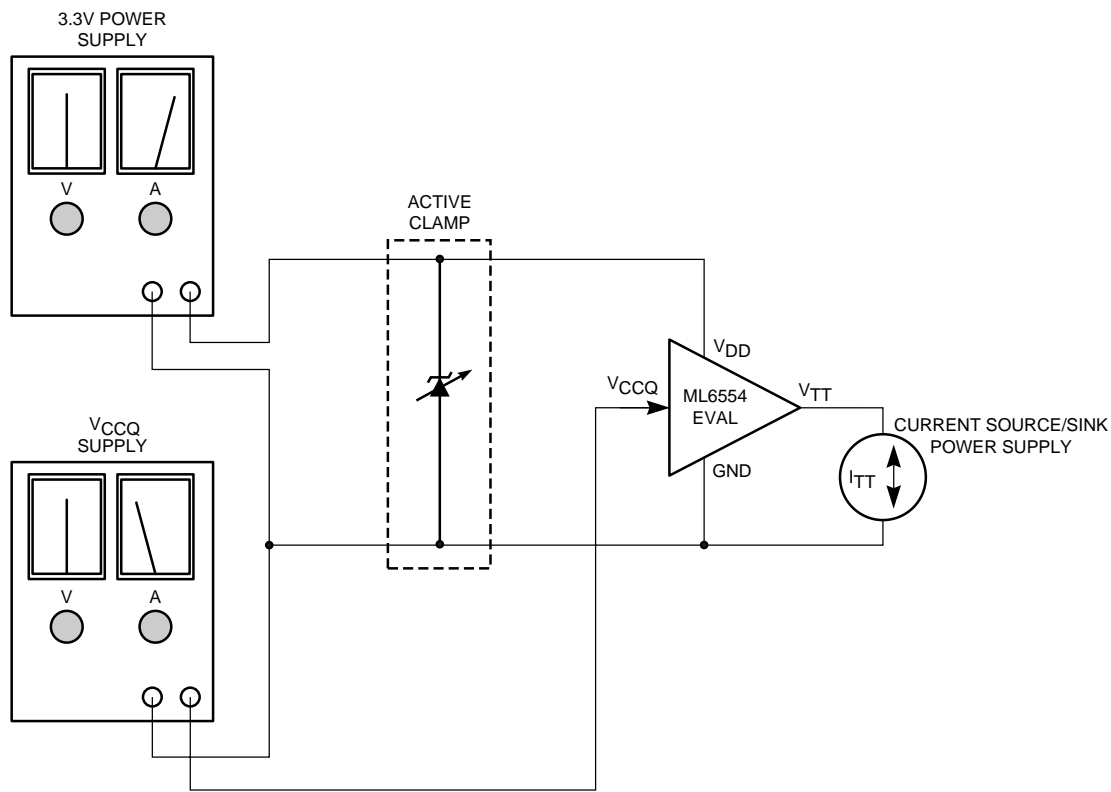


Figure 9. Test Circuit Setup

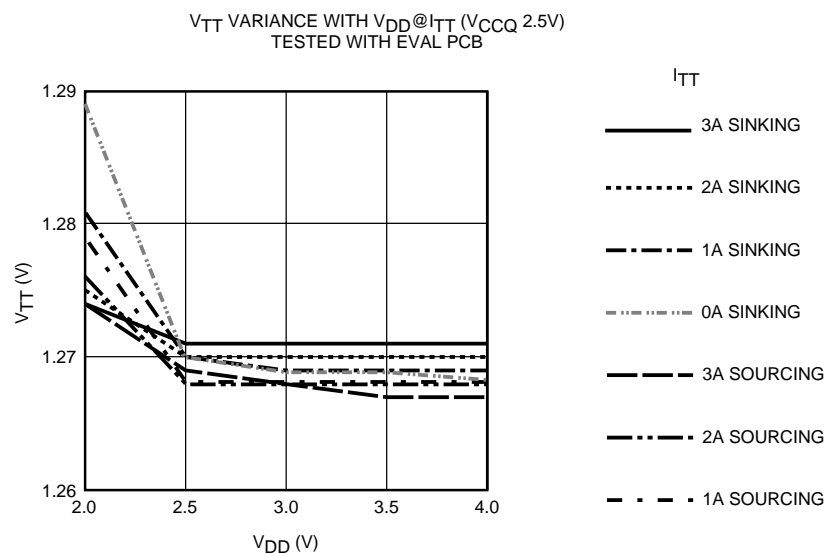


Figure 10. VTT Performance for SSTL-2 Bus

Table 1. Recommend Parts List for SSTL-2 Termination Circuit in Figure 2.

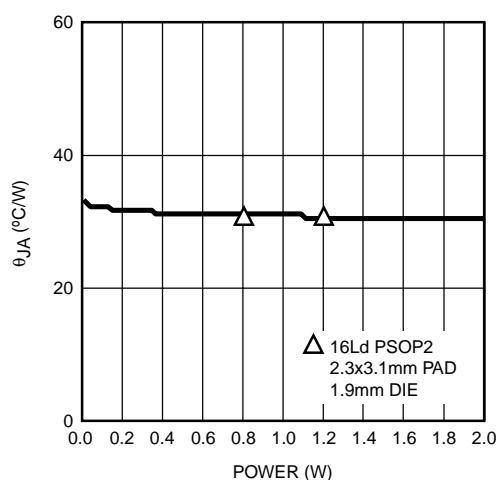
| Item | Qty | Description | Manufacturer / Part Number | Designator |
|-------------------|-----|--|---|----------------|
| Resistors | | | | |
| 1 | 2 | 100Ω1210 SMD | Panasonic/ERJ-8ENF1000V | R1, R2 |
| 2 | 1 | 1kΩ 1210 SMD | Panasonic/ERJ-8ENF1001V | R5 |
| 3 | 2 | 100kΩ1210 SMD | Panasonic/ERJ-8ENF1003V | R3, R4 |
| Capacitors | | | | |
| 4 | 3 | 0.1μF 1210 Film SMD | Panasonic/ECV3VB1E104K Panasonic/ECU-V1H104KBW | C2, C8, C9 |
| 5 | 1 | 820μF 2V Solid Elect. SMD | Sanyo/2SV820M Os Con | C1 |
| 6 | 2 | 330μF Tant 6.3V 100mΩ | AVX/TPSE337M006R0100 | C5, C6 |
| 7 | 1 | 1nF 1210 Film SMD | Panasonic/ECU-V1H102KBM | C7 |
| 8 | 2 | 0.1μF 0805 Film | Panasonic/ECJ-2VF1C104Z | C3, C4 |
| ICS | | | | |
| 9 | 1 | ML6554 Bus Terminator Power SOP Package | ML6554CU or ML6554IU | U1 |
| Magnetics | | | | |
| 10 | 1 | 3.3μH 5A inductor SMD | Coilcraft/D03316P-332HC Pulse Eng./ P0751.332T Gowanda/SMP3316-331M XFMRS inc./XF0046-S4 | L1 |
| Other | | | | |
| 11 | 1 | Scope probe socket | Tektronics/131-4353-00 | TP1 |
| 12 | 1 | 12 Pin breakaway strip | Sullins/PTC36SAAN (36 PINS) | I/O, standoffs |

Table 2. Recommend Parts List for Figure 3.

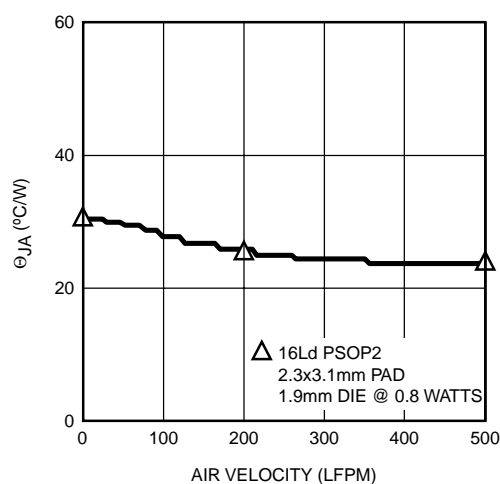
| Item | Qty | Description | Manufacturer / Part Number | Designator |
|-------------------|-----|--|---|----------------|
| Resistors | | | | |
| 1 | 2 | 100kΩ 0805 SMD | Panasonic/ERJ-8ENF1000V | R1, R3 |
| 2 | 1 | 1kΩ 0805 SMD | Panasonic/ERJ-8ENF1000V | R2 |
| Capacitors | | | | |
| 3 | 1 | 0.1μF, 1210 Film SMD | Panasonic/ECV3VB1E104K Panasonic/ECU-V1H104KBW | C2 |
| 4 | 1 | 820μF 2V Solid Elect. SMD | Sanyo/2SV820M Os Con | C1 |
| 5 | 2 | 330μF Tant 6.3V 100mΩ | AVX/TPSE337M006R0100 | C5, C6 |
| 6 | 1 | 1nF 1210 Film SMD | Panasonic/ECU-V1H102KBM | C4 |
| 7 | 1 | 10μF 6.3V Ceramic | TDK/C2012X5R0J106M | C3 |
| ICS | | | | |
| 8 | 1 | ML6554 Bus Terminator Power SOP Package | ML6554CU or ML6554IU | U1 |
| Magnetics | | | | |
| 9 | 1 | 3.3μH 5A inductor SMD | Coilcraft/D03316P-332HC Pulse Eng./ P0751.332T Gowanda/SMP3316-331M XFMRS inc./XF0046-S4 | L1 |
| Other | | | | |
| 10 | 1 | Scope probe socket | Tektronics/131-4353-00 | TP1 |
| 11 | 1 | 12 Pin breakaway strip | Sullins/PTC36SAAN (36 PINS) | I/O, standoffs |

Vendor List

1. AVX (207) 282-5111
2. Sanyo (619) 661-6835
3. Tektronix (408) 496-0800
4. Coilcraft (847) 639-6400
5. Pulse (800) 797-8573
6. Gowanda (716) 532-2234
7. Xfmrs Inc. (317) 834-1066
8. Panasonic (714) 373-7366
9. Digikey (800) 344-4539



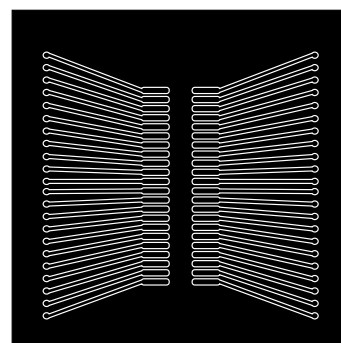
NATURAL CONVECTION θ_{JA} TEST RESULTS
1.27mm PITCH PowerSOP™ 2
SLUG SOLDERED



FORCED CONVECTION θ_{JA} TEST RESULTS
1.27mm PITCH PowerSOP™ 2
SLUG SOLDERED

Figure 11. Graphical Results Summary – 1S2P Test Board

| | |
|--|-------------------------------------|
| DRAWING NUMBER | ENG-CB-1007 REV A |
| Applicable Jedec Spec | JC 51-X (Note 1) (Proposed Spec) |
| Substrate Material | FR-4 |
| Dimensions (LxW) (Overall) | 114.3 x 76.2mm |
| Dimensions (LxW) (Metallization) | 55 x 65mm |
| Dimensions (LxW) (Inner Planes) | 73 x 73mm |
| Thickness | 1.6 mm |
| Pitch | 1.27mm |
| Stackup (# Signal Layers, # Cu Planes) | 1S2P |
| Cu Trace Coverage (Signal Layer) | 12% |
| Cu Coverage (Internal Layer) | 100% |
| Trace Width (Spec/Measured) | 235.5±25.5/288µm |
| Trace Cu Thickness (Spec/Measured) | 70±14/67µm |
| Inner Cu Thickness (Spec/Measured) | 35±3.5/31µm |
| Build # | C1797 |

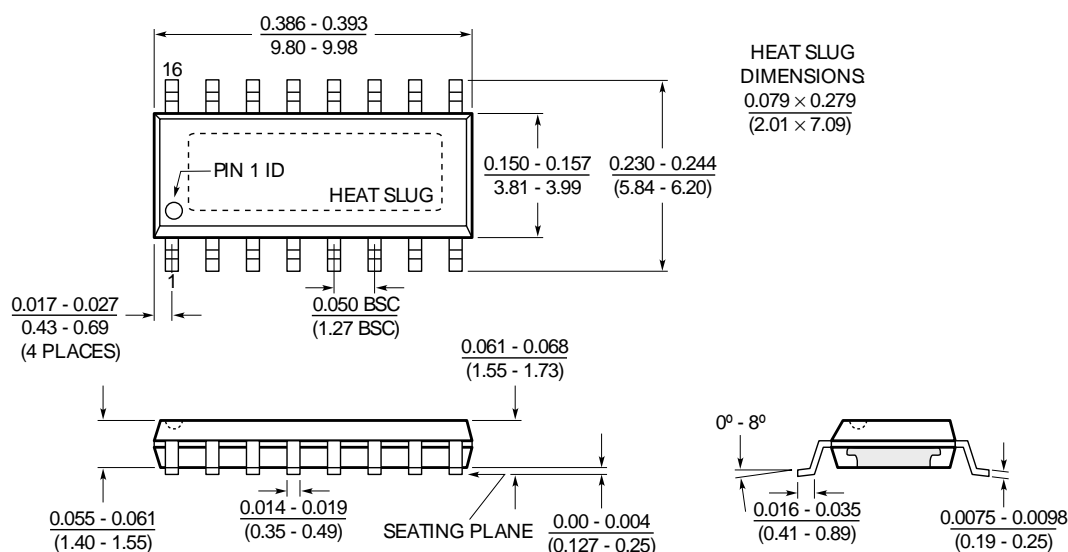


Note 1: Proposed Spec "Thermal Test Board with Two Internal Solid Copper Planes for leaded Surface Mount Packages".

Figure 12. Test Board Layout for Θ_{JA} vs. Airflow

Table 3. Termination Solutions Summary By Buss Type

| Bus | Description | Driving Method | VDDQ | VTT | V _{REF} | Fairchild Solutions | Industry System Components |
|--------|---|------------------------------------|-----------------------|------------------------------------|--------------------|--|--|
| GTL+ | Gunning Transceiver Bus Plus | Open Drain | 5v or 3.3V Note 10 | 1.5V±10% Note12 | 1.0V±2% Note 11 | ML6554CU; Mode: V _{REF} Input = 1.5V, V _{CC} = 5V | 300 to 500MHz Processor; PC Chipsets; GTLP 16xxx Buffers; Fairchild, Texas Instr. |
| SSTL_2 | Series Stub Terminated Logic for 2V | Symmetric Drive, Series Resistance | 2.5V±10% | 0.5x (V _{DDQ}) ±3% | 2.5V | ML6554CU or ML6553CS; Mode: V _{REF} Input = Floating or Forced, V _{CC} = 3.3V | SSTL SDRAM; Hitachi, Fujitsu, NEC, Micro, Mitsubishi |
| RAMBUS | RAMBUS Signaling Logic | Open Drain | None Specified | 2.5V | 2.0V | ML6553CS; Mode: V _{REF} Input = Open, V _{CC} = V _{DDQ} | nDRAM, RAMBUS, Intel, Toshiba |
| LV-TTL | Low Voltage TTL Logic or PECL or 3.3V VME | Symmetric Drive | 3.3±10% | V _{DDQ} /2 | 3.3V | ML6553CS; Mode: V _{REF} Input = Open, V _{CC} = V _{DDQ} | Processors or backplanes; LV-TTL SDRAM, EDO RAM |

Package: U16
16-Pin PSOP

| Part Number | Temperature Range | Package |
|-------------|-------------------|-------------------|
| ML6554CU | 0°C to 70°C | 16-Pin PSOP (U16) |
| ML6554IU | -40°C to +85°C | 16-Pin PSOP (U16) |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.