FAIRCHILD SEMICONDUCTOR®

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KM4112

70μA, Low Cost, +2.7V & +5V, 7.3MHz Rail-to-Rail Amplifier

Features

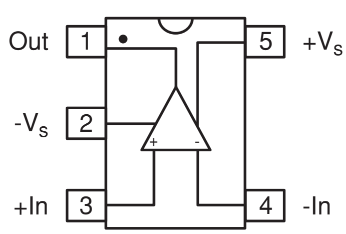
- 70μA supply current
- 7.3MHz bandwidth
- Fully specified at +2.7V and +5V supplies
- Output voltage range: 0.04V to 4.96V; V_S = +5
- Input voltage range: -0.3V to +3.8V; V_S = +5
- 9V/μs slew rate
- ±4mA linear output current
- ±9mA short circuit output current
- 29nV/√Hz input voltage noise
- Competes with low power CMOS amps
- Small package option (SOT23-5)

Applications

- Portable/battery-powered applications
- A/D buffer
- Active filters
- Signal conditioning
- Portable test instruments

KM4112 Package

SOT23-5

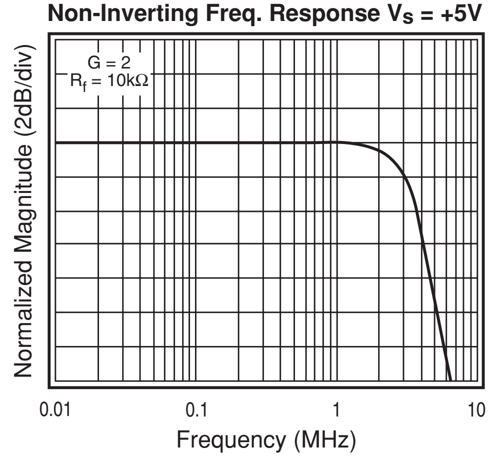


General Description

The KM4112 is an ultra-low power, low cost, voltage feedback amplifier. The KM4112 uses only 70μA of supply current and is designed to operate on +2.7V, +5V, or ±2.5V supplies. The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail.

The KM4112 offers high bipolar performance at a low CMOS price. The KM4112 offers superior dynamic performance with a 7.3MHz small signal bandwidth and 9V/μs slew rate. The combination of low power, high bandwidth, and rail-to-rail performance make the KM4112 well suited for battery-powered communication/computing systems.

Non-Inverting Freq. Response V_S = +5V



KM4112 Electrical Characteristics (V_s = +2.7V, G = 2, R_L = 10kΩ to V_s/2, R_f = 10kΩ; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN & MAX	UNITS	NOTES
Case Temperature		+25°C	+25°C		
Frequency Domain Response					
-3dB bandwidth	G = +1, V_O = 0.05V_{pp}	6.5		MHz	1
	G = +2, V_O < 0.2V_{pp}	3		MHz	
full power bandwidth	G = -1, V_O = 2V_{pp}	2		MHz	
gain bandwidth product		3.5		MHz	
Time Domain Response					
rise and fall time	0.2V step	55		ns	
settling time to 0.1%	1V step	700		ns	
overshoot	1V step,	7		%	
slew rate	2V step, G = -1	7		V/μs	
Distortion and Noise Response					
2nd harmonic distortion	1V_{pp}, 100kHz	68		dBc	
3rd harmonic distortion	1V_{pp}, 100kHz	65		dBc	
THD	1V_{pp}, 100kHz	63		dB	
input voltage noise	>10kHz	30		nV/√Hz	
DC Performance					
input offset voltage		1	±5	mV	2
average drift		3		μV/°C	
input bias current		90	250	nA	2
average drift		100		pA/°C	
input offset current		2.1	100	nA	2
power supply rejection ratio	DC	63	58	dB	2
open loop gain		82	65	dB	2
quiescent current		62	95	μA	2
Input Characteristics					
input resistance		>10		MΩ	
input capacitance		1.6		pF	
input common mode voltage range		-0.3 to 1.5		V	
common mode rejection ratio	DC, V_{cm} = 0V to V_s - 1.5	95	68	dB	2
Output Characteristics					
output voltage swing	R_L = 10kΩ to V_s/2	0.035 to 2.665	0.15 to 2.55	V	2
	R_L = 2kΩ to V_s/2	0.07 to 2.6		V	
linear output current		±4		mA	
short circuit output current		±9		mA	
power supply operating range		2.7	2.5 to 5.5	V	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

NOTES:

1) For G = +1, R_f = 0.

2) 100% tested at +25°C.

Absolute Maximum Ratings

supply voltage	0 to +6V
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (10 sec)	+260°C
operating temperature range (recommended)	-40°C to +85°C
input voltage range	+V_s +0.5V; -V_s -0.5V
internal power dissipation	see power derating curves

Package Thermal Resistance

Package	θ_{JA}
5 lead SOT23	256°C/W

KM4112 Electrical Characteristics (V_s = +5V, G = 2, R_L = 10kΩ to $V_s/2$, R_f = 10kΩ; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN & MAX	UNITS	NOTES
Case Temperature		+25°C	+25°C		
Frequency Domain Response					
-3dB bandwidth	G = +1, V_O = 0.05V_{pp}	7.3		MHz	1
	G = +2, V_O < 0.2V_{pp}	3.4		MHz	
full power bandwidth	G = -1, V_O = 2V_{pp}	2.5		MHz	
gain bandwidth product		4		MHz	
Time Domain Response					
rise and fall time	0.2V step	50		ns	
settling time to 0.1%	2V step	600		ns	
overshoot	2V step,	4		%	
slew rate	2V step, G = -1	9		V/μs	
Distortion and Noise Response					
2nd harmonic distortion	2V_{pp}, 100kHz	67		dBc	
3rd harmonic distortion	2V_{pp}, 100kHz	56		dBc	
THD	2V_{pp}, 100kHz	55		dB	
input voltage noise	>10kHz	29		nV/√Hz	
DC Performance					
input offset voltage		1	±5	mV	2
average drift		8		μV/°C	
input bias current		90	250	nA	2
average drift		100		pA/°C	
input offset current		1.3	100	nA	2
power supply rejection ratio	DC	63	58	dB	2
open loop gain		76	65	dB	2
quiescent current		70	100	μA	2
Input Characteristics					
input resistance		>10		MΩ	
input capacitance		1.6		pF	
input common mode voltage range		-0.3 to 3.8		V	
common mode rejection ratio	DC, V_{cm} = 0V to V_s - 1.5	97	68	dB	2
Output Characteristics					
output voltage swing	R_L = 10kΩ to $V_s/2$	0.04 to 4.96	0.15 to 4.85	V	2
	R_L = 2kΩ to $V_s/2$	0.09 to 4.9		V	
linear output current		±4		mA	
short circuit output current		±9		mA	
power supply operating range		5	2.5 to 5.5	V	

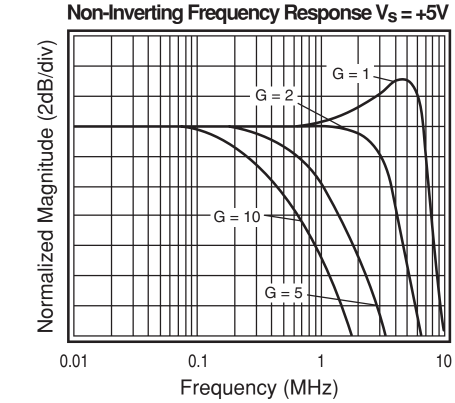
Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

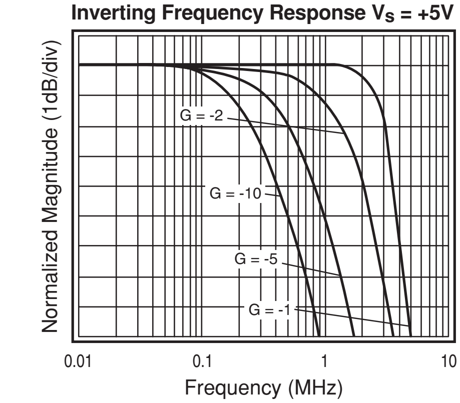
NOTES:

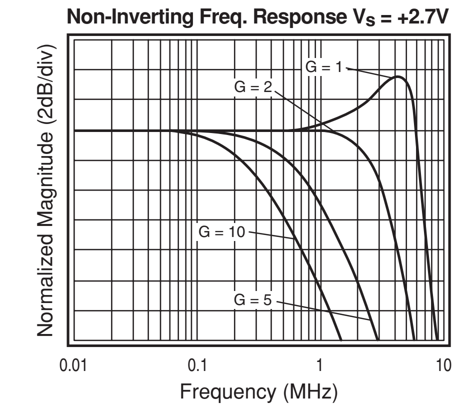
1) For G = +1, R_f = 0.

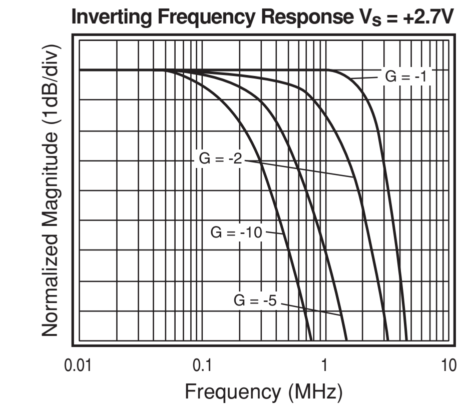
2) 100% tested at +25°C.

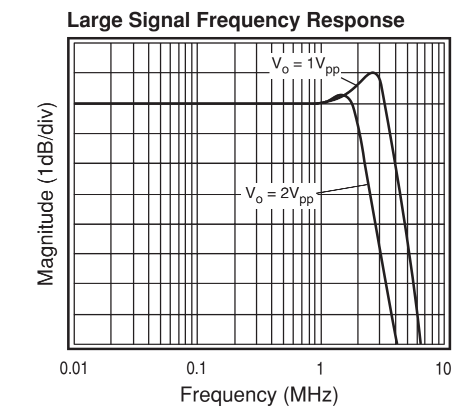
KM4112 Performance Characteristics (V_s = +5V, G = 2, R_L = 10kΩ to V_s/2, R_f = 10kΩ; unless noted)

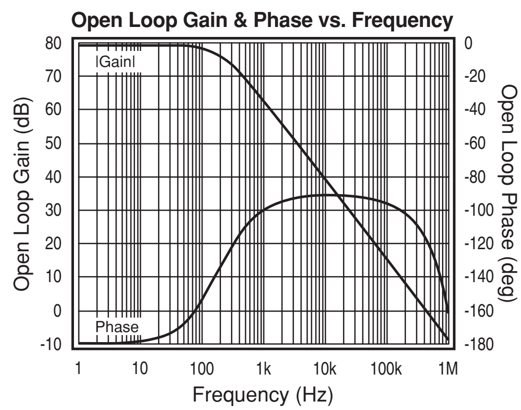


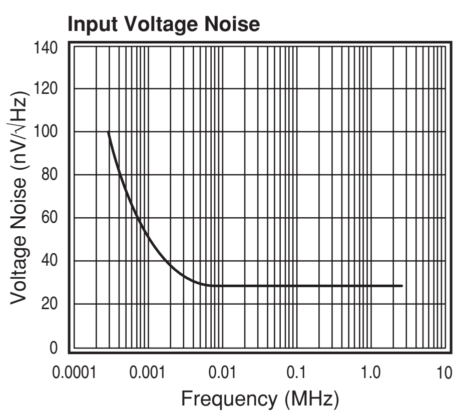


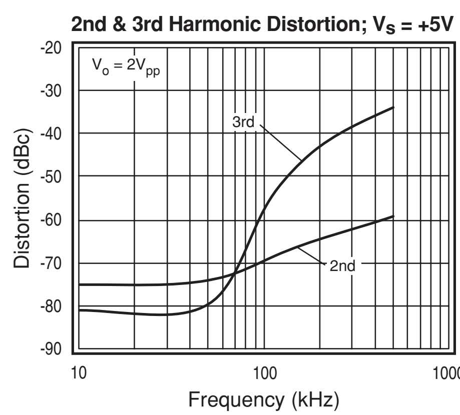




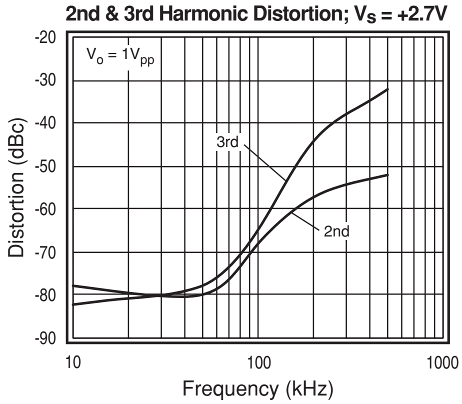


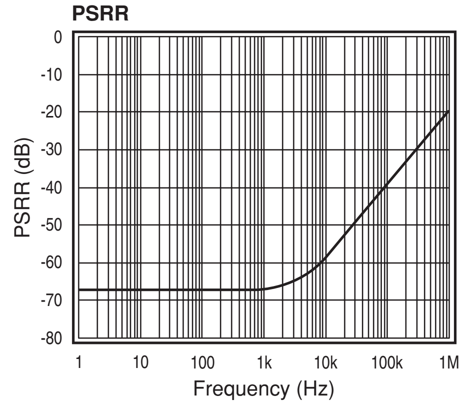


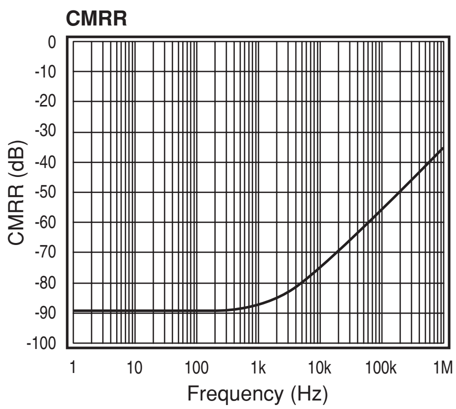


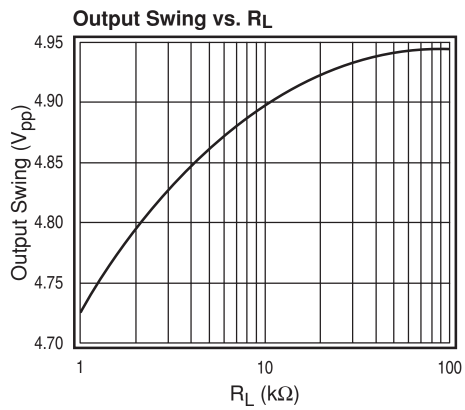


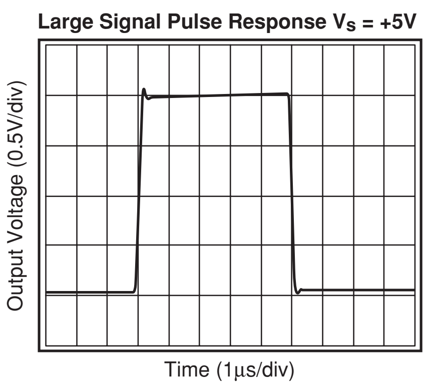
KM4112 Performance Characteristics (V_s = +5V, G = 2, R_L = 10kΩ to V_s/2, R_f = 10kΩ; unless noted)











General Description

The KM4112 is a single supply, general purpose, voltage-feedback amplifier fabricated on a complementary bipolar process. The KM4112 offers 7.3MHz unity gain bandwidth, 9V/μs slew rate, and only 70μA supply current. It features a rail-to-rail output stage and is unity gain stable.

The design utilizes a patent pending topology that provides increased slew rate performance. The common mode input range extends to 300mV below ground and to 1.2V below V_S. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

The typical circuit schematic is shown in Figure 1.

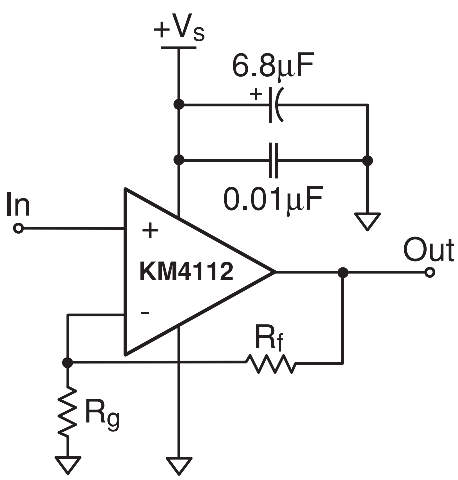


Figure 1: Typical Configuration

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some reliability degradation will occur. If the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

The KM4112 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Follow the maximum power derating curves shown in Figure 2 to ensure proper operation.

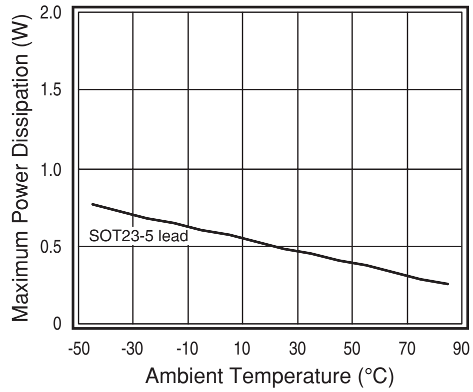


Figure 2: Power Derating Curves

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The KM4112 will typically recover in less than 60ns from an overdrive condition. Figure 3 shows the KM4112 in an overdriven condition.

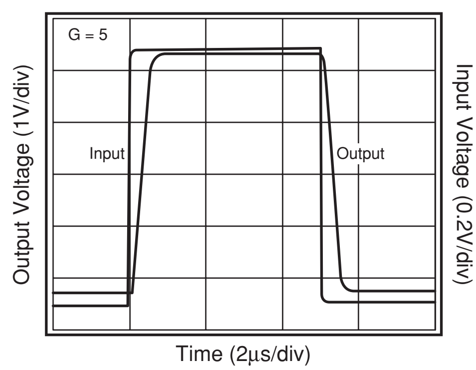


Figure 3: Overdrive Recovery

Driving Capacitive Loads

A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 4, will improve stability and settling performance.

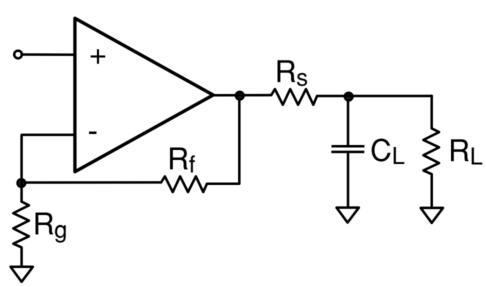


Figure 4: Typical Topology for driving a capacitive load

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and to aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.01μF ceramic capacitors
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.01μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 6 for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

Eval Board	Description	Products
KEB002	Single Channel, Dual Supply 5 & 6 lead SOT23	KM4112IT5

Evaluation board schematics and layouts are shown in Figure 5 and Figure 6.

The KEB002 evaluation board is built for dual supply operation. Follow these steps to use the board in a single supply application:

1. Short $-V_S$ to ground
2. Use C3 and C4, if the $-V_S$ pin of the KM4112 is not directly connected to the ground plane.

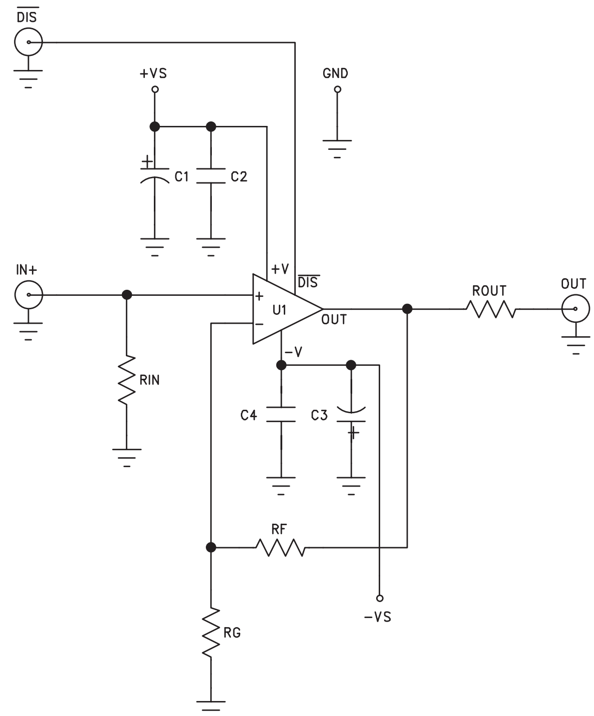


Figure 5: Evaluation Board Schematic

KM4112 Evaluation Board Layout

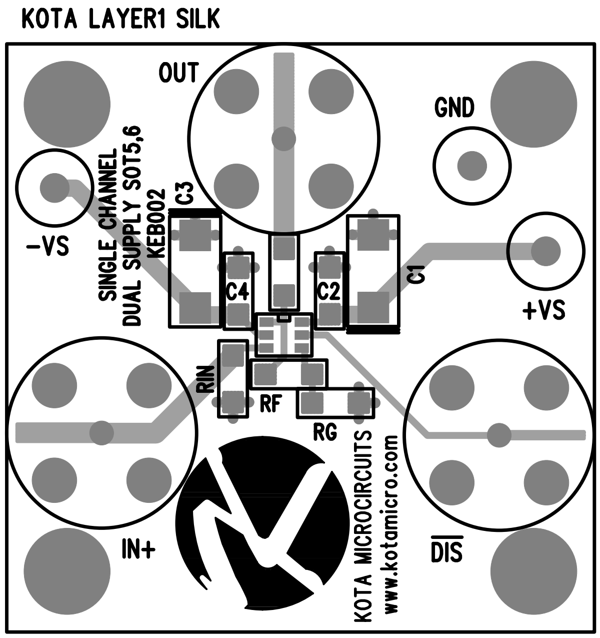


Figure 6a: KEB002 (top side)

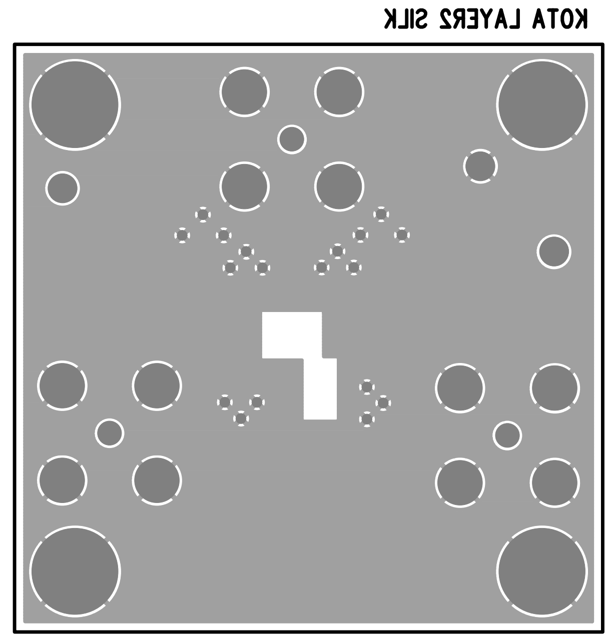
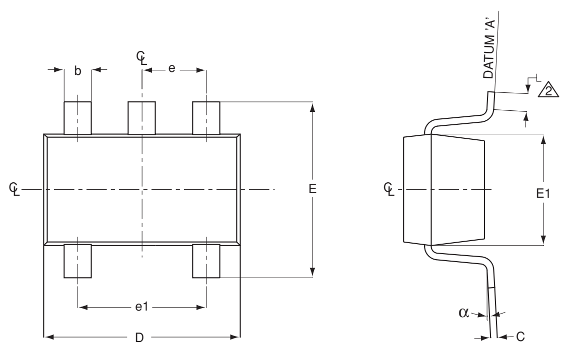


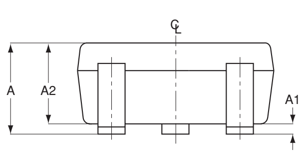
Figure 6b: KEB002 (bottom side)

KM4112 Package Dimensions

SOT23-5



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
C	0.09	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 ref	
e1	1.90 ref	
α	0°	10°



NOTE:
1. All dimensions are in millimeters.
2. Foot length measured reference to flat foot surface parallel to DATUM 'A' and lead surface.
3. Package outline exclusive of mold flash & metal burr.
4. Package outline inclusive of solder plating.
5. Comply to EIAJ SC74A.
6. Package ST 0003 REV A supercedes SOT-D-2005 REV C.

Ordering Information

Model	Part Number	Package	Container	Pack Qty
KM4112	KM4112IT5	SOT23-5	Partial Reel	<3000
KM4112	KM4112IT5TR3	SOT23-5	Reel	3000

Temperature range for all parts: -40°C to +85°C