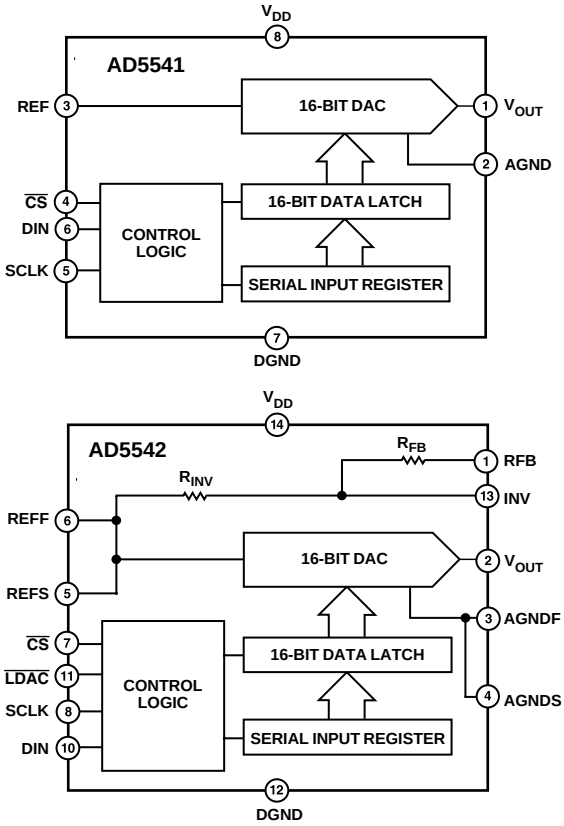
5 V, Serial-Input Voltage-Output, 16-Bit DACs

AD5541/AD5542

FEATURES
Full 16-Bit Performance
5 V Single Supply Operation
Low Power
Short Settling Time
Unbuffered Voltage Output Capable of Driving 60 kΩ Loads Directly
SPI™/QSPI™/MICROWIRE™-Compatible Interface Standards
Power-On Reset Clears DAC Output to 0 V (Unipolar Mode)
Schmitt Trigger Inputs for Direct Optocoupler Interface

APPLICATIONS
Digital Gain and Offset Adjustment
Automatic Test Equipment
Data Acquisition Systems
Industrial Process Control

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The AD5541 and AD5542 are single, 16-bit, serial input, voltage output DACs that operate from a single 5 V ± 10% supply.

The AD5541 and AD5542 utilize a versatile 3-wire interface that is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards.

These DACs provide 16-bit performance without any adjustments. The DAC output is unbuffered, which reduces power consumption and offset errors contributed to by an output buffer.

The AD5542 can be operated in bipolar mode generating a $\pm V_{REF}$ output swing. The AD5542 also includes Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity.

The AD5541 and AD5542 are available in an SO package.

PRODUCT HIGHLIGHTS

1. Single Supply Operation.
   The AD5541 and AD5542 are fully specified and guaranteed for a single 5 V ± 10% supply.
2. Low Power Consumption.
   These parts consume typically 1.5 mW with a 5 V supply.
3. 3-Wire Serial Interface.
4. Unbuffered output capable of driving 60 kΩ loads.
   This reduces power consumption as there is no internal buffer to drive.
5. Power-On Reset circuitry.

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MICROWIRE is a trademark of National Semiconductor Corporation.

REV. A

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AD5541/AD5542–SPECIFICATIONS

(V_{DD} = 5 V ± 10%, V_{REF} = 2.5 V, AGND = DGND = 0 V. All specifications $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Condition
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy, INL		±0.5	±1.0	LSB	L, C Grades
		±0.5	±2.0	LSB	B, J Grades
		±0.5	±4.0	LSB	A Grade
Differential Nonlinearity		±0.5	±1.0	LSB	Guaranteed Monotonic
			±1.5	LSB	J Grade
Gain Error		–1.5	±5	LSB	T_A = 25°C
			±7	LSB	
Gain Error Temperature Coefficient		±0.1		ppm/°C	
Zero Code Error		0.3	±1	LSB	T_A = 25°C
			±2	LSB	
Zero Code Temperature Coefficient		±0.05		ppm/°C	
AD5542					
Bipolar Resistor Matching		1.000		Ω/Ω	R_{FB}/R_{INV}, Typically $R_{FB} = R_{INV}$ = 28 kΩ
		±0.0015	±0.0076	%	Ratio Error
Bipolar Zero Offset Error		±1	±5	LSB	T_A = 25°C
			±7	LSB	
Bipolar Zero Temperature Coefficient		±0.2		ppm/°C	
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF} – 1 LSB	V	Unipolar Operation
	$-V_{REF}$		V_{REF} – 1 LSB	V	AD5542 Bipolar Operation
Output Voltage Settling Time		1		µs	to 1/2 LSB of FS, C_L = 10 pF
Slew Rate		25		V/µs	C_L = 10 pF, Measured from 0% to 63%
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB Change Around the Major Carry
Digital Feedthrough		10		nV-s	All 1s Loaded to DAC, V_{REF} = 2.5 V
DAC Output Impedance		6.25		kΩ	Tolerance Typically 20%
Power Supply Rejection Ratio			±1.0	LSB	ΔV_{DD} ± 10%
DAC REFERENCE INPUT					
Reference Input Range	2.0		V_{DD}	V	
Reference Input Resistance[2]	9			kΩ	Unipolar Operation
	7.5			kΩ	AD5542, Bipolar Operation
LOGIC INPUTS					
Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.4			V	
Input Capacitance[3]			10	pF	
Hysteresis Voltage[3]		0.4		V	
REFERENCE					
Reference –3 dB Bandwidth		1.3		MHz	All 1s Loaded
Reference Feedthrough		1		mV p-p	All 0s Loaded, V_{REF} = 1 V p-p at 100 kHz
Signal-to-Noise Ratio		92		dB	
Reference Input Capacitance		75		pF	Code 0000 Hex
		120		pF	Code FFFF Hex
POWER REQUIREMENTS					
V_{DD}	4.50		5.50	V	
I_{DD}		0.3	1.1	mA	
Power Dissipation		1.5	6.05	mW	

NOTES

[1]Temperature ranges are as follows: A, B, C Versions: –40°C to +85°C. J, L Versions: 0°C to 70°C.

[2]Reference input resistance is code-dependent, minimum at 8555 hex.

[3]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = 5 V ± 5%, V_{REF} = 2.5 V, AGND = DGND = 0 V. All specifications $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} All Versions	Unit	Description
f_{SCLK}	25	MHz max	SCLK Cycle Frequency
t_1	40	ns min	SCLK Cycle Time
t_2	20	ns min	SCLK High Time
t_3	20	ns min	SCLK Low Time
t_4	15	ns min	$\overline{CS}$ Low to SCLK High Setup
t_5	15	ns min	$\overline{CS}$ High to SCLK High Setup
t_6	35	ns min	SCLK High to $\overline{CS}$ Low Hold Time
t_7	20	ns min	SCLK High to $\overline{CS}$ High Hold Time
t_8	15	ns min	Data Setup Time
t_9	0	ns min	Data Hold Time
t_{10}	30	ns min	$\overline{LDAC}$ Pulsewidth
t_{11}	30	ns min	$\overline{CS}$ High to $\overline{LDAC}$ Low Setup
t_{12}	30	ns min	$\overline{CS}$ High Time Between Active Periods

NOTES

[1]Guaranteed by design. Not production tested.

[2]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Specifications subject to change without notice.

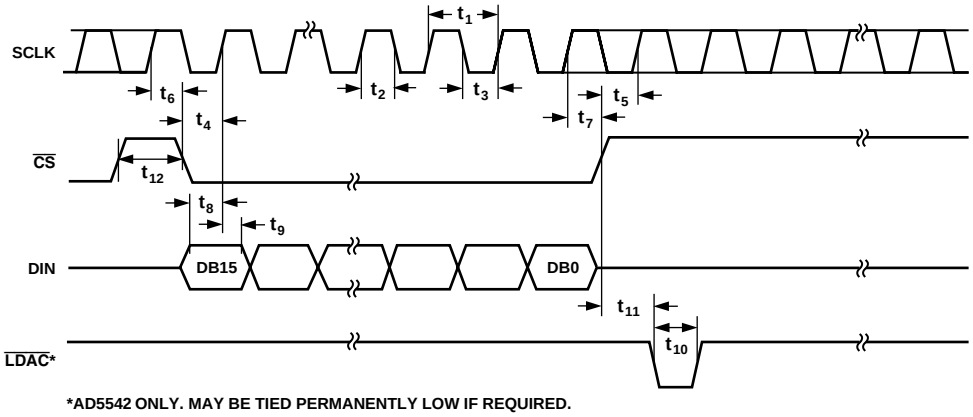


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to AGND . . . . . –0.3 V to +6 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . –0.3 V to V_{DD} + 0.3 V
AGND, AGNDF, AGNDS to DGND . . . . . –0.3 V to +0.3 V
Input Current to Any Pin Except Supplies . . . . . ±10 mA
Operating Temperature Range
Industrial (A, B, C Versions) . . . . . –40°C to +85°C
Commercial (J, L Versions) . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature, (T_J max) . . . . . 150°C
Package Power Dissipation . . . . . (T_J max – T_A)/θ_{JA}
Thermal Impedance θ_{JA}
SOIC (SO-8) . . . . . 149.5°C/W
SOIC (R-14) . . . . . 104.5°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	INL	DNL	Temperature Range	Package Description	Package Option
AD5541CR	±1 LSB	±1 LSB	–40°C to +85°C	8-Lead Small Outline IC	SO-8
AD5541LR	±1 LSB	±1 LSB	0°C to 70°C	8-Lead Small Outline IC	SO-8
AD5541BR	±2 LSB	±1 LSB	–40°C to +85°C	8-Lead Small Outline IC	SO-8
AD5541JR	±2 LSB	±1.5 LSB	0°C to 70°C	8-Lead Small Outline IC	SO-8
AD5541AR	±4 LSB	±1 LSB	–40°C to +85°C	8-Lead Small Outline IC	SO-8
AD5542CR	±1 LSB	±1 LSB	–40°C to +85°C	14-Lead Small Outline IC	R-14
AD5542LR	±1 LSB	±1 LSB	0°C to 70°C	14-Lead Small Outline IC	R-14
AD5542BR	±2 LSB	±1 LSB	–40°C to +85°C	14-Lead Small Outline IC	R-14
AD5542JR	±2 LSB	±1.5 LSB	0°C to 70°C	14-Lead Small Outline IC	R-14
AD5542AR	±4 LSB	±1 LSB	–40°C to +85°C	14-Lead Small Outline IC	R-14

Die Size = 80 × 139 = 11,120 sq mil; Number of Transistors = 1,230.

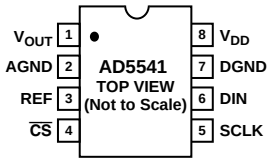
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5541/AD5542 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD5541 PIN FUNCTION DESCRIPTIONS

Mnemonic	Pin No.	Description
V_{OUT}	1	Analog Output Voltage from the DAC.
AGND	2	Ground Reference Point for Analog Circuitry.
REF	3	This is the voltage reference input for the DAC. Connect to external 2.5 V reference. Reference can range from 2 V to V_{DD}.
$\overline{CS}$	4	This is a logic input signal. The chip select signal is used to frame the serial data input.
SCLK	5	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
DIN	6	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
DGND	7	Digital Ground. Ground reference for digital circuitry.
V_{DD}	8	Analog Supply Voltage, 5 V ± 10%.

AD5541 PIN CONFIGURATION
SOIC



AD5542 PIN CONFIGURATION
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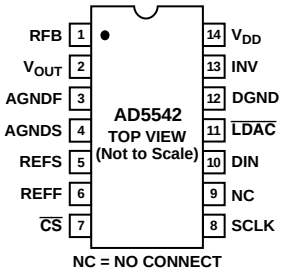


AD5542 PIN FUNCTION DESCRIPTIONS

Mnemonic	Pin No.	Description
RFB	1	Feedback Resistor. In bipolar mode connect this pin to external op amp output.
V_{OUT}	2	Analog Output Voltage from the DAC.
AGNDF	3	Ground Reference Point for Analog Circuitry (Force).
AGNDS	4	Ground Reference Point for Analog Circuitry (Sense).
REFS	5	This is the voltage reference input (sense) for the DAC. Connect to external 2.5 V reference. Reference can range from 2 V to V_{DD}.
REFF	6	This is the voltage reference input (force) for the DAC. Connect to external 2.5 V reference. Reference can range from 2 V to V_{DD}.
$\overline{CS}$	7	This is a logic input signal. The chip select signal is used to frame the serial data input.
SCLK	8	Clock input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
NC	9	No Connect.
DIN	10	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
$\overline{LDAC}$	11	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register.
DGND	12	Digital Ground. Ground reference for digital circuitry.
INV	13	Connected to the Internal Scaling Resistors of the DAC. Connect INV pin to external op amps inverting input in bipolar mode.
V_{DD}	14	Analog Supply Voltage, 5 V ± 10%.

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL versus code plot can be seen in Figure 2.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. Figure 3 illustrates a typical DNL versus code plot.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
This is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero Code Error
Zero code error is a measure of the output error when zero code is loaded to the DAC register.

Zero Code Temperature Coefficient
This is a measure of the change in zero code error with a change in temperature. It is expressed in mV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition. A plot of the glitch impulse is shown in Figure 15.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{CS}$ is held high, while the CLK and DIN signals are toggled. It is specified in nV-s and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa. A typical plot of digital feedthrough is shown in Figure 14.

Power Supply Rejection Ratio
This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power-supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
This is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

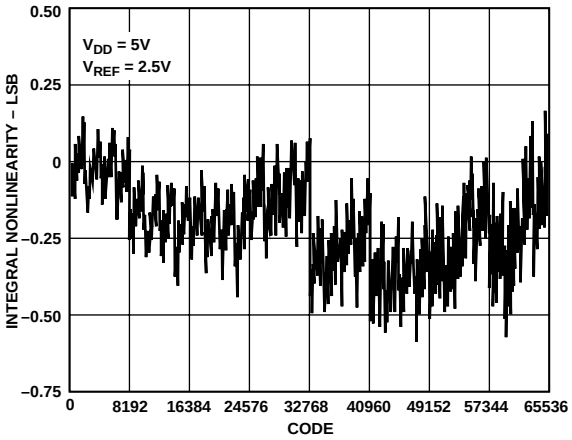


Figure 2. Integral Nonlinearity vs. Code

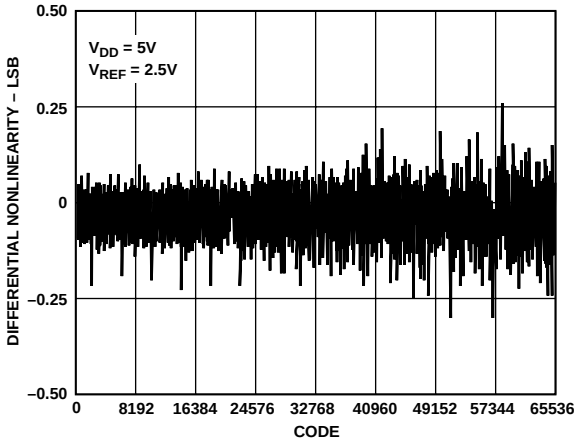


Figure 5. Differential Nonlinearity vs. Code

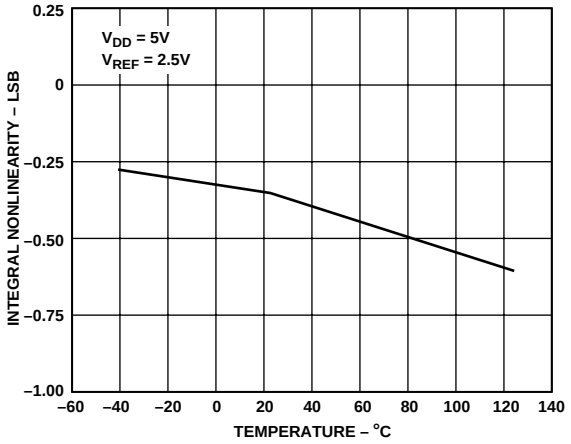


Figure 3. Integral Nonlinearity vs. Temperature

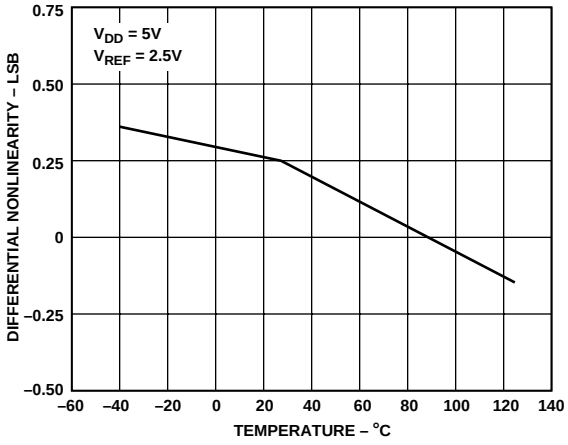


Figure 6. Differential Nonlinearity vs. Temperature

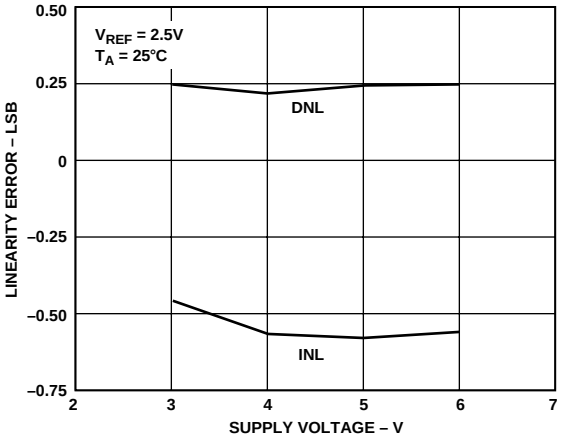


Figure 4. Linearity Error vs. Supply Voltage

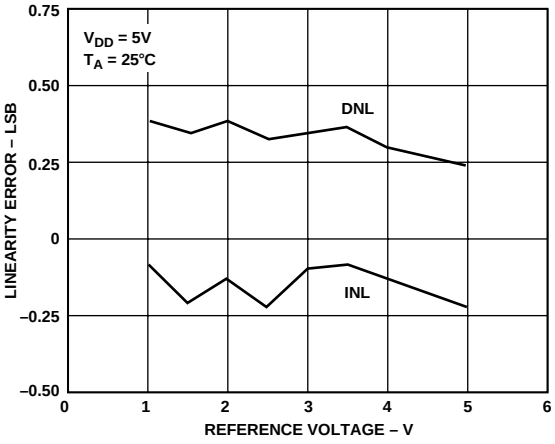


Figure 7. Linearity Error vs. Reference Voltage

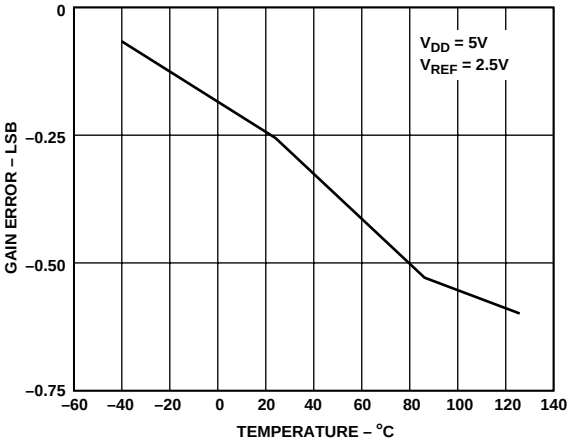


Figure 8. Gain Error vs. Temperature

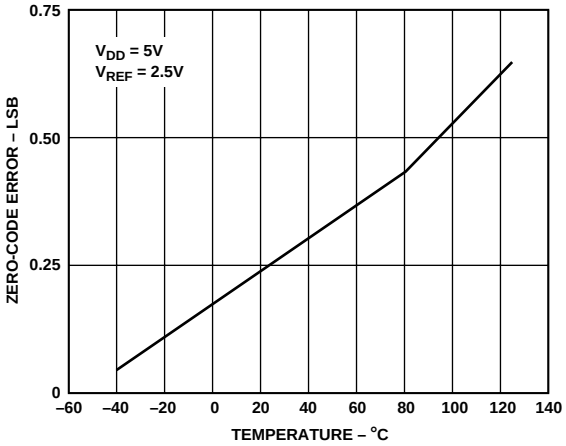


Figure 11. Zero-Code Error vs. Temperature

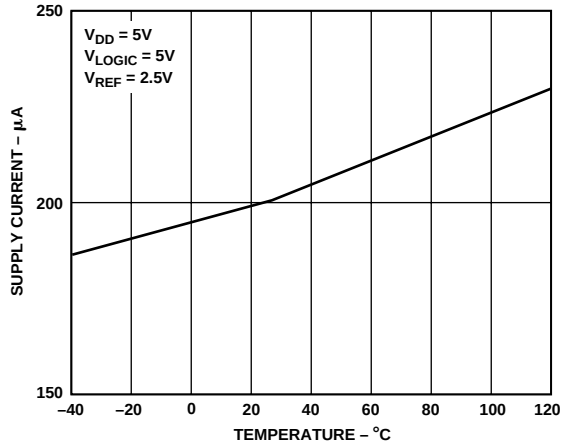


Figure 9. Supply Current vs. Temperature

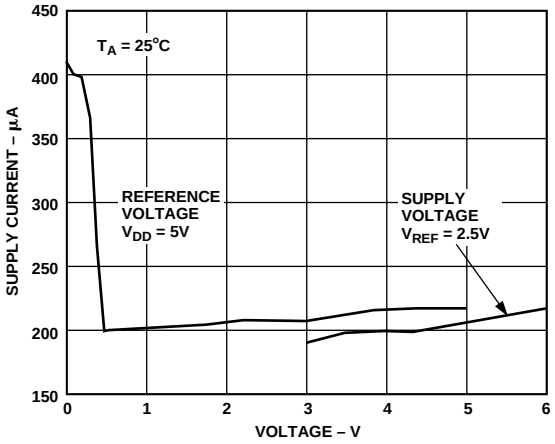


Figure 12. Supply Current vs Reference Voltage or Supply Voltage

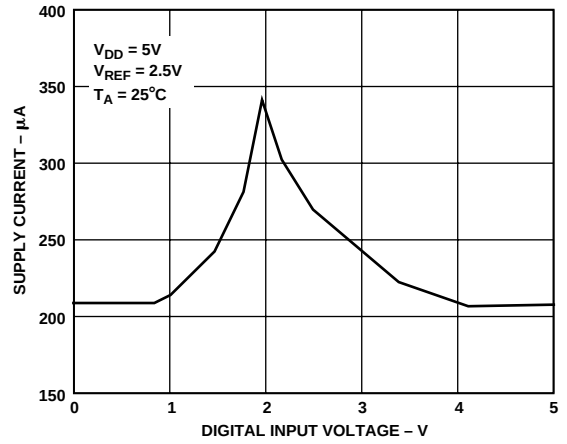


Figure 10. Supply Current vs. Digital Input Voltage

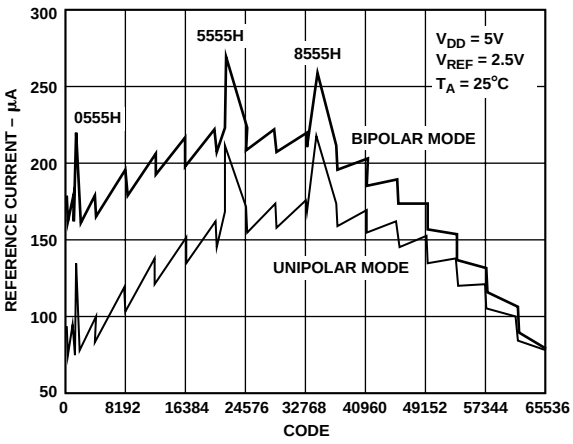


Figure 13. Reference Current vs. Code

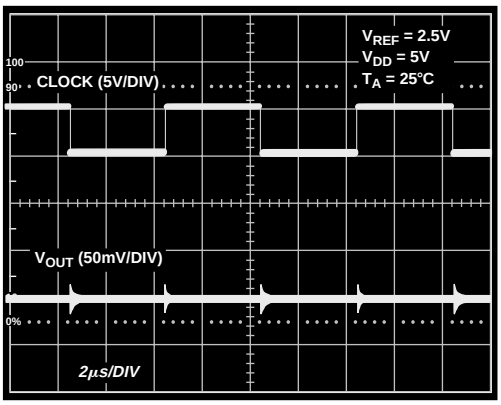


Figure 14. Digital Feedthrough

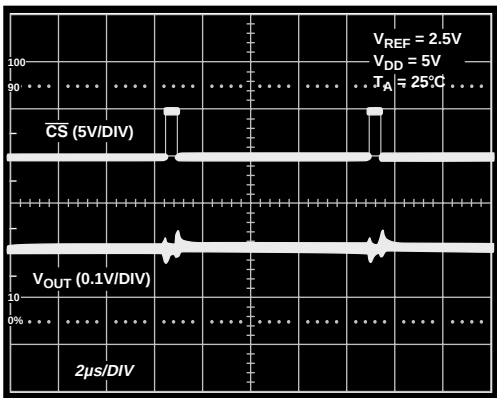


Figure 15. Digital-to-Analog Glitch Impulse

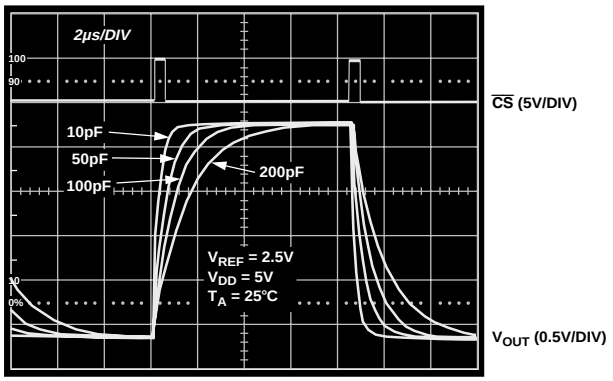


Figure 16. Large Signal Settling Time

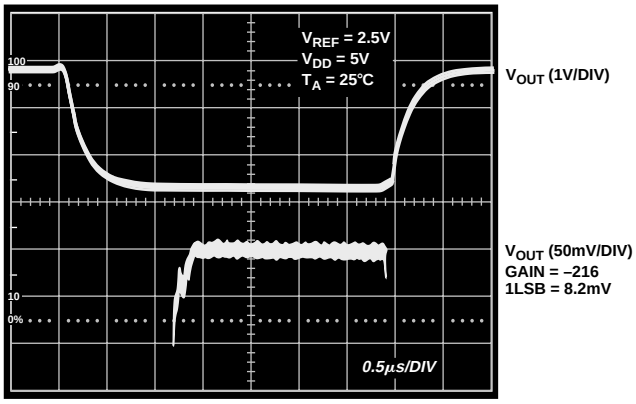


Figure 17. Small Signal Settling Time

GENERAL DESCRIPTION

The AD5541/AD5542 are single, 16-bit, serial input, voltage output DACs. They operate from a single supply ranging from 2.7 V to 5 V and consume typically 300 mA with a supply of 5 V. Data is written to these devices in a 16-bit word format, via a 3- or 4-wire serial interface. To ensure a known power-up state, these parts were designed with a power-on reset function. In unipolar mode, the output is reset to 0 V, while in bipolar mode, the AD5542 output is set to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the AD5542.

Digital-to-Analog Section

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 18. The DAC architecture of the AD5541/AD5542 is segmented. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

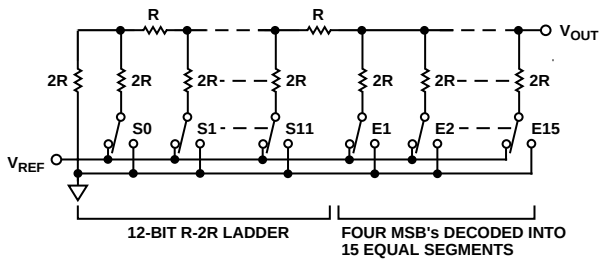


Figure 18. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage as shown in the following equation.

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where D is the decimal data word loaded to the DAC register and N is the resolution of the DAC. For a reference of 2.5 V, the equation simplifies to the following.

$$V_{OUT} = \frac{2.5 \times D}{65,536}$$

giving a V_{OUT} of 1.25 V with midscale loaded, and 2.5 V with full-scale loaded to the DAC.

The LSB size is $V_{REF}/65,536$.

Serial Interface

The AD5541 and AD5542 are controlled by a versatile 3-wire serial interface, which operates at clock rates up to 25 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram can be seen in Figure 1. Input data is framed by the chip select input, $\overline{CS}$. After a high-to-low transition on $\overline{CS}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 16-bit words. After 16 data bits have been loaded into the serial input register, a low-to-high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC. Data can only be loaded to the part while $\overline{CS}$ is low.

The AD5542 has an $\overline{LDAC}$ function that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be maintained high while data is written to the shift register. Alternatively, $\overline{LDAC}$ may be tied permanently low to update the DAC synchronously. With $\overline{LDAC}$ tied permanently low, the rising edge of $\overline{CS}$ will load the data to the DAC.

Unipolar Output Operation

These DACs are capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low-supply current, typically 300 μA, and a low-offset error. The AD5541 provides a unipolar output swing ranging from 0 V to V_{REF}. The AD5542 can be configured to output both unipolar and bipolar voltages. Figure 19 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table I.

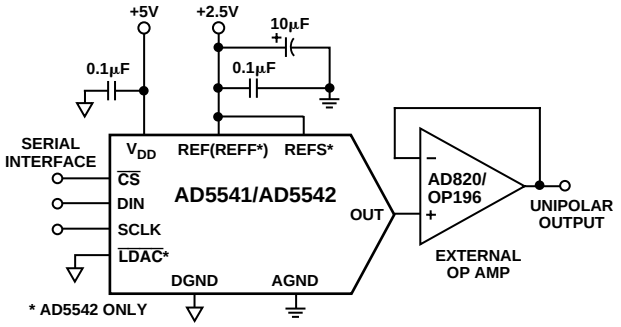


Figure 19. Unipolar Output

Table I. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$V_{REF} \times (65{,}535/65{,}536)$
1000 0000 0000 0000	$V_{REF} \times (32{,}768/65{,}536) = 1/2\ V_{REF}$
0000 0000 0000 0001	$V_{REF} \times (1/65{,}536)$
0000 0000 0000 0000	0 V

Assuming a perfect reference, the worst case output voltage may be calculated from the following equation.

Unipolar Mode Worst-Case Output

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

where

$V_{OUT-UNI}$ = Unipolar Mode Worst-Case Output
D = Code Loaded to DAC
V_{REF} = Reference Voltage Applied to Part
V_{GE} = Gain Error in Volts
V_{ZSE} = Zero Scale Error in Volts
INL = Integral Nonlinearity in Volts

Bipolar Output Operation

With the aid of an external op amp, the AD5542 may be configured to provide a bipolar voltage output. A typical circuit of such operation is shown in Figure 20. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external op amp to achieve this bipolar output swing, typically $R_{FB} = R_{INV} = 28$ kΩ. Table II shows the transfer function for this output operating mode. Also provided on the AD5542 are a set of Kelvin connections to the analog ground inputs.

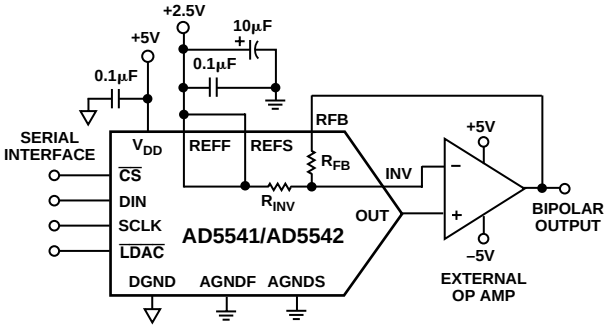


Figure 20. Bipolar Output (AD5542 Only)

Table II. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$+V_{REF} \times (32{,}767/32{,}768)$
1000 0000 0000 0001	$+V_{REF} \times (1/32{,}768)$
1000 0000 0000 0000	0 V
0111 1111 1111 1111	$-V_{REF} \times (1/32{,}768)$
0000 0000 0000 0000	$-V_{REF} \times (32{,}768/32{,}768) = -V_{REF}$

Assuming a perfect reference, the worst-case bipolar output voltage may be calculated from the following equation.

Bipolar Mode Worst-Case Output

$$V_{OUT-BIP} = \frac{\left[\left(V_{OUT-UNI} + V_{OS}\right)\left(2 + RD\right) - V_{REF}\left(1 + RD\right)\right]}{1 + \left(2 + RD\right)/A}$$

where

V_{OS} = External Op Amp Input Offset Voltage
RD = R_{FB} and R_{IN} Resistor Matching Error
A = Op Amp Open-Loop Gain

Output Amplifier Selection

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply. This will provide the $\pm V_{REF}$ output. In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp needs to have very low-offset voltage, (the DAC LSB is 38 μV with a 2.5 V reference), to eliminate the need for output offset trims. Input bias current should also be very low as the bias current multiplied by the DAC output impedance (approximately 6K) will add to the zero code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, hence increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

Force Sense Amplifier Selection

These amplifiers will be single-supply, low-noise amplifiers. A low-output impedance at high frequencies is preferred as they need to be able to handle dynamic currents of up to ±20 mA.

Reference and Ground

As the input impedance is code-dependent, the reference pin should be driven from a low-impedance source. The AD5541/AD5542 operates with a voltage reference ranging from 2 V to V_{DD}. References below 2 V will result in reduced accuracy. The DAC's full-scale output voltage is determined by the reference. Tables I and II outline the analog output voltage or particular digital codes. For optimum performance, Kelvin sense connections are provided on the AD5542.

If the application doesn't require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

Power-On Reset

These parts have a power-on reset function to ensure the output is at a known state upon power-up. On power-up, the DAC register contains all zeros, until data is loaded from the serial register. However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the DAC, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept, and if less than 16 are loaded, bits will remain from the previous word. If the AD5541/AD5542 needs to be interfaced with data shorter than 16 bits, the data should be padded with zeros at the LSBs.

Power Supply and Reference Bypassing

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5541/AD5542 is via a serial bus that uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD5541/AD5542 requires a 16-bit data word with data valid on the rising edge of SCLK. The DAC update may be done automatically when all the data is clocked in or it may be done under control of LDAC (AD5542 only).

AD5541/AD5542–ADSP-2101/ADSP-2103 Interface

Figure 21 shows a serial interface between the AD5541/AD5542 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set to operate in the SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out on each rising edge of the serial clock, an inverter is required between the DSP and the DAC, because the AD5541/AD5542 clocks data in on the falling edge of the SCLK.

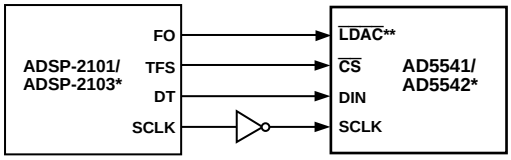


Figure 21. AD5541/AD5542 to ADSP-2101/ADSP-2103 Interface

AD5541/AD5542 to 68HC11 Interface

Figure 22 shows a serial interface between the AD5541/AD5542 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC, while the MOSI output drives the serial data lines SDIN. $\overline{CS}$ signal is driven from one of the port lines. The 68HC11 is configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

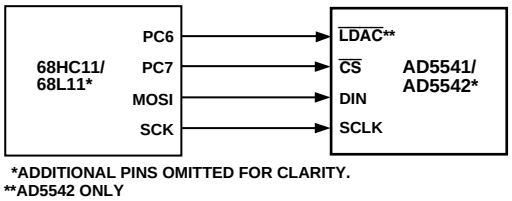


Figure 22. AD5541/AD5542 to 68HC11/68L11 Interface

AD5541/AD5542 to MICROWIRE Interface

Figure 23 shows an interface between the AD5541/AD5542 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the AD5541/AD5542 on the rising edge of the serial clock. No glue logic is required as the DAC clocks data into the input shift register on the rising edge.

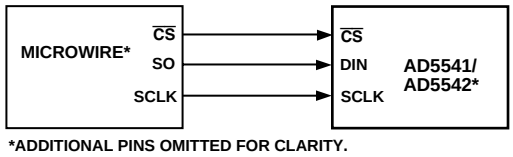


Figure 23. AD5541/AD5542 to MICROWIRE Interface

AD5541/AD5542 to 80C51/80L51 Interface

A serial interface between the AD5541/AD5542 and the 80C51/80L51 microcontroller is shown in Figure 24. TxD of the microcontroller drives the SCLK of the AD5541/AD5542, while RxD drives the serial data line of the DAC. P3.3 is a bit programmable pin on the serial port which is used to drive $\overline{CS}$.

The 80C51/80L51 provides the LSB first, while the AD5541/AD5542 expects the MSB of the 16-bit word first. Care should be taken to ensure the transmit routine takes this into account.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmits its data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the DAC requires a 16-bit word, P3.3 must be left low after the first eight bits are transferred, and brought high after the second byte is transferred. $\overline{LDAC}$ on the AD5542 may also be controlled by the 80C51/80L51 serial port output by using another bit programmable pin, P3.4.

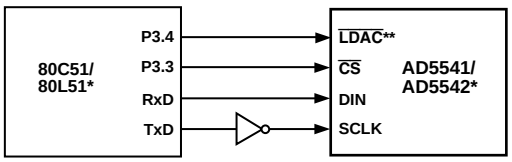


Figure 24. AD5541/AD5542 to 80C51/80L51 Interface

APPLICATIONS

Optocoupler interface

The digital inputs of the AD5541/AD5542 are Schmitt-triggered, so they can accept slow transitions on the digital input lines. This makes these parts ideal for industrial applications where it may be necessary that the DAC is isolated from the controller via optocouplers. Figure 25 illustrates such an interface.

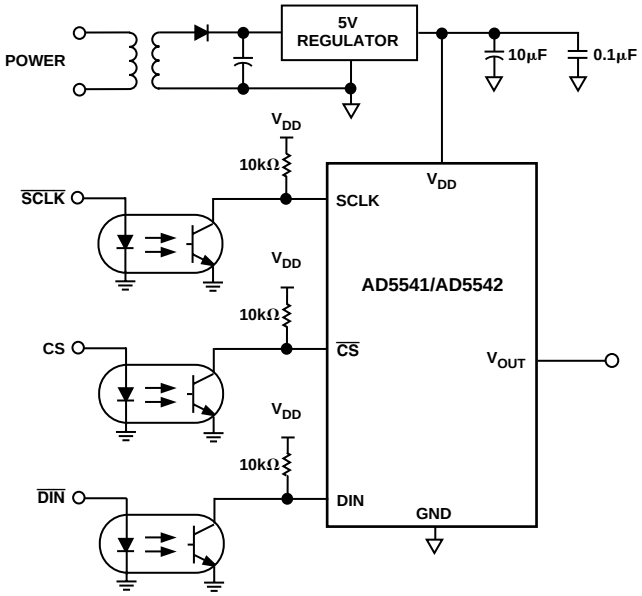


Figure 25. AD5541/AD5542 in an Optocoupler Interface

Decoding Multiple AD5541/AD5542s

The $\overline{CS}$ pin of the AD5541/AD5542 can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device will receive the $\overline{CS}$ signal at any one time. The DAC addressed will be determined by the decoder. There will be some digital feedthrough from the digital input lines. Using a burst clock will minimize the effects of digital feedthrough on the analog signal channels. Figure 26 shows a typical circuit.

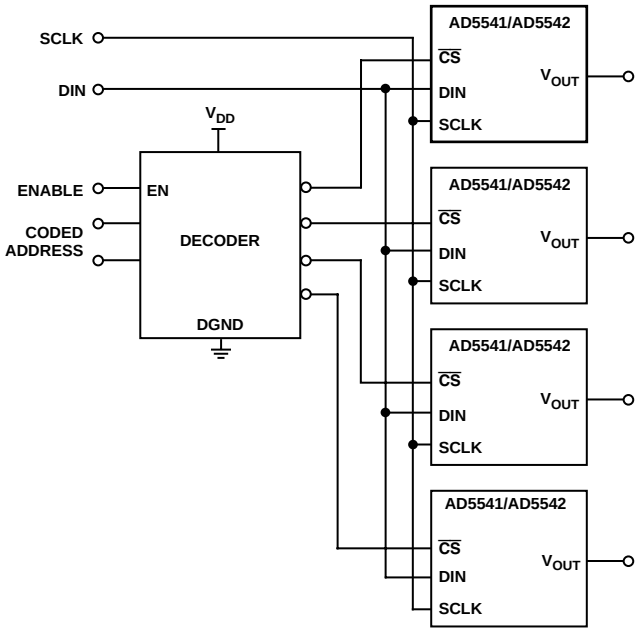


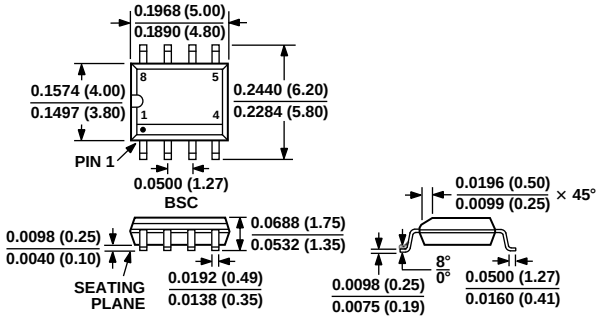
Figure 26. Addressing Multiple AD5541/AD5542s

C3713–8–10/99

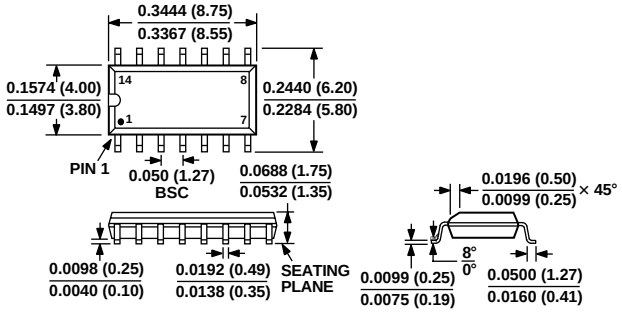
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SO
(SO-8)



14-Lead SO
(R-14)



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