

AD10235

PERFORMANCE FEATURES

Dual Channel, 215MSPS minimum sample rate
SNR = 65 dB @ F_{in} up to 65MHz at 215MSPS
ENOB of 10.3 @ F_{in} up to 65MHz at 215MSPS
(-1dBFS)

SFDR = -80dBc @ F_{in} up to 65MHz at 215MSPS
(-1dBFS)

Input VSWR 1.1:1 to Nyquist

Gain Flatness up to Nyquist: < 0.1dB

LVDS Digital Output Data

400MHz Full Power Analog Bandwidth

Power dissipation = 1.3W typical at 215MSPS per
channel

1.5V Input voltage range

Output data format option

Data Sync input and Data Clock output provided

Interleaved or parallel data output option

APPLICATIONS

Wireless and Wired Broadband Communications

- Wideband carrier frequency systems
- Cable Modem Reverse Path

Communications Test Equipment

Radar and Satellite sub-systems

PRODUCT DESCRIPTION

The AD10235 is a dual 12-bit analog-to-digital converter with a transformer coupled analog input and features low cost, low power, small size and ease of use. The product operates up to 215MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier systems.

The AD10235 requires a +3.3V supply and a differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are Low Voltage Differential Signal (LVDS) compatible. Separate digital output power supply pins support flexible output data formats.

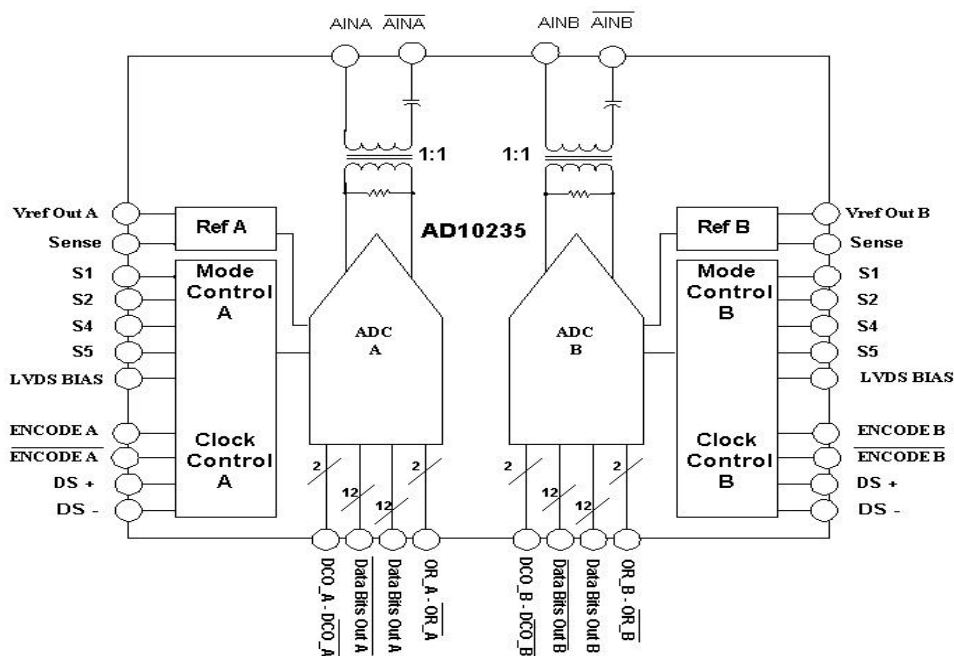
An output data format select option of two's complement or offset binary is supported.

Each channel is completely independent, allowing operation with independent encode and analog inputs. The AD10235 is available in a 40sq-mm, 729-lead PBGA package.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 215MSPS.
2. Input signal conditioning included with full power bandwidth to 400MHz
3. Optimized for IF Sampling.

FUNCTIONAL BLOCK DIAGRAM



AD10235 TARGET SPECIFICATIONS

(DC Specifications ($AV_{DD} = 3.3V$, $DrV_{DD} = 3.3V$; $T_{MIN} = -40^{\circ}C$, $T_{MAX} = +85^{\circ}C$, $Fin = -0.5dBFS$, LVDS Output Mode))

| Parameter | Temp | Test Level | AD10235AB | | | Units |
|---|-------|------------|-----------|----------------------|-------|--------|
| | | | Min | Typical | Max | |
| RESOLUTION | | | | 12 | | |
| ACCURACY | | | | Guaranteed | | |
| No Missing Codes | Full | I | | tbd | | mV |
| Offset Error | +25°C | I | | tbd | | %FS |
| Gain Error | +25°C | I | | tbd | | LSB |
| Differential Nonlinearity (DNL) | +25°C | I | | ±1 | | LSB |
| Integral Nonlinearity (INL) | +25°C | I | | ±1.5 | | LSB |
| TEMPERATURE DRIFT | | | | | | |
| Offset Error | Full | V | | tbd | | ppm/°C |
| Gain Error | Full | V | | tbd | | ppm/°C |
| REFERENCE OUT (V_{REF}) | Full | V | | 1.235 | | V |
| ANALOG INPUT (A_{IN} , $\overline{A_{IN}}$) | | | | | | |
| Input Voltage Range ($A_{IN} - \overline{A_{IN}}$) ¹ | Full | V | | ±.766 | | V |
| Input Resistance | Full | V | | 50 | | Ω |
| Input Capacitance | Full | V | | 5 | | pF |
| SWITCHING PERFORMANCE | | | | | | |
| Maximum Conversion Rate ¹ | Full | I | 215 | | | MSPS |
| Minimum Conversion Rate ¹ | Full | V | | | 40 | MSPS |
| Encode Pulse Width High (t_{EH}) ¹ | Full | V | | 2 | | nS |
| Encode Pulse Width Low (t_{EL}) ¹ | Full | V | | 2 | | nS |
| ENCODE AND DIGITAL I/O | | | | | | |
| INPUTS (ENC, \overline{ENC}) | | | | | | |
| Differential Input Voltage ¹ | Full | IV | 0.2 | | | V |
| Input Resistance | Full | IV | | 5.5 | | KΩ |
| Input Capacitance | Full | IV | | 4 | | pF |
| LOGIC INPUTS (S1, S5) | | | | | | |
| Logic '1' voltage | Full | IV | 2.0 | | | V |
| Logic '0' voltage | Full | IV | | | .8 | V |
| Input Resistance | Full | IV | | 30 | | KΩ |
| Input Capacitance | Full | IV | | 4 | | pF |
| LOGIC OUTPUTS (LVDSMode) ² | | | | | | |
| V_{OD} Differential Output Voltage | Full | IV | 247 | | 454 | mV |
| V_{OS} Output Offset Voltage | Full | IV | 1.125 | | 1.375 | V |
| Output Coding | Full | IV | | Two's comp or Binary | | |
| POWER SUPPLY | | | | | | |
| Supply Voltages | | | | | | |
| AV_{DD} | Full | V | 3.0 | 3.3 | 3.6 | V |
| DrV_{DD} | Full | V | 3.0 | 3.3 | 3.6 | V |
| Supply Current | | | | | | |
| Total I_{ANALOG} ($AV_{DD} = 3.3V$) | Full | V | | 640 | | mA |
| Total $I_{DIGITAL}$ ($DrV_{DD} = 3.3V$) | Full | V | | 110 | | mA |
| POWER SUPPLY REJECTION | Full | V | | ± tbd | | mV/V |
| TOTAL POWER DISSIPATION | Full | V | | 2.5 | | W |

AD10235 TARGET SPECIFICATIONS

(AC Specifications¹ (AV_{DD} = 3.3V, DrV_{DD} = 3.3V; ENCODE = 215MHz; Internal voltage reference, LVDS Output Mode)

| Parameter | Temp | Test Level | AD10235AB | | | Units |
|--|--------|------------|-----------|---------|-----|--------|
| | | | Min | Typical | Max | |
| DYNAMIC PERFORMANCE | | | | | | |
| SNR | | | | | | |
| Analog Input | 10MHz | 25°C | I | 65.5 | | dB |
| @ -0.5dBFS | 65MHz | 25°C | I | 65 | | dB |
| | 100MHz | 25°C | V | 64 | | dB |
| | 240MHz | 25°C | V | 60 | | dB |
| SINAD | | | | | | |
| Analog Input | 10MHz | 25°C | I | 65 | | dB |
| @ -0.5dBFS | 65MHz | 25°C | I | 64.5 | | dB |
| | 100MHz | 25°C | V | 63.4 | | dB |
| | 240MHz | 25°C | V | TBD | | dB |
| Spurious Free Dynamic Range | | | | | | |
| Analog Input | 10MHz | 25°C | I | 82 | | dBc |
| @ -0.5dBFS | 65MHz | 25°C | I | 80 | | dBc |
| | 100MHz | 25°C | V | 76 | | dBc |
| | 240MHz | 25°C | V | 59 | | dBc |
| Two-tone Intermodulation | | | | | | |
| Distortion (IMD) | | | | | | |
| f _{IN} = 29.3MHz; f _{IN} = 30.3MHz | 25°C | V | | tbd | | dBc |
| f _{IN} = 150MHz; f _{IN} = 151MHz | 25°C | V | | tbd | | dBc |
| f _{IN} = 250MHz; f _{IN} = 251MHz | 25°C | V | | tbd | | dBc |
| Analog Input Bandwidth | 25°C | V | | 400 | | MHz |
| OUTPUT Parameters in LVDS Mode ³ | | | | | | |
| Valid Time (t _V) | Full | IV | | tbd | | ns |
| Propagation Delay (t _{PD}) | Full | I | | 3.9 | | ns |
| Rise Time (t _R) (20% to 80%) | 25°C | V | | .5 | | ns |
| FallTime (t _F) (20% to 80%) | 25°C | V | | .5 | | ns |
| DCO Propagation Delay (t _{CPD}) | Full | VI | | 2.9 | | ns |
| Data to DCO Skew (t _{PD} - t _{CPD}) | Full | IV | | 1 | | ns |
| Pipeline Latency | Full | VI | | 14 | | Cycles |
| Aperture Delay (t _A) | 25°C | V | | tbd | | ps |
| Aperture Uncertainty (Jitter, t _J) | 25°C | V | | 0.25 | | ps rms |

NOTES

1. All AC specifications tested by driving ENCODE and ENCODE differentially, LVDS Mode (ENCODE and ENCODE > 200mV.
2. Digital Output Logic Levels: DrV_{DD} = 3.3V, C_{LOAD} = 5pF.
3. LVDS R1 = 100 ohms. LVDS Output Swing Set Resistor = 3.4K.

AD10235

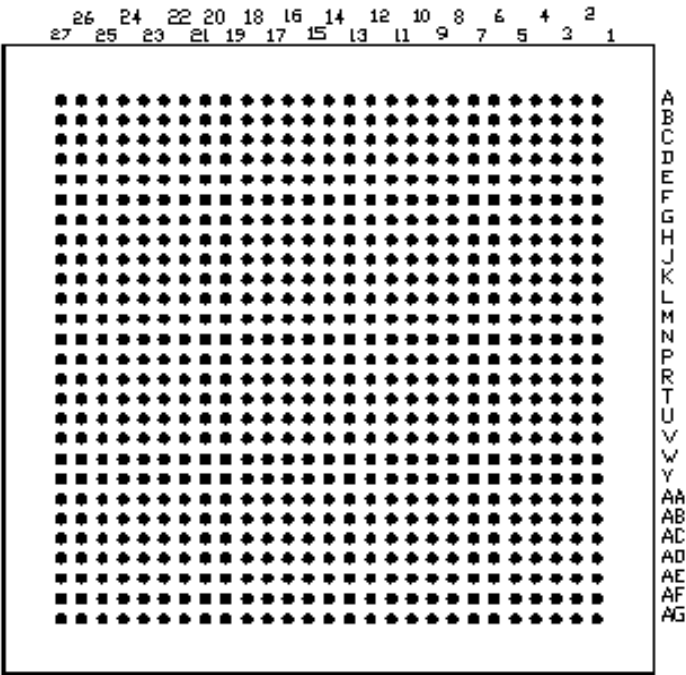
Table 1. AD10235 Output Select Coding¹

| S1 Data Format Select) ² | S5 (Full Scale Adjust) | Mode |
|--|---------------------------------|--|
| 1 | X | 2's Compliment |
| 0 | X | Offset Binary |
| X | 1 | 1.533 Vpp Single- Ended Full Scale -> .766 V _{pp,differential} |
| X | 0 | Full Scale -> 1.533V _{pp,differential} |

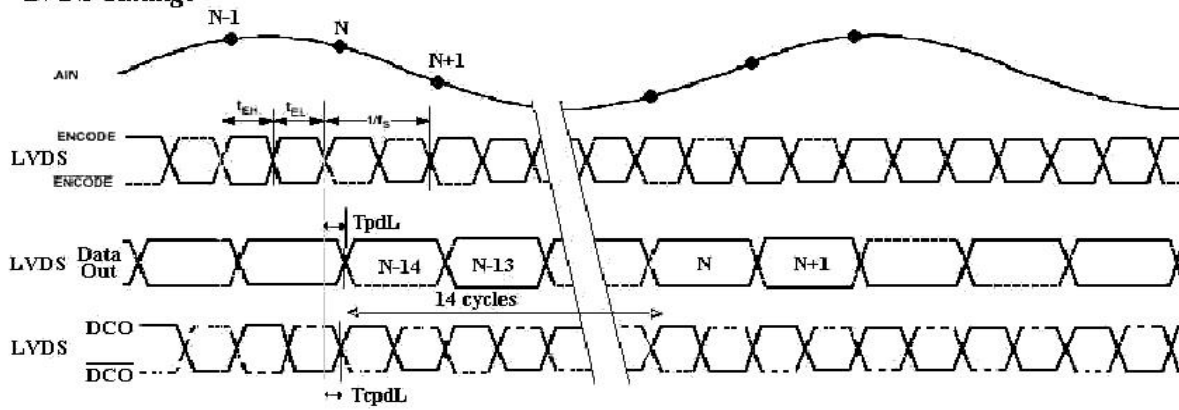
Notes:

- ¹ S1- S5 all have 30K resistive pulldowns on chip
- ² S1 Pin is independent of S5 and sets output coding for both states of S5
- ³ For CMOS output requirements, consult the factory.

Pin Configuration



Bottom View

LVDS Timing:

PRELIMINARY
TECHNICAL
DATA

AD10235

ABSOLUTE MAXIMUM RATINGS

| | |
|------------------------------------|------------------------|
| AVDD, DRVDD | 4V |
| Analog Inputs | -0.5 V to AVDD + 0.5V |
| Digital Inputs | -0.5 V to DRVDD + 0.5V |
| REFIN Inputs | -0.5V to AVDD +0.5V |
| Digital Output Current | 20 mA |
| Operating Temperature | -55°C to + 125°C |
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Maximum Case Temperature | 150°C |
| θ_{JA}^2 | 25C/W, 32C/W |

Notes

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

² Typical $\theta_{JA}^2 = 32C/W$ (heat slug not soldered), Typical $\theta_{JA}^2 = 25C/W$ (heat slug soldered), for multilayered board in still air.

EXPLANATION OF TEST LEVELS

Test Level

- I 100% production tested.
- II 100% production tested at 25°C and sample tested at specified temperatures.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

Caution: ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD10235 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PLANNED GRADES

| Model | Temperature Range | Package Description |
|-------------|-------------------------|---------------------------------|
| AD10235AB | -40°C to 85°C (Ambient) | 40 sq-mm 729 lead PBGA |
| AD10235/PCB | | Evaluation Board with AD10235AB |

PIN FUNCTION DESCRIPTIONS LVDS Mode

| Name | Function in LVDS Mode |
|--------------------|---|
| DNC | Do not connect |
| S5X | Full Scale Adjust pin: High = fullscale is 0.766 Vp-p differential Low = fullscale is 1.533 Vp-p differential |
| S4X | Not used - tie to ground |
| S3X | Test pin - Tie to ground. |
| S2X | Output Mode select. Tie to +3.3V |
| S1X | Data format select. Low = Two's compliment, High = Binary |
| LVDSBIASX | |
| +3.3VAX | 3.3V analog supply (3.0V to 3.6V) |
| AGNDX | Analog ground |
| REFX | 1.235 Reference I/O - function dependent on REFSENSE |
| A _{IN} X- | Analog input - true |
| A _{IN} X+ | Analog input - compliment |
| DSX+ | Data sync (input) - true. Not used in LVDS mode. Tie LOW. |
| DSX- | Data sync (input) - compliment. Not used in LVDS mode. Tie HIGH. |
| <u>ENCX</u> | Clock input - true. (LVPECL levels) |
| ENCX | Clock input - compliment. (LVPECL levels) |
| DrV _{DD} | 3.3V digital output supply (3.0V to 3.6V) |
| <u>DGNDX</u> | Digital Ground |
| <u>D0X</u> | D0 complement output bit (LSB) (LVDS Levels) |
| <u>D0X</u> | D0 true output bit (LSB) (LVDS Levels) |
| <u>D1X</u> | D1 complement output bit (LSB) (LVDS Levels) |
| <u>D1X</u> | D1 true output bit (LSB) (LVDS Levels) |
| <u>D2X</u> | D2 complement output bit (LSB) (LVDS Levels) |
| <u>D2X</u> | D2 true output bit (LSB) (LVDS Levels) |
| <u>D3X</u> | D3 complement output bit (LSB) (LVDS Levels) |
| <u>D3X</u> | D3 true output bit (LSB) (LVDS Levels) |
| <u>D4X</u> | D4 complement output bit (LSB) (LVDS Levels) |
| <u>D4X</u> | D4 true output bit (LSB) (LVDS Levels) |
| <u>DCO_X</u> | Data Clock output - compliment (LVDS Levels) |
| <u>DCO_X</u> | Data Clock output - true (LVDS Levels) |
| <u>D5X</u> | D5 complement output bit (LSB) (LVDS Levels) |
| <u>D5X</u> | D5 true output bit (LSB) (LVDS Levels) |
| <u>D6X</u> | D6 complement output bit (LSB) (LVDS Levels) |
| <u>D6X</u> | D6 true output bit (LSB) (LVDS Levels) |
| <u>D7X</u> | D7 complement output bit (LSB) (LVDS Levels) |
| <u>D7X</u> | D7 true output bit (LSB) (LVDS Levels) |
| <u>D8X</u> | D8 complement output bit (LSB) (LVDS Levels) |
| <u>D8X</u> | D8 true output bit (LSB) (LVDS Levels) |
| <u>D9X</u> | D9 complement output bit (LSB) (LVDS Levels) |
| <u>D9X</u> | D9 true output bit (LSB) (LVDS Levels) |
| <u>D10X</u> | D10 complement output bit (LSB) (LVDS Levels) |
| <u>D10X</u> | D10 true output bit (LSB) (LVDS Levels) |
| <u>D11X</u> | D11 complement output bit (LVDS Levels) MSB |
| <u>D11X</u> | D11 true output bit (LVDS Levels) MSB |
| <u>ORX</u> | Overrange complement output bit (LVDS Levels) |
| <u>ORX</u> | Overrange true output bit (LVDS Levels) |

1 / Notes: X= (A) Channel A or (B) Channel B

AD10235

LVDS Mode Pin Configuration (PCB Footprint)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | |
|----|-----------|-----------|---------|---------|---------|---------|---------|---------|---------|--------|------------|--------|--------|-----------|--------|--------|--------|--------|---------|---------|---------|---------|---------|---------|---------|------------|------------|-------|
| A | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | S1A | S3A | S4A | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| B | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | S1A | S3A | S4A | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | REF B | REF B | |
| C | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | REF A | LVDS BIASA | S2A | S5A | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | LVDS BIASB | LVDS BIASB | |
| D | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | A1NA- | AGNDA | A1NA+ | AGNDA | REF A | LVDS BIASA | S2A | S5A | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | A1NB- | AGNDB | A1NB+ | AGNDB | S1B | S1B |
| E | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | S2B | S2B | |
| F | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | S3B | S3B | |
| G | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | S4B | S4B | |
| H | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | NC | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | S5B | S5B | |
| J | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | |
| K | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | +3.3VAA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | +3.3VAB | |
| L | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| M | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| N | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| P | AGNDA | AGNDA | +3.3VAA | +3.3VAA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | +3.3VAB | +3.3VAB | AGNDB | AGNDB |
| R | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| T | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| U | AGNDA | AGNDA | ENCA | ENCA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | ENCB | ENCB | AGNDB | AGNDB |
| V | AGNDA | AGNDA | ENCA | ENCA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | ENCB | ENCB | AGNDB | AGNDB |
| W | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| Y | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDA | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | AGNDB | |
| AA | NC | NC | NC | NC | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | ORB | ORB | ORB | ORB |
| AB | NC | NC | D0A | D0A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | D11B | D11B | D11B | D11B |
| AC | D0A | D0A | D1A | D1A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND A | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | DGND B | D10B | D10B | D10B | D10B |
| AD | D1A | D1A | D3A | D4A | DCO A | D5A | D6A | D7A | D8A | D9A | D10A | D11A | ORA | +3.3VDIGB | NC | NC | D0B | D1B | D2B | D3B | D4B | DCO B | D5B | D6B | D7B | D9B | D9B | |
| AE | D2A | D2A | D3A | D4A | DCO A | D5A | D6A | D7A | D8A | D9A | D10A | D11A | ORA | +3.3VDIGB | NC | NCB | D0B | D1B | D2B | D3B | D4B | DCO B | D5B | D6B | D7B | D9B | D9B | |
| AF | D2A | D2A | D3A | D4A | DCO A | D5A | D6A | D7A | D8A | D9A | D10A | D11A | ORA | +3.3VDIGA | NC | D0B | D1B | D2B | D3B | D4B | DCO B | D5B | D6B | D7B | D8B | D8B | D8B | |
| AG | +3.3VDIGA | +3.3VDIGA | D3A | D4A | DCO A | D5A | D6A | D7A | D8A | D9A | D10A | D11A | ORA | +3.3VDIGA | NC | D0B | D1B | D2B | D3B | D4B | DCO B | D5B | D6B | D7B | D8B | +3.3VDIGB | +3.3VDIGB | |

TERMINOLOGY

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits

The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76 \text{ dB}}{6.02}$$

ENCODE Pulswidth / Duty Cycle

Pulswidth high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulswidth low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specifications define an acceptable ENCODE duty cycle.

Full-Scale Input Power

Expressed in dBm. Computed using the following equation:

$$Power_{Fullscale} = 10 \log \left(\frac{V_{Fullscale\ rms}^2}{Z_{Input} \cdot .001} \right)$$

Gain Error

Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3dB below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed.

Output Propagation Delay

The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

AD10235

APPLICATION NOTES THEORY OF OPERATION

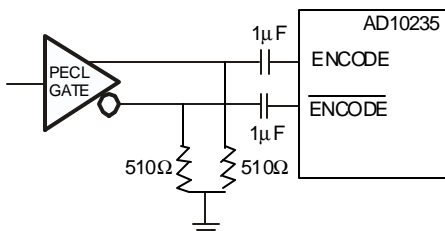
The AD10235 architecture is optimized for high speed and ease of use. The analog inputs drive a wide-bandwidth, high performance transformer circuit, which drives the A/D converter. A unique termination scheme (patent pending) is employed to enhance the input bandwidth. For ease of use, the part includes an onboard reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output logic levels are standard LVDS (ANSI-644 compatible).

USING THE AD10235

ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. An A/D converter's track/hold circuit is essentially a mixer, combining any noise, distortion, or timing jitter on the clock with the desired signal prior to the A/D conversion circuit. For that reason, considerable care has been taken in the design of the ENCODE input of the AD10235, and the user is advised to give commensurate thought to the clock source.

The AD10235 has an internal clock duty cycle stabilization circuit that locks onto the rising edge of ENCODE (falling edge of ENCODE if driven differentially), and optimizes timing internally. This allows for a wide range in input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern, and is not reduced by the internal stabilization circuit. This circuit is always on, and cannot be disabled by the user. The ENCODE and ENCODE inputs are internally biased to 1.5V (nominal), and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. Good performance can be achieved by using an MC10EL16 to drive the encode inputs and provide single-ended to differential conversion, as illustrated in figure below.



Driving Encode with ELI6

Analog Input

The analog input is a differentially ac-coupled high performance 1:1 transformer with an input impedance of 50 Ω . The nominal full scale input is 1.533 V_{p-p}. For best dynamic performance, impedances at A_{IN} and $\overline{A_{IN}}$ are matched. The analog input has been optimized to provide superior wideband performance and requires that the analog inputs be driven differentially. The wideband transformer is used to provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog

inputs are self-biased by an on-chip resistor divider to a nominal 2.8V. (See Equivalent Circuits section TBD.) Special care was taken in the design of the Analog Input section of the AD10235 to prevent damage and corruption of data when the input is overdriven.

Digital Outputs

The AD10235 has been designed to provide LVDS digital outputs. This allows for higher-speed operation while reducing the amount of digital noise coupled into the analog section of the system. CMOS output versions of this device are available. Consult the factory for more information.

LVDS outputs are available when $S2=VDD$ and a 3.4K RSET resistor is placed at pin 7 ($LVDSBIAS$). This resistor sets the current at each output equal to a nominal 3.5mA ($1.2V/RSET$). A 100 ohm differential termination resistor placed at the LVDS receiver inputs results in a nominal 350mV voltage swing at the termination of the line. When operating in LVDS mode, the output supply must be at a DC potential that is greater than or equal to the analog supply level ($AVDD$) using the same power supply for both pins, using an inductor for noise isolation if necessary.

Clock Outputs (\overline{DCO} , \overline{DCO})

Clock output signals are derived from ENCODE and are available off-chip at \overline{DCO} and \overline{DCO} . These clocks can facilitate data latching and other downstream timing functions, providing a low skew clocking solution (see timing diagram). The capacitive loading on these signals should not exceed 5pF, limiting the transient currents associated with such high speed conversion signals. Note that a 100 ohm differential termination resistor is required at the receiver for proper LVDS operation.

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD10235 ($VREF$). An external reference is not required.

AD10235

OUTLINE DIMENSIONS
dimensions shown in mm

