

PM3351 Elan 1x100

2-Port Fast Ethernet Switch Reference Design

PROPRIETARY AND CONFIDENTIAL

ADVANCE

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REFERENCES

- PMC-Sierra PM3351 Datasheet, Issue 2 (July 1997)
- ISO/IEEE 8802.3 CSMA/CD Local Area Networking Specification (1993)
- IEEE 802.3u MAC Parameters, Physical Layer, Medium Attachment Units and Repeater for 100 Mbit/s Operation (January 1995)
- IEEE 802.3x Specification for 802.3 Full Duplex Operation (September 1996)
- National Semiconductor DP83840A Datasheet (1996)
- National Semiconductor DP83223 Datasheet (December 1996)
- National Semiconductor 100BASE-TX Unmanaged Repeater Design Recommendations (Appnote 1010) (October 1995)
- National Semiconductor 10/100 Ethernet Common Magnetics Using DP83840A and the DP83223 (April 1996)

OVERVIEW

This document describes an implementation of a 2-port Fast Ethernet Switch based on PMC-Sierra's PM3351 Elan 1x100 Standard Product. This reference design embodies PMC-Sierra's guidelines and suggestions for designing an Ethernet switch.

This reference design is intended to operate in two modes: 1) Stand-alone mode, where this design provides the complete functionality of a 2-port Fast Ethernet Switch, and 2) This design can interface with other PMC switch reference designs through a PCI expansion backplane. It can be combined with the 24-port PM3350 ELAN 8x10 10Mbit/s Ethernet Switch reference design to form a 24+2 switch or another 2-port Fast Ethernet Switch Reference design to build a 4-port 100 Mbit/s switch.

In addition to the PM3351 Elan 1x100 devices, this reference design incorporates on-board SRAM, EPROM, oscillators, 100BaseT PHY chips (National DP83840A, DP83223 chipset), 100BaseT magnetics, RJ45 jacks, status LEDs and other miscellaneous devices to complete the switch design. A complete list of components can be found in the Bill of Materials.

The Functional Description gives a list of key features of this reference design. The Implementation Description provides a detailed description of all the major components which are found in the schematics (included as Attachment I). The Interface Description lists the RJ45 and the PCI expansion bus pin definitions. The Layout Description describes the component placement guidelines and general layout considerations. For readers who are interested more additional in-depth considerations for this reference design, the Design Consideration section provides many tips and guidelines for high-speed circuit board design and component selection. Finally, a Bill of Materials and the schematics are included at the end.

FUNCTIONAL DESCRIPTION

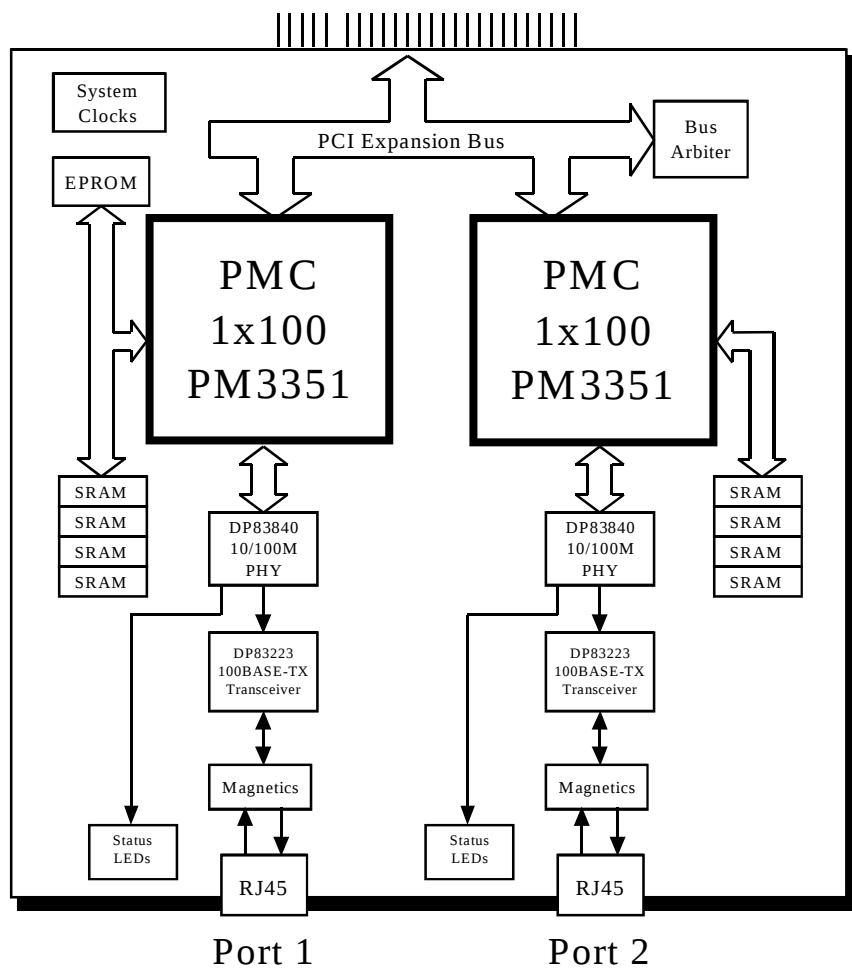
The block diagram of this reference design is shown in Figure 1. The following is a summary of the features offered in this switch.

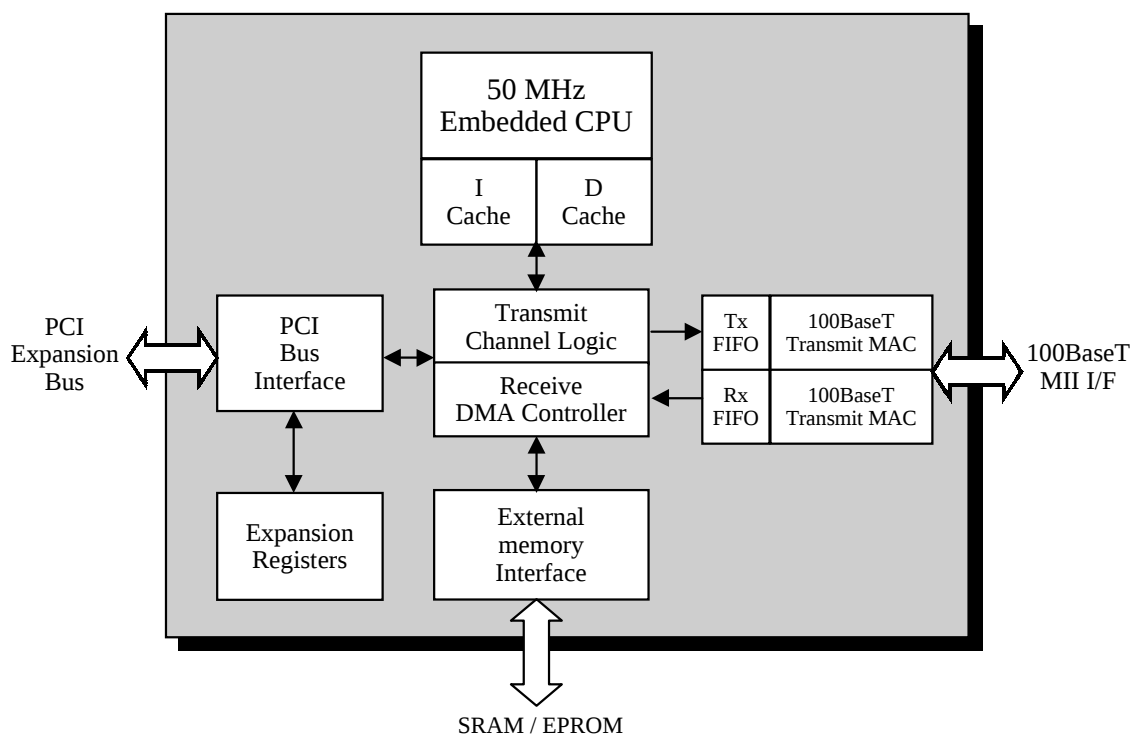
Feature List

- Complete 2-port full-duplex 100BASE-T non-blocking switching
- Operates i) as a completely stand-alone switch, or ii) in conjunction with other switch cards using the PCI expansion bus. It can be combined with the 24-port PM3350 ELAN 8x10 10Mbit/s Ethernet Switch reference design to form a 24+2 switch or another 2-port Fast Ethernet Reference design to build a 4-port 100 Mbit/s switch
- Supports a system bandwidth of 500 - 600 Mbit/s using the PCI expansion bus
- Filters and switches packets using a locally-maintained database¹
- Performs packet switching, IEEE 802.1d compliant transparent bridging, or both
- Store-and-forward mode with full CRC check.

¹ Refer to the System Configuration to determine the number of MAC addresses supported by the firmware programmed into the EPROM. The system can be configured to support up to 32k MAC addresses. See PM3351 datasheet.

Fig. 1 Reference Design System Block Diagram



PM3351 Elan 1x100**Fig. 2 Block Diagram****PM3351 Overview**

The PM3351 is a low-cost, highly integrated stand-alone single-chip switching device for 10/100 Mbit/s Ethernet (IEEE 802.3u, IEEE 802.12) switching and bridging applications. The device supports all processing required for switching Ethernet packets between the on-chip Medium Independent Interface (MII) port and the built-in 1 Gbit/s expansion port, to which other PM3351 devices may be attached.

In addition, the PM3351 is directly compatible with the PM3350, 8-port 10Mbps Ethernet switch chip. The PM3351 can be used with the PM3350 to create non-blocking switches of the configurations shown in the table below, with each 100 Mbit/s port configured for full-duplex and each 10 Mbit/s port configured for half-duplex

All of the initialization, switching, interfacing, management and statistics gathering functions are performed by the PM3351, minimizing the size and cost of a switching

hub with one or more 100 Mbit/s ports. Switch configuration and management can be performed either remotely (in-band), via the on-chip SNMP MIB.

The PM3351 chip contains all the required elements of a high-performance Ethernet switch: an MII interface for connection to physical-layer transceivers, MAC-layer processing logic, buffer FIFOs, a high-speed DMA engine for fast packet transfers, a local memory interface for up to 16 MB of external buffer memory, a fully-compatible PCI bus master and slave unit for modular expansion, and a powerful switch processing unit that implements the switching and bridging functions. The only additional components required for each 100 Mbit/s switch port are an MII compliant transceiver (supports 100BaseTX/FX, 100BaseT4, 100BaseT2, and any future 802.3-compliant 100Mbit MII PHYs), passive line interface devices, a bank of external memory and a system clock. The amount of external memory may be extended up to 4 Mbytes of SRAM, depending on the amount of packet buffering required and the number of MAC addresses to be supported. Switch configuration information is provided to the PM3351 using a single non-volatile device.

Table 1 Non-Blocking Configurations

# PM3350 Devices	# PM3351 Devices	Switch Port Configuration
8	0	64x10
7	1	56x10 + 1x10/100
6	1	48x10 + 1x10/100
5	2	40x10 + 2x10/100
4	2	32x10 + 2x10/100
3	2	24x10 + 2x10/100
2	3	16x10 + 3x10/100
1	4	8x10 + 4x10/100
0	4	4x10/100

IMPLEMENTATION DESCRIPTION

The schematics of the 2-Port Elan 1x100 Reference Design, Revision D, are included in Attachment I.

The core functionality consists of two identical² "ports" or "slices" of 100M circuitry, each using a PM3351, SRAM memory, and physical interface components. Additionally, the board contains an EPROM for code download, PCI Arbiter, connectors, timing sources and miscellaneous "glue" circuitry.

Functional blocks are described below. All of the major components are described for one slice of the 100M circuitry. The same description apply to both slices:

- Port 1: Sheets 3 - 5
- Port 2: Sheets 6 – 8

The component ID's are listed in parenthesis after each component name.

Note that a component designated as PRES in the schematic indicates a signal either 1) pulled-up, 2) pulled-down, or 3) left unconnected (floating).

²Identical except for the EPROM which only PM3351 #1 is connected to.

100M Fast Ethernet Switch Circuitry

PM3351

U14 (SH3), U9 (SH6)

The PM3351 Elan 1x100 chip forms the core of each slice of 100M switch circuitry.

SRAM

U11, U12, U21, U22 (SH4); U1, U2, U19, U20 (SH7)

Four, 128K by 8-bit, 15ns SRAM chips (512K bytes total) are used to provide RAM storage for each PM3351. The SRAM is used for MAC address tables, packet buffer storage, and for data structures required during operation.

EPROM

U10 (SH2)

The board uses a 256K x 8-bit EPROM for the PM3351 boot code, switching code, SNMP code (when available), and any special function code (e.g., custom LED display, aging, backpressure, VLAN, etc.). The EPROM must be 150 ns or faster. Code is downloaded into the first PM3351 device [U14], which in turn will download the code to the other PM3351 device [U9].

If an application code image does not include SNMP management, then a smaller 128K by 8-bit device is adequate.

This device has a socket for ease of replacement.

10/100M Physical Layer Device

U15 (SH5), U6 (SH8)

The National Semiconductor DP83840A is a Physical Layer device for 10BASE-T and 100BASE-Tx Ethernet systems. It contains all the MAC layer functions, and it supports full-duplex operation. It features the Media Independent Interface (MII) which is used to connect to the PM3351 device, and it interfaces with the PMC sublayer through the DP83223 Twister Pair Transceiver. It comes in a 100-pin PQFP package.

U15/U6 Configuration Interface:

SIGNAL NAME	PIN #	DESCRIPTION	PCB REF	CONFIG	SETTING
REQ	29	Equalization Resistor	R83/R4	Open	Tx cable lengths < 100m
RTX	28	Extended Cable Resistor	R95/R3	Open	Tx cable lengths < 100m
AN0	95	Operating Mode	R147/R67	Open	Auto-negotiation enabled
AN1	46	Operating Mode	R96/R7	Open	Auto-negotiation enabled

Please refer to a current issue of the National Semiconductor Databook for additional information describing this 10/100M physical layer device.

Transceiver

U17 (SH5), U7 (SH8)

The National Semiconductor DP83223 TWISTER transceiver interfaces with up to 100 meters of 100 ohm UTP5 cable at 100M data rate. It is compliant with the ANSI X3T12 TP-PMD standard and the IEEE 802.3 100BASE-TX standard. It comes in a 28-pin PLCC package.

Note that MLT-3 encoding is used (100BASE-TX).

U17/U7 Configuration Interface:

SIGNAL NAME	PIN #	DESCRIPTION	PCB REF	CONFIG	SETTING
EQSEL	17	Equalization Select	R151/R73	Open	Adaptive Equalization Mode

Please refer to a current issue of the National Semiconductor Databook for information describing this Twister Pair Transceiver device.

Line Interface Circuitry

The line interface circuitry consists of the transformers, connectors and passive networks necessary to interface the National DP83223A transceiver to cables carrying Ethernet 100 BaseT signals. This circuitry reflects recommendations in the National Semiconductor Databook and associated application notes. Please refer to the Design Considerations section for details on this circuitry.

Transformers

T1 (SH8), T2 (SH5)

Single 100-BASE-TX transformers with common mode chokes are used in this reference design. Dual directional transformers are used to save space and cost, given that the crosstalk between the transmit and the receive is acceptable (better than -35dB). Please refer to the component selection section in Appendix A for vendor information.

RJ45 Connectors

J1 (SH8), J2 (SH5)

There are two RJ45 connectors for connection of Ethernet 100 BaseT segments to the switch. Shielded RJ45 connectors are used to minimize electromagnetic interference (EMI). These connectors are configured as a "hub" connection. Please refer to the Interface Description section for details on pin definition.

PHY Layer LEDs

D8, D9, D10, D11, D12 (SH5); D1, D2, D3, D4, D5 (SH8); D6, D7 (SH4)

There are five LEDs per port, arranged horizontally next to the featured port. They indicate status information as shown in the following table:

D1/D8	<u>Full Duplex LED</u> : Indicates Full Duplex mode status for 100 Mbit/s operation. Inactive in Full Duplex 10 Mbit/s mode.
D2/D9	<u>Collision LED</u> : Indicates the presence of collision activity for 10 Mbit/s and 100 Mbit/s operation. This LED has no meaning for Full Duplex operation.
D3/D10	<u>Receive LED</u> : Indicates the presence of any receive activity.

D4/D11	<u>Transmit LED</u> : Indicates the presence of transmit activity.
D5/D12	<u>Link LED</u> : Indicates Good Link status.

Status LEDs

D6, D7, D13-D26 (SH4/7)

Status LEDs which can be used by the RISC controller to indicate system status.

Common Components

System Clocks

U4, U8 (SH2)

The system clock to the PM3351 devices is sourced from a 50 MHz crystal oscillator [U8]. A 74AC540 buffer [U5] is used to drive the clock signal to each chip.

The PCI bus clock is sourced from a 40 MHz crystal oscillator [U4]. The 74AC540 is also used to drive the clock signal to each PM3351 and the arbiter.

Both oscillators have sockets for ease of replacement. Sockets can be omitted to lower the cost of manufacturing.

PCI Edge Connector Termination Resistors

R164-R171 (SH3)

This set of resistors pull-up the PCI control signals to ensure that they contain stable values when no agent is actively driving the bus. This includes FRAME, TRDY, IRDY, INTA, DEVSEL, STOP, SERR, and PERR.

PCI Bus Connector

P1 (SH2)

This edge connector connects the onboard PCI bus to the expansion port backplane. It is used to interface this board to other reference designs such as the 24-port 10M Ethernet Switch using the PM3350. When this reference design is operating in the stand-alone mode, this edge connector is not used. Please refer to the Interface Description section for the pin definitions.

Note that this PCI connection is not compliant to the PCI specification, v2.1. This is because of 1) the pin redefinition required for PCI arbitration (see the PCI Arbiter description), and 2) the fact that there are more than one "PCI device load" on a single board attached to the bus.

PCI Arbiter

U3 (SH2)

A PCI Arbiter implements a simple round-robin algorithm to control bus access by the PM3351 devices onto the PCI expansion bus. This arbiter is implemented in a 44-PLCC CPLD (Xilinx XC9572). Please contact PMC-Sierra, Ethernet Division, for information on the implementation of the arbiter.

This arbiter should be removed when this reference design board is interfaced to the 24-port 10M Ethernet Switch reference design. In this case, the PCI arbiter on the 24-port reference design assumes control over the PCI bus. Because of this, additional REQ/GNT signals of the PM3351 devices are routed through the PCI bus backplane, which is accomplished by re-defining some of the unused pins on the PCI connector.

This device has a socket for ease of replacement.

Headers and Jumpers

JP1 (SH2) 1-2 3-4	<u>PCI REQ0/1 Enable</u>: If connected, the PM3351 PCI bus request appears at the PCI bus edge connector for processing by an external arbiter. This header is connected only when another reference design is connected to this board, and this board is configured as the slave board (i.e. the PCI arbiter is not populated, and the arbiter on the external board has control of the PCI bus).
JP2 (SH2) 1-2 3-4	<u>PCI GNT0/1 Enable</u>: If connected, PCI grants received from an external arbiter over the PCI bus edge connector are enabled at the PM3351 interface. This header is connected only when another reference design is connected to this board, and this board is configured as the slave board (i.e. the PCI arbiter is not populated, and the arbiter on the external board has control of the PCI bus).
JP3 (SH2)	<u>PCI Clock Source</u>: The clock may be sourced from the on-board oscillator [U4], or from the PCI bus edge connector [P1]. Connecting this header selects the on-board oscillator. Jumper the header when the board is being operated stand-alone, or if the board is the clock source for another reference design.
JP6 (SH3)	<u>Port 1 ERST Enable</u>: Connect the header to implement the watchdog capability of the port 2 PM3351. A watchdog timeout will invoke a system reset.

JP7 (SH2)	<u>PCI Reset Select:</u> Jumper if the board is part of a multi-board system.
JP8-2 (SH2)	<u>PCI Clock Test Point</u>
JP9-2 (SH2)	<u>System Clock Test Point</u>
JP10 (SH2)	<u>PCI Control Signals Test Points:</u> 1=GND, 2=FRAME, 3=IRDY, 4=TRDY, 5=DEVSEL, 6=GND.
JP11 (SH3)	<u>PM3351 U14 Debug Pins</u>
JP12 (SH3)	<u>PM3351 U14 IDSEL:</u> 1-2. Selects PCI Address bit 29. Jumper if (1) the board is used with a PM3350 reference board, or if (2) the board is part of a 4 PM3351 system and is designated as the slave/slave board. 2-3. Selects PCI Address bit 31. Jumper if the board is part of a 4 PM3351 system and is designated as the master/slave board.
JP13 (SH4)	<u>PCI RUN Bit Bank 0:</u> 1-2. Jumper if PM3351 U14 (bank 0) is a slave device. 2-3. Jumper if PM3351 U14 (bank 0) is a master device.
JP14 (SH4)	<u>PM3351 Reserved Bit:</u> 1-2. Default
JP15 (SH4)	<u>PM3351 U14 CHIPID1:</u> 1-2. Jumper if PM3351 U14 is configured as a slave device. 2-3. Jumper if PM3351 U14 is configured as a master device.
JP16 (SH6)	<u>PM3351 U9 Debug Pins</u>
JP17 (SH6)	<u>PM3351 U9 IDSEL:</u> 1-2. Selects PCI Address bit 28. Jumper if (1) the board is used with a PM3350 reference board, or if (2) the board is part of a 4 PM3351 system and is designated as the slave/slave board. 2-3. Selects PCI Address bit 30. Jumper if the board is part of a 4 PM3351 system and is designated as the master/slave board, and is operated in stand-alone mode.
JP18 (SH7)	<u>PM3351 U9 Reserved Bit:</u> 1-2. Default.

JP19 (SH7)	<u>PM3351 U9 CHIPID1:</u> 1-2. Jumper if PM3351 U9 is configured as a slave and U14 is also a slave. 2-3. Jumper if PM3351 U9 is configured as a slave and U14 is a master.
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Reset Debounce Circuit

U23 (SH2)

The Dallas DS1233 "EconoReset" device is used to provide power-up reset and the reset debounce function. It monitors the status of the power supply (Vcc) and will automatically assert the reset when a threshold is crossed. Reset is maintained active for a minimum time of 350ms.

Reset Switch

SW1 (SH2)

This switch is a master reset for the reference design board.

Power Supply Connectors

JK1, JK2 (SH9)

This reference design board requires a 5.0V +/- 5% power supply capable of providing a minimum of 2.5 Amps.

Configuration Resistors

Each "slice" of 100M port circuitry uses a bank of 4.7K ohm resistors to configure the PM3351 after reset. The Configuration Resistors provide the default pull-up/down values on the local memory data bus, which are read by the PM3351 after reset. The resistor functions and default values are given below.

Function	Bank 0	Value	Bank 1	Value	Data Bus
PCIRUN	R197	1	R250	1	D31
RISCRUN	R172	JP13	R251	0	D30
Reserved	R198	JP14	R252	JP18	D29
IMDIS	R199	0	R253	0	D28
PCI3V	R200	0	R254	0	D27
FIRM	R201	0	R255	0	D26
CHIPID [3]	R202	1	R256	1	D25
CHIPID [2]	R203	1	R257	1	D24
CHIPID [1]	R173	JP15	R175	JP19	D23
CHIPID [0]	R204	1	R258	0	D22
RTCDIV [5]	R205	1	R259	1	D21
RTCDIV [4]	R206	1	R260	1	D20
RTCDIV [3]	R207	0	R261	0	D19
RTCDIV [2]	R208	0	R262	0	D18
RTCDIV [1]	R209	0	R263	0	D17
RTCDIV [0]	R210	1	R264	1	D16
MXSEL1	R211	0	R265	0	D15
MXSEL0	R212	1	R266	1	D14
MSLO	R213	0	R267	0	D13
MDCAS	R214	1	R268	1	D12
MTYPE3 [2]	R215	1	R269	1	D11
MTYPE3 [1]	R216	0	R270	0	D10
MTYPE3 [0]	R217	1	R271	1	D9
MTYPE2 [2]	R218	1	R272	1	D8
MTYPE2 [1]	R219	0	R273	0	D7
MTYPE2 [0]	R220	1	R274	1	D6
MTYPE1 [2]	R221	1	R275	1	D5
MTYPE1 [1]	R222	0	R276	0	D4
MTYPE1 [0]	R223	1	R277	1	D3
MTYPE0 [2]	R224	0	R278	0	D2
MTYPE0 [1]	R225	1	R279	1	D1
MTYPE0 [0]	R226	0	R280	0	D0

Configuration Word Functions

PCIRUN: This input to the PM3351 selects the default operating mode of the PCI interface. If logic 1, the device responds to PCI memory space accesses and to be a bus master. If logic 0, the device is disabled from responding to PCI memory space accesses and will not be a bus master.

RISCRUN: A logic 0 halts the Switch Processor upon reset, effectively placing the PM3351 into stand-by mode.

IMDIS: Internal memory disable, which controls the bootcode fetch location. High = boot strapped from the external local memory, Low = boot strapped from on-chip ROM.

PCI3V: This selects the PCI interface signaling environment. High = 3.3V, Low = 5V.

CHIPID: These 4-bits determine the chip's PCI address. This is used to set the second nibble (bits 24 - 27) of the PM3351's address space on the PCI bus. The top nibble (bits 28 - 31) are initialized to zero (0), but can be set by software control if required.

RTCDIV: These 6-bits determine the setting for the Real-Time Clock Divisor.

MTYPE Configuration

These twelve resistors per PM3351 are divided into four groups of three bits each. Each bit combination selects one of eight different memory types. These bits are read off the data bus during start-up, and tell the RISC how to access memory. Each group corresponds to one of the four banks of memory. On the reference design board:

- Bank 0 is configured as type SRAM,
- Bank 1 is configured as type EPROM (unused)
- Bank 2 is configured as type EPROM
- Bank 3 is configured as type EPROM (LED select)

MTYPE	Memory Type	Speed
000	Reserved	n/a
001	Reserved	n/a
010	SRAM	15 ns
011	Reserved	n/a
100	Reserved	n/a
101	EPROM	150 ns
110	EDO DRAM	60 ns
111	EDO DRAM/Fast Page DRAM	60 ns

The memory configuration for this reference design is four 128K x 8bit, 15ns SRAM chips per PM3351.

INTERFACE DESCRIPTION

This section is a detailed description the physical interfaces in this reference design, which include 1) the RJ45 connectors, and 2) the PCI Expansion Bus connector.

RJ45 Pin Definition

Each of the two RJ45 connectors on the reference design have the following pin definition.

Signal Name	Pin	Type	Description
TX+	3	O	Transmit Pair on UTP5 Cable.
TX -	6		
RX +	2	I	Receive Pair on UTP5 Cable.
RX -	1		

The pins are defined such that the port looks like a hub port. This allows a direct cable connection from the switch port to a computer. A crossover cable is needed to connect the switch port to another switch port.

PCI Expansion Bus Interface

Signal Name	Pin	Type	Description
AD[31:0]	B20	I/O	Multiplexed PCI address/data bus, used by the PCI host or the PM3351 to transfer addresses or data.
	A20		
	B21		
	A22		
	B23		
	A23		
	B24		
	A25		
	B27		
	A28		
	B29		
	A29		
	B30		
	A31		
	B32		
	A32		
	A44		
	B45		
	A46		
	B47		
	A47		
	B48		
	A49		
	B52		

	B53 A54 B55 A55 B56 A57 A59 B58		
CBE[3:0]	B26 B33 B44 A52	I/O	Command/Byte-Enable lines. These lines supply a command during the PCI address phase or byte enables during the data phase for each bus transaction.
PAR	A43	I/O	Address/data/command parity, supplies the even parity computed over the AD[31:0] and CBE[3:0] lines during valid data phases; it is sampled (when the PM3351 is acting as a target) or driven (when the PM3351 acts as an initiator) one clock edge after the respective data phase.
FRAME*	A34	I/O	Bus transaction delimiter (framing signal); a HIGH-to-LOW transition on this signal indicates that a new transaction is beginning (with an address phase); a LOW-to-HIGH transition indicates that the next valid data phase will end the currently ongoing transaction.
IRDY*	B35	I/O	Transaction Initiator (master) ready, used by the transaction initiator or bus master to indicate that it is ready for a data transfer. A valid data phase ends with data transfer when both IRDY* and TRDY* are sampled asserted on the same clock edge.
TRDY*	A36	I/O	Transaction Target ready, used by the transaction target or bus slave to indicate that it is ready for a data transfer. A valid data phase ends with data transfer when both IRDY* and TRDY* are sampled asserted on the same clock edge.
STOP*	A38	I/O	Transaction termination request, driven by the current target or slave to abort, disconnect or retry the current transfer.

DEVSEL*	B37	I/O	Device acknowledge: driven by a target to indicate to the initiator that the address placed on the AD[31:0] lines, together with the command on the CBE[3:0] lines, has been decoded and accepted as a valid reference to the target's address space. Once asserted, it is held asserted until FRAME* is de-asserted; otherwise, it indicates (in conjunction with STOP* and TRDY*) a target-abort.
IDSEL	A26	I	Device identification (slot) select. Assertion of IDSEL signals the PM3351 that it is being selected for a configuration space access.
REQ*	B18	O	Bus requests. They are only used when the PCI expansion bus is used to interface with another board, such as the 24-port 10M Ethernet Reference Design. PCI 2.1 specification defines only one Bus Request signal. In this case, the extra Bus Request signals occupy the following unused pins on the PCI connector: B1: -12V (REQ1*), A1: TRST* (REQ0*)
REQ1*	B1		
REQ0*	A1		
GNT*	A17	I	Bus grant from the bus arbiter; this indicates to the PM3351 that it has been granted control of the PCI bus. These are only used when the PCI expansion bus is used to interface with another board, such as the 24-port 10M Ethernet Reference Design. PCI 2.1 specification defines only one Bus Grant signal. In this case, the extra Bus Grant signals occupy the following unused pins on the PCI connector: B7: INTB* (GNT1*), A7: INTC* (GNT0*)
GNT1*	B7		
GNT0*	A7		
INT*	A6	O	Interrupt request. This pin signals an interrupt request to the PCI host.
PERR*	B40	I/O	Bus parity error signal, asserted by the PM3351 as a bus slave, or sampled by the PM3351 as a bus master, to indicate a parity error on the AD[31:0] and CBE[3:0] lines.
SERR*	B42	OD	System error, used by the PM3351 to indicate to the PCI central resource that there was a parity error on the AD[31:0] and CBE[3:0] lines during an address phase.
PCICLK	B16	I	PCI bus clock; supplies the PCI bus clock signal to the PM3351.
RST*	A15	I	PCI bus reset (system reset). Performs a hardware reset of the PM3351 and associated peripherals when asserted.

Note:

- The '*' indicates active-low signals, which corresponds to '#' used in the PCI specification.
- Pin numbers are listed MSB first

LAYOUT DESCRIPTION

Figure 5 shows the layout of this reference design. The purpose of this diagram is to show the Vcc and Ground plane isolation scheme in order to minimize noise-coupling between the various portions of the circuits, and EMI.

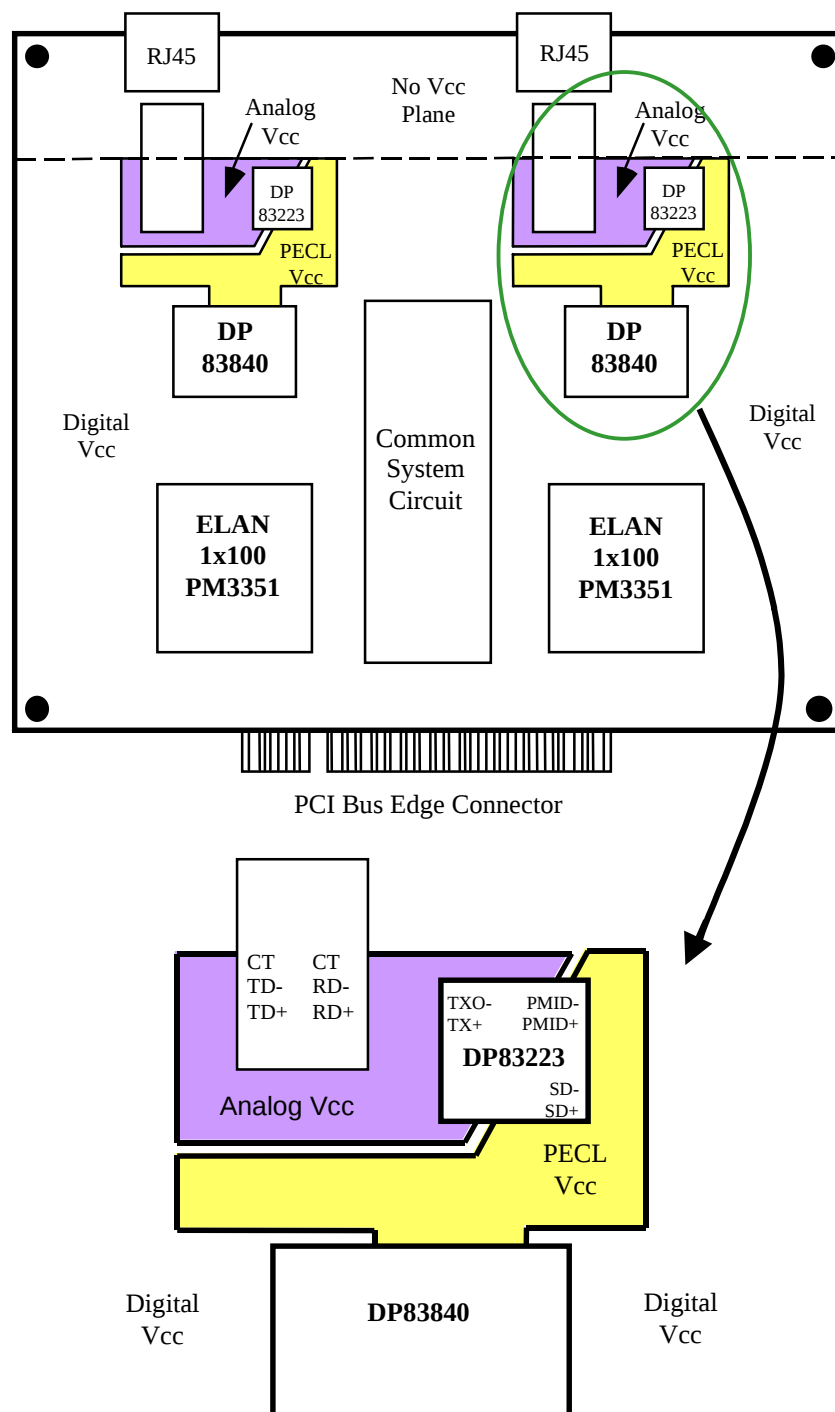
This diagram shows only the approximate placement of the components. *The layout is not meant to guarantee correct operation and performance of the design.* In particular, PHY vendor recommendations should be consulted. Here, the power plane cuts are based on recommendations found in the National Semiconductor 100BASE-TX Unmanaged Repeater Design appnote (Appnote 1010, October 1995).

Power and Ground Plane Isolation

There are three islands of Vcc planes as shown in Fig. 5 for each "slice" of the 100M port circuitry. The Vcc plane cuts are to isolate 1) the Analog high-speed (125Mbps due to 4B/5B encoding) circuitry and traces for the DP83223 and the magnetics, 2) the high-speed (125M PECL due to 4B/5B encoding) digital circuitry and traces for the DP83223 and the DP83840A, and 3) the rest of the lower-speed (max. 50MHz) digital circuitry on the board. Power is fed into the Analog and PECL Vcc planes via ferrite beads (inductors). Important signals on the DP83223 and the DP83840A to be isolated to a specific Vcc plane are shown in the figure. These Vcc islands are on the same Vcc plane with minimum 50 mil separation between any two adjacent islands.

There are two islands of Ground planes as shown for the entire board. The Ground plane cuts are to isolate the "cable" side from the "switch". Chassis ground covers the "cable" side of the magnetics and the RJ45 connector, whereas System ground covers the rest of the board. Chassis ground is used to provide a quiet ground plane for the UTP5 connection and to minimize EMI into and out of the RJ45 connection. A single System ground plane is used to minimize impedance, thus reducing ground noise. The System ground plane overlaps all Vcc islands, which minimizes fringing fields at the edges of the Vcc islands.

To connect the chassis ground island to the system's chassis ground, the mounting screws can be used as chassis ground contact points as they make mechanical contact with the mounting bracket which in turn connects mechanically to the chassis. Furthermore, the shield of the RJ45 connector should be connected to the chassis ground island in order for it to be effective.

Fig. 5 Board Layout

Component Placement

The overall placement strategies of the components are:

- Place the analog circuitry away from the digital circuitry.
- Keep analog transmit side components (mostly passive) separate from the analog receive side components.
- Keep the transformer as close to the RJ45 as possible so that the common-mode noise riding on the traces coming from the RJ45 will be suppressed by the transformer before it can radiate.
- With adequate bypassing and decoupling on the digital side the digital Vcc and ground noise will not propagate to the analog section. Furthermore, additional filtering with ferrite beads on analog power supply reduces noise seen by the analog side, and attenuates noise generated by the analog side. Local decoupling capacitors are also placed near all analog and digital power supply pins.

In addition, the following guidelines are used:

- All source termination resistors are placed near the outputs and load termination resistors are placed near the inputs.
- All pull down resistors are placed near the output pins.
- All decoupling capacitors are placed near the power supply pins. All bypassing capacitors on the analog side are placed near the ferrite beads. The bulk decoupling capacitors (22uF) are placed near the power entrance.

APPENDIX A: DESIGN CONSIDERATIONS

For those who are interested more additional in-depth considerations for this reference design, this Design Consideration section provides many tips and guidelines for high-speed circuit board design and component selection.

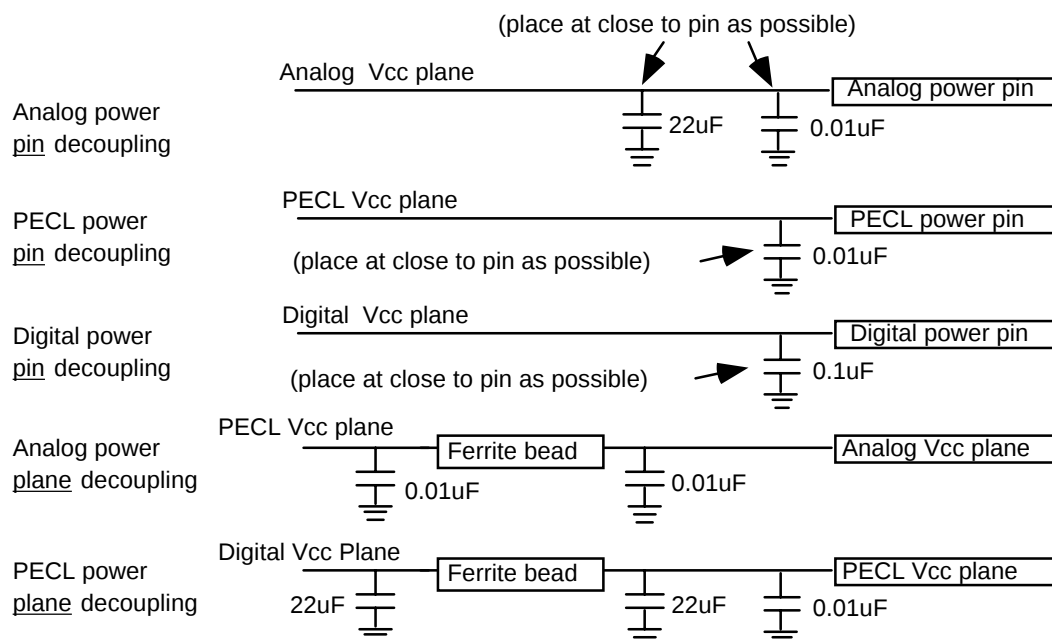
Power Supply Decoupling

Power pins

Analog power supply pins on the DP83840A and DP83223 devices requires special attention to filter out Vcc noise. For the power pins on the PECL Vcc plane and the Analog Vcc plane, a 0.01uF or 0.1uF bypassing capacitor is placed near each power pin, together with 22uF bulk decoupling capacitors for the entire plane.

A 0.01uF or 0.1uF decoupling capacitor is also placed as close to each digital power pin as possible. Ferrite beads are not used on the digital power pins because they add series inductance which limits the current that is required to recharge the decoupling capacitors. If noise attenuation is required, a small surface mount series resistor (1 to 10 ohms) can be added in series with the power pin.

Fig. 6 Power Supply Decoupling



Power planes

Analog circuitry draws mostly constant current and requires little switching current. Therefore, ferrite beads are used to isolate the Analog Vcc plane from the noisy PECL/Digital Vcc plane.

Bulk decoupling is provided for the Digital Vcc islands. 22uF electrolytic capacitors are used for this purpose, and they are placed at the entrance of each Digital Vcc island. In addition, 22uF capacitors are placed after the ferrite bead that feeds power to the PECL Vcc islands.

Please consult the National Semiconductor datasheets for more detail on power supply decoupling of the PHY devices.

Unused CMOS Inputs

"Floating" CMOS inputs (those that are left unconnected) may switch unpredictably, causing unwanted noise and power consumption. Therefore, all unused inputs should be connected to their inactive state: to ground or to the power rail. Unused bi-directionals should be "pulled" through a series resistor (4.7k or greater) to avoid short-circuits occurring if the bi-directionals are erroneously configured as outputs.

Additional Layout Considerations

High-speed Traces

High speed traces should be kept as short as possible in general. This applies to the traces with high-speed data between the RJ45 connector, the magnetics and the DP83223, which carry 125Mbps data (125 Mbit/s is due to the 4B/5B encoding). These traces should be treated as transmission lines, with proper terminations applied (please refer to the schematics for terminations. Also please consult the PHY device vendor datasheets for recommendations on proper termination). In addition, the pair of traces for the differential signals should have the same length, so as to minimize signal distortion and jitter.

The traces with the high-speed data between the RJ45 connector, the magnetics and the DP83223 should have an impedance of 50ohm, in order to match the 100ohm differential impedance of the UTP5 cable. Controlled impedance traces can be used to ensure a 50ohm impedance.

EMI Considerations

EMI can be reduced via proper routing, decoupling, power and ground distribution, shielding, and filtering. Most of the items listed below for EMI improvement also lend themselves towards improving system level performance.

Routing Guidelines

Proper decoupling and termination are effective ways of reducing EMI. The following are some routing guidelines which will help reduce EMI:

- Data lines should be kept away from the clock signals to avoid noise coupling.
- No high speed signals should be routed near the vicinity of the RJ45 modular jack and the transformer in order to prevent common-mode noise coupling onto the cable.
- Footprints of capacitors can be placed along signals with fast rise and fall times. In the event that fast edges causes excessive EMI, they can be slowed down (if timing and system level performance are not compromised) using these capacitors.

Power and Ground planes

- The power plane should be kept away from the RJ45 modular jack and the transformer to prevent noise coupling.
- When separate power planes are used, keep the power planes away from each other. Ensure that for each section of the power plane, there is a ground plane of larger size underneath. The larger ground plane, plus the physical separation of the power planes, will reduce the return current or noise from fringing into adjacent planes. Power planes should also be kept away from the edge of the board to prevent noise fringing between the power and ground planes at the edge of the card and causing unwanted emission.
- Ensure that power and ground planes of different sections do not overlap in order to prevent noise coupling.
- Provide a chassis ground plane under the RJ45 modular jack.

Component Selection

SRAM

The following table shows a selection of compatible SRAM's that can be used in this design:

Vendor	Configuration	Part Number	Package
Toshiba	128K x 8	TC558128AJ-15	32SOJ
Hitachi	128K x 8	HM628127HBJP-15	32SOJ
IDT	128K x 8	IDT71024S15Y	32SOJ

RJ45 Connector

8-pin 8 position RJ45 modular jacks are used in this reference design. There are three types of modular jacks:

- non-filtered and non-shielded
- shielded and non-filtered
- shielded and filtered (capacitive filtering or inductive filtering)

A shielded and non-filtered jack is used in the reference design. Furthermore, in order for the shielding to be effective, the shield should be electrically connected to the chassis ground via a low impedance connection (i.e. using copper finger stocks or firm mechanical contact with the mounting bracket). Typically, the shielded portion of the jack will extend through the opening in the mounting bracket and make firm mechanical contact with the bracket on all sides.

The following vendors provide RJ45 connectors:

- Stewart Connectors Tel: 717-235-7512
- AMP Tel: 800-522-6752
- Kycon Tel: 800-544-6941

- Power Dynamics Tel: 201-736-5722

Transformer

The following transformers are recommended:

- Pulse Engineering PE68515 Tel: 619-674-8100
- Valor PT4171S Tel: 800-318-2567

Both have chokes built-in. They are pin-compatible. PE68515 is selected because of better overall performance.

Oscillator

The on-board oscillators provide a timing reference for the PM3351 device, the National PHY chipset, and the PCI bus interface. The oscillators should be +/-100ppm or better. The stability figure of an oscillator should include any variation due to calibration, temperature, voltage, load, aging, shock, and vibration, and is specified over the life time of the oscillator.

Either CMOS or TTL oscillator can be used. The following is a list of vendors that provide these oscillators:

- Motron Industries Tel: 605-665-9321
- Connor Winfield Tel: 708-851-4722
- Champion Tel: 708-451-1000
- Oak Frequency Control Group Tel: 717-486-3411
- Ecliptek Tel: 714-433-1200

APPENDIX B: BILL OF MATERIALS

This table lists the components used in this reference design. Note that compatible components can be substituted, but this is not guaranteed. Please refer to the Component Selection section in Appendix A for suggestions on alternative sources for some of the major components.

Item	Board ID	Description	Mfgr	Part Number	Qty
1	C1, C2, C3, C4, C5, C6, C9, C10, C11, C16, C23, C24, C26, C27, C28, C29, C30, C31, C32, C35, C36, C37, C38, C40, C41, C42, C43, C44, C45, C47, C51, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C68, C69, C70, C71, C72, C73, C74, C75, C76, C78, C80, C81, C82, C83, C84, C85, C87, C88, C89, C90, C91, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C112, C113, C115, C116, C117, C118, C121, C122, C124, C125, C126, C127, C128, C129, C130, C132, C138, C139, C142, C146, C149, C150, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164	0.1 uF surface mount bypass capacitor, 1206 SMD package	Panasonic	ECU-V1H104KBW	105

2	C7, C8, C25, C46, C50, C52, C53, C54, C66, C79, C86, C93, C131, C135, C140, C141, C145, C147, C151, C152, C153, C154, C165, C166	22 uF surface mount bypass capacitor EIA Size C	Panasonic	ECS-T1AC226R	24
3	C12, C15, C19, C20, C22, C33, C34, C39, C48, C49, C55, C67, C77, C92, C96, C110, C114, C119, C120, C133, C134, C136, C137, C148	0.01uF multi-layer ceramic chip capacitor, 1206 SMD package	Panasonic	ECU-V1H103KBM	24
4	C13, C14, C17, C94, C95, C98	1000 pF multi-layer ceramic chip capacitor, 0805 SMD package	Panasonic	ECU-V1H102KBM	6
5	C18, C97	9 pF multi-layer ceramic chip 0805 SMD package	Panasonic	ECU-V1H090DCN	2

Item	Board ID	Description	Mfgr	Part Number	Qty
6	C21, C111	0.001 uF 2KV ceramic disc capacitor	Panasonic	ECK-D3D102KBP	2
7	C123	500 pF 1206 SMD			1
8	C143, C144	10 uF EIA Size B			2
9	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26	LED			26
10	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8	Ferrite Bead 1206 SMD package	Murata	BLM31A700SPTM-03	8
11	JP1, JP2	4 pin double row header 0.100 inch spacing	Sullins	PZC04DACN	2
12	JP3, JP6, JP7, JP8, JP9	2 pin single row header 0.100 inch spacing	Sullins	PZC02SACN	3
12.1	JP10	Header 6			1
12.2	JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19	Header 3			9
13	J1, J2	Single RJ45 jack with shield, 8 position	AMP	558505-1	2
14	Q1, Q2, Q3, Q4, Q5, Q6	NPN transistor SOT-23 package	National	MMBT2222A	6
15	-----				
16	-----				

Item	Board ID	Description	Mfgr	Part Number	Qty
17	R1, R2, R3, R4, R5, R7, R8, R10, R13, R15, R16, R20, R21, R24, R25, R34, R44, R45, R57, R63, R64, R67, R68, R70, R71, R73, R76, R77, R78, R79, R83, R86, R87, R90, R95, R96, R97, R99, R102, R106, R107, R109, R111, R113, R116, R124, R133, R138, R147, R148, R149, R151, R153, R154, R155, R156, R157, R164, R165, R166, R167, R168, R169, R170, R172, R173, R175, R176, R177, R178, R179, R197, R198, R199, R200, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R278, R279, R280, R289, R290	4.7K ohm, 5%, 0.1W chip resistor 0805 SMD package	Panasonic	ERJ-6GEYJ4.7K	134
18	R9, R14, R17, R23, R27, R30, R103, R108, R112, R118, R121, R128	51 ohm, 0805 SMD			12

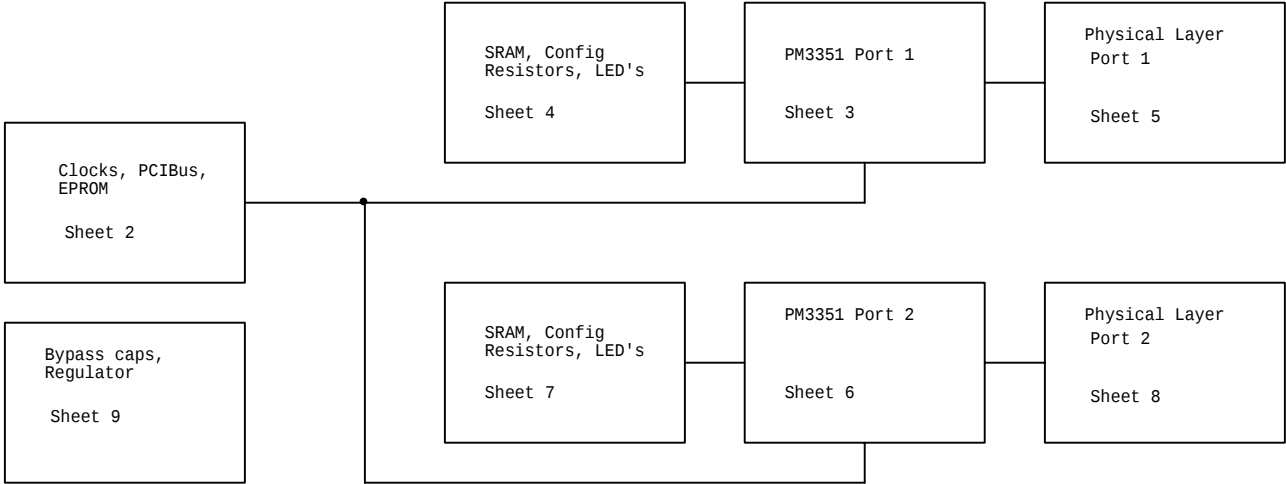
19	R6, R11, R12, R19, R33, R50, R98, R100, R101, R105, R123, R130	10 ohm, 0805 SMD			12
20	R18, R22, R104, R110	47 ohm, 0805 SMD			4

Item	Board ID	Description	Mfgr	Part Number	Qty
21	R26, R36, R47, R55, R61, R65, R119, R122, R127, R139, R141, R144	82 ohm, 0805 SMD			12
22	R28, R31, R115, R120	39 ohm, 0805 SMD			4
23	R29, R32, R51, R53, R56, R66, R117, R125, R131, R140, R143, R145	130 ohm, 0805 SMD			12
24	R35, R48, R126, R132	75 ohm, 0805 SMD	Panasonic	ERJ-6ENF75	4
25	R38, R40, R41, R42, R43, R46, R58, R81, R84, R85, R88, R89, R91, R93, R94, R136, R162, R163, R174, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R192, R193, R194, R195, R196, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249	22 ohm, 0805 SMD			24
26	R49, R129	511 ohm, 0805 SMD			2

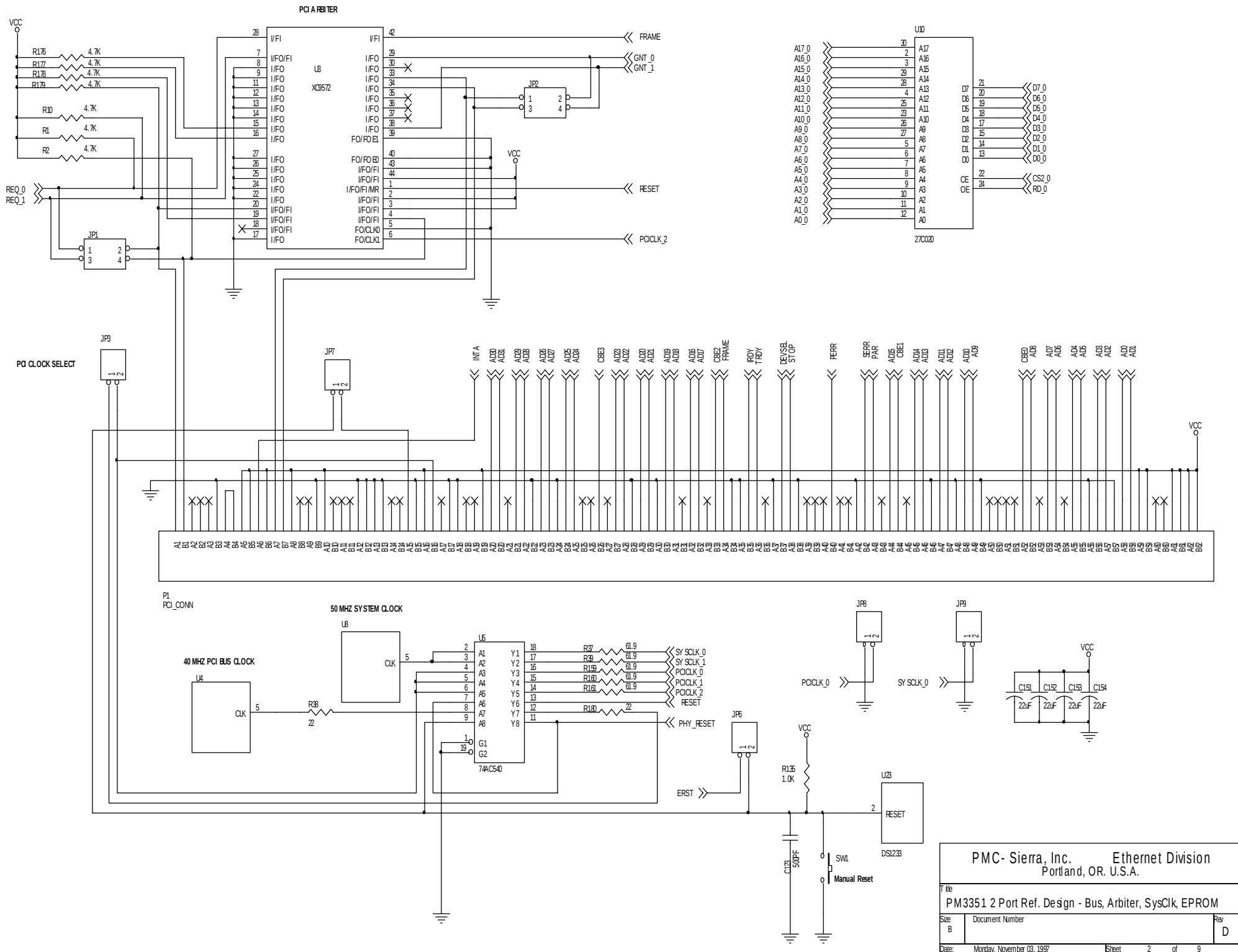
27	R52, R54, R62, R69, R72, R137, R142, R146, R150, R158	680 ohm, 0805 SMD			10
28	R59, R92, R135	1.0K ohm, 0805 SMD			5
29	R74, R152	3.9 ohm, 0805 SMD			2
30	R80, R82, R227, R228, R229, R230, R231, R232, R281, R282, R283, R284, R285, R286, R287, R288	390 ohm, 0805 SMD			2
31	R171	2.7K ohm, 0805 SMD			1
32	SW1	Pushbutton SW	Panasonic	EVQ-QEC05K	1
33	T1, T2	10/100M LAN Transformer	Pulse Engineering	PE-68515L	2
34	U1, U2, U11, U12, U19, U20, U21, U22	128K x 8 SRAM, 32SOJ	Hitachi	HM628127HBJP-15	8
35	U3	CPLD	XILINX	XC9572-15	1
36	U4	40.0 MHz TTL Clock Oscillator 8 pin DIP	Epson America	SG-531PH-40.000MC	1
37	U8	50.0 MHz TTL Clock Oscillator 8 pin DIP	Epson America	SG-531PH-50.000MC	1
38	U5	Inverting Tri-State Buffer	National Semi	74AC540	1
39	U6, U15	10/100M Ethernet Physical Layer 100 pin PQFP	National Semi	DP83840AVCE	2

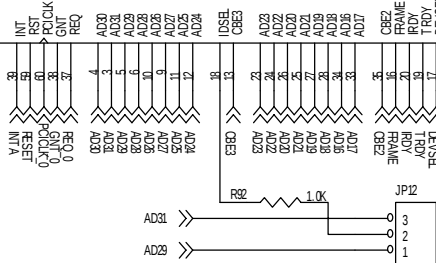
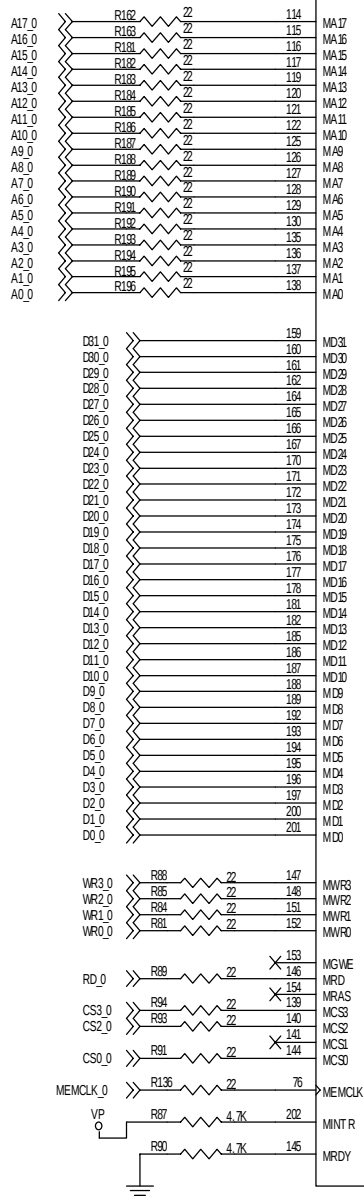
Line	Board ID	Description	Mfgr	Part Number	Qty
40	U7, U17	100BASE-TX Transceiver 28 PLCC	National	DP83223VCE	2
41	U9, U14	Fast Ethernet Switch IC metal package	PMC-Sierra	PM3351	2
42	U10	EPROM, 1M bit; 256K x 8 32DIP package	AMD	AM27C020 -150DC	1
43	U13, U24	Octal D Flip-Flop	National Semi	74AC825SC	1
44	U18	3.3 V Regulator, 4.6 A	Linear Technology	LT1585CT-3.3	1
45	U23	Econo Reset	Dallas	DS1233	1
46	JK1	Banana jacks - red	E.F. Johnson	111-0102-001	1
47	JK2	Banana jacks - black	E.F. Johnson	111-0103-001	1

ELAN 1x100: 2 Port 10/100 Mbit/s Switch

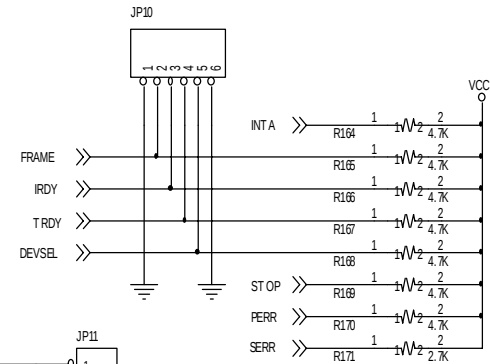
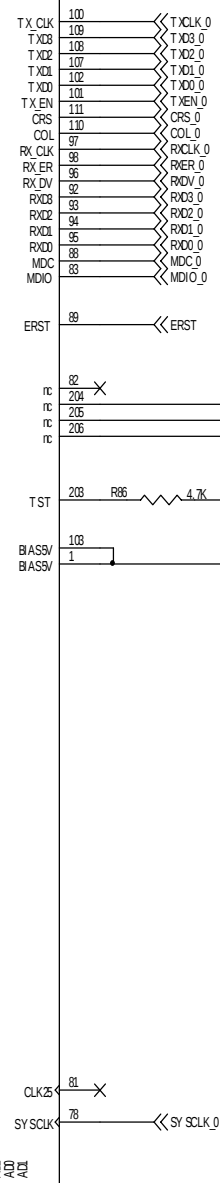


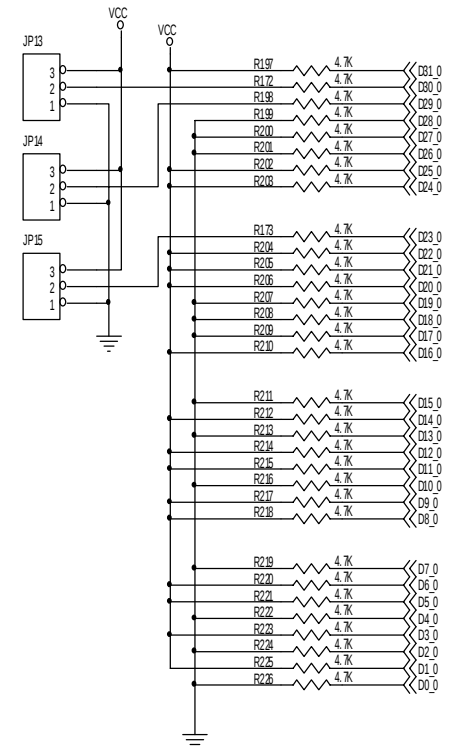
PMC - Sierra, Inc. Ethernet Division Portland, OR. U.S.A.		
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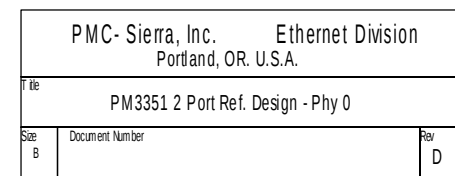


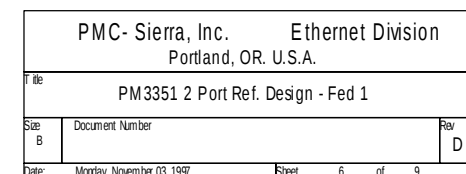


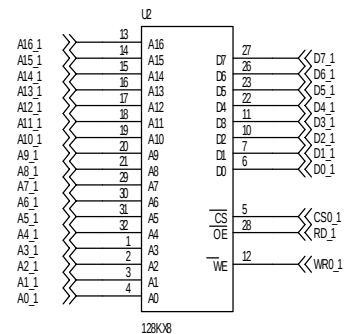
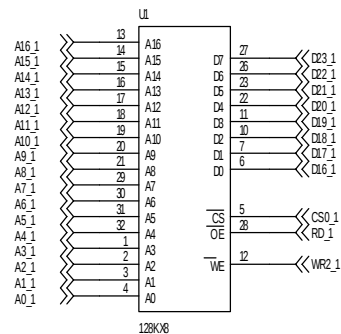
U14
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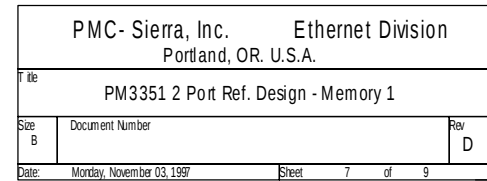


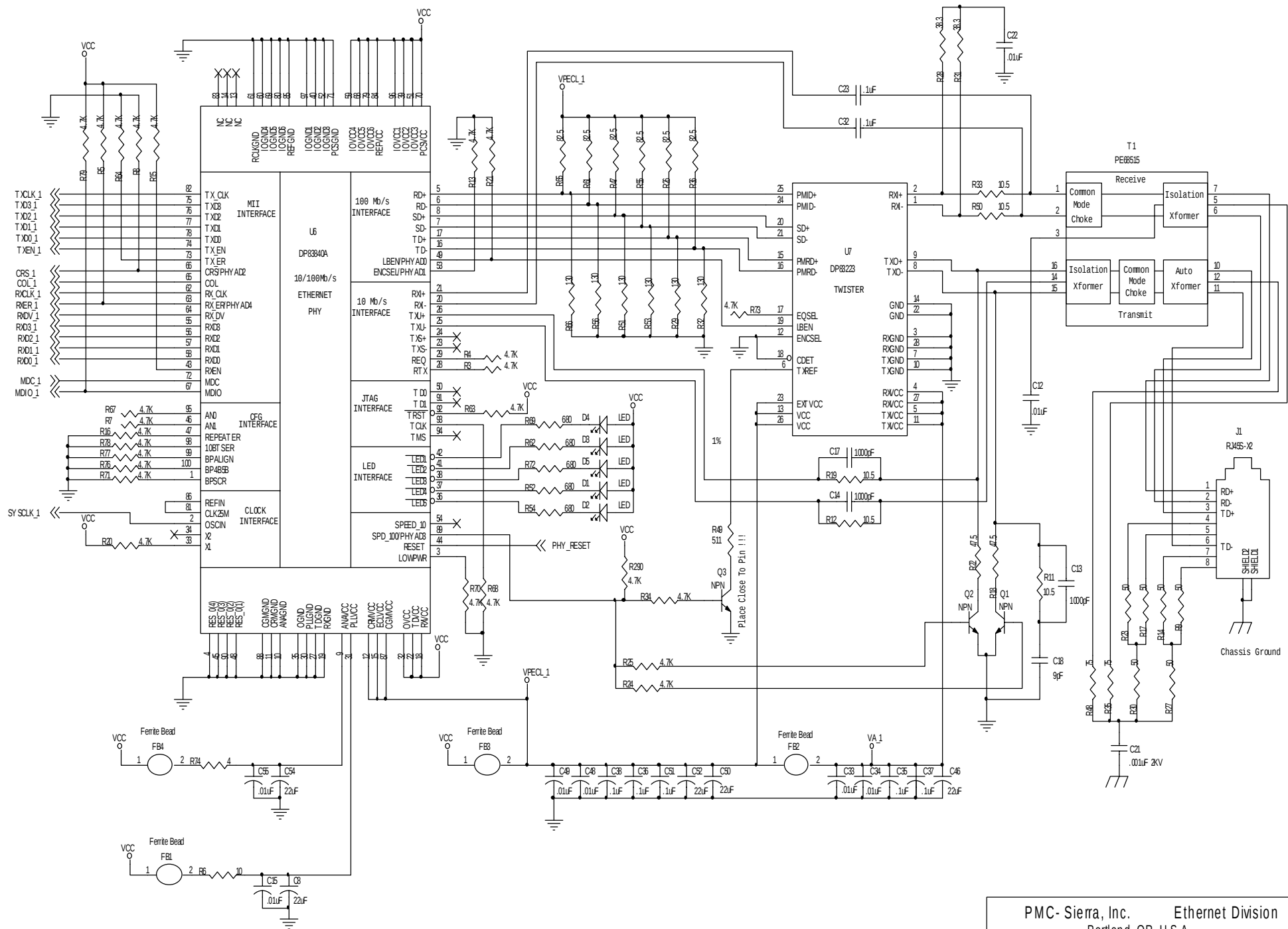


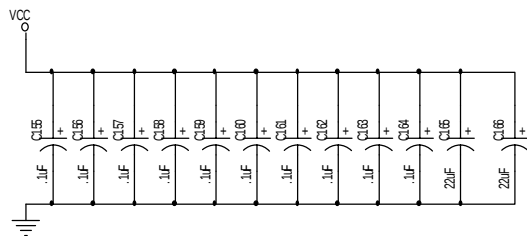
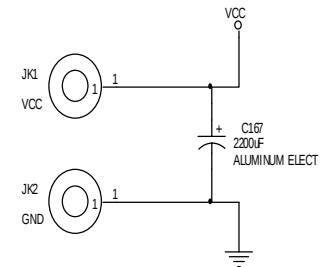
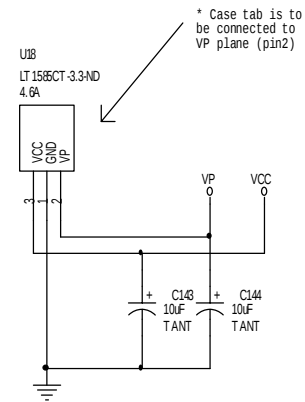
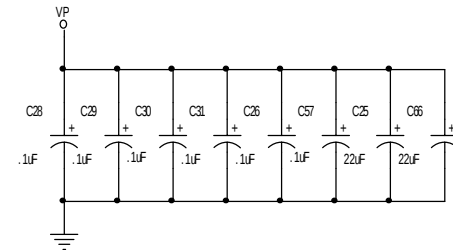
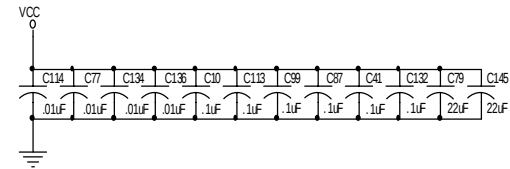
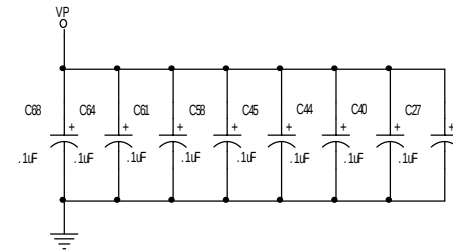
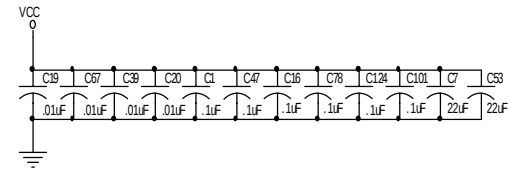
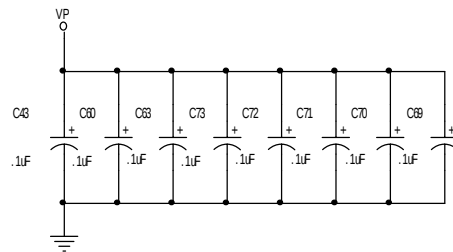




The schematic diagram illustrates the internal architecture of the R2000 CPU. It features two 3-pin connectors, JP18 and JP19, which are connected to a VCC supply and ground. The VCC supply is connected to the top pin of both connectors. The ground connection is made to the bottom pin of JP19. The internal components include a series of resistors (R250 through R280) connected to the VCC supply. These resistors are labeled with their values (4.7K) and are connected to various internal nodes. The diagram also shows a series of output signals, labeled D81.1 through D80.1, which are connected to the internal nodes. The output signals are labeled with their values (4.7K) and are connected to various internal nodes. The diagram also shows a series of output signals, labeled D81.1 through D80.1, which are connected to the internal nodes. The output signals are labeled with their values (4.7K) and are connected to various internal nodes.







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