

PM7345 S/UNI-PDH

AVOIDING BUS CONTENTION ON THE S/UNI-PDH UTOPIA INTERFACE

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BACKGROUND

PMC-Sierra has issued an errata (PMC-950649R2) for the PM7345 S/UNI-PDH product. One of the items in that errata concerns the tristate operation of the RSOC and FRDATA[7:0] outputs while the device is in the reset state. The errata is that these signals will not be tristated during a reset, even if the TSEN input is active.

This errata implies that bus contention could occur if multiple S/UNI-PDHs sharing the same RSOC and FRDATA[7:0] bus are simultaneously held in reset. The question naturally arises: What is the effect of such contention on the integrity of a S/UNI-PDH device?

A second occasion where the RSOC and FRDATA[7:0] outputs may not be tristate, despite TSEN being active, is during the time between the application of power to the S/UNI-PDH and the first reset of the device. This case arises because the state of the S/UNI-PDH registers cannot be determined after power up (the default values given in the data book refer only to the values after a reset). In the S/UNI-PDH there is a FIFOBYP bit in Register 00H which, if powered up as a logic one, will override the tristate function of the TSEN input.

This latter case implies that bus contention could occur when multiple S/UNI-PDHs sharing the same RSOC and FRDATA[7:0] bus are simultaneously powered up. Again the same question: What is the effect of such contention on the integrity of a S/UNI-PDH device?

This document investigates the answer to this question and specifies guidelines for avoiding and limiting the duration of the contention state.

RELIABILITY ISSUES RELATED TO BUS CONTENTION

There are three potential reliability issues related to driving a contended bus: hot electron damage, fusing of wire bonds, and overheating. Each of these issues is dealt with separately below.

In the following analysis, it is assumed that bus contention can be modeled as a short circuit. Additionally, it will be assumed that the device is trying to drive the contending signals to a logic low state (i.e. n-channel driver is turned on). Lastly, it will be assumed that all nine outputs are contending. This is a very worst case scenario.

HOT ELECTRON DAMAGE

Typically, peak hot electron damage occurs when the gate bias is between 40 and 50 percent of the drain bias.^[1] On a contending bus, the gate bias will be at VDD; therefore, the hot electron damage will be on the same order as during normal operation.

Thus hot electron damage will not be significantly increased due to bus contention.

FUSING OF WIRE BONDS

The wire bonds for the signals in question on the S/UNI-PDH are 1 mil gold wires. less than 40 mil in length. For such wires, wire bond fusing current (or glow current) is 650 mA DC.^[2] The rated current is half this: 325 mA DC.

PMC-Sierra characterization of the n-channel output drivers used on the S/UNI-PDH shows that the short circuit current at the fastest environmental corner (-40 C and 5.5 V) is a maximum of 75 mA.

Since this current is much less than the wire bond glow current rating, fusing will not occur due to bus contention.

OVERHEATING

The maximum transient chip temperature is specified to be 150 C over ambient.

For a given power dissipation, the time to heat a given volume of silicon to by specific temperature difference is given by:

$$t = \frac{mcT}{P} = \frac{mcT}{nVI}$$

where t is time to heat (s)
 m is mass of silicon affected (g)

- c is specific heat of silicon (0.7 J/g-C)
- P is power dissipation (W)
- n is number of shorted output drivers
- V is the supply voltage to the output drivers (V)
- I is the current drive of the shorted output drivers (A)

The estimated mass of silicon heated by each driver is 7.9 μg . Therefore, the mass heated by nine drivers is 71 μg .

Thus, substituting values into the equation:

$$t = \frac{mcT}{nVI} = \frac{(71 \times 10^{-6})(0.7)(150)}{(9)(5.5)(75 \times 10^{-3})}$$
$$t = 2.0 \text{ ms}$$

This shows that temperature build-up is the prime reliability factor associated with bus contention.

A 100% engineering margin should be added to the specification:

PMC-Sierra therefore specifies that the S/UNI-PDH should not be operated in a condition of output contention for more than a maximum of 1.0 ms.

The two situations where contention can commonly occur are: during the period following the application of power to the S/UNI-PDH, and during a reset state. The duration of these conditions (separately or in combination) should be limited to a maximum of 1.0 ms.

RECOMMENDATIONS FOR MAINTAINING RELIABILITY

There are a variety of ways to design with the S/UNI-PDH such that bus contention does not affect reliability. Besides a software work-around method (which allows a reset without affecting the tristate operation), the duration of the indeterminate power up state and the duration of the reset state must be limited. One way for meeting this goal is to use a monostable multivibrator circuit to limit the duration of the reset signal. Each of these points is explained in the following subsections.

SOFTWARE WORK-AROUND METHOD

It is possible to perform a software reset of the S/UNI-PDH while maintaining the outputs in tristate. This can be accomplished by taking advantage of a tristate function available in a test mode of the S/UNI-PDH.

The steps are:

- 1) Program Register 80H to a value of 01H. This sets the HIZIO bit which will tristate all outputs (except the data bus on the microprocessor port).
- 2) Program Register 04H to a value of 80H. This sets the RESET bit, initiating a software reset of the S/UNI-PDH.

Note that, although not explicitly stated in the data book, Register 80H is the only register in the S/UNI-PDH which is not returned to a default value due to a software reset — it is returned to default only due to a *hardware* reset.

- 3) Program Register 04H to a value of 00H. This clears the RESET bit, exiting the reset state.
- 4) Program Register 80H to a value of 00H. This clears the HIZIO bit, returning to normal operation.

This work-around has been verified both by inspection of the design and by testing in PMC-Sierra's Conformance Laboratory.

Whenever possible, it is recommended that the S/UNI-PDH device be reset in the above manner (i.e. using the HIZIO bit to maintain tristate operation), rather than directly applying a hardware or software reset. This will avoid any contention on the UTOPIA bus.

LIMIT DURATION OF INDETERMINATE STATE AFTER POWER UP

The data book for the S/UNI-PDH gives default values for the internal registers. These default values refer to the values these registers go to in response to a reset. The registers will not necessarily go to their default values after power is applied — a reset is necessary to ensure this.

Therefore, for the period between the application of power to the S/UNI-PDH and the first reset, the register bits are in an indeterminate state. One of the bits, FIFOBYP in Register 00H, can override the TSEN pin's control of the tristate operation on the UTOPIA bus. Thus, if the FIFOBYP powers up in a logic one state, there is potential for contention on the UTOPIA bus outputs. For this reason, the following recommendation is made.

It is recommended that the duration between the application of power to the S/UNI-PDH and the time of the first reset should be limited to a maximum of 1.0 ms.

This implies that a reset should be performed fairly quickly after power up. This reset could either be software or hardware induced, but (if the reset is not performed with the above software work-around method) then the duration of the reset pulse itself must be included in the limit of 1.0 ms.

LIMIT DURATION OF RESET STATE

It is recommended that the duration of the reset state should be limited to a maximum of 1.0 ms.

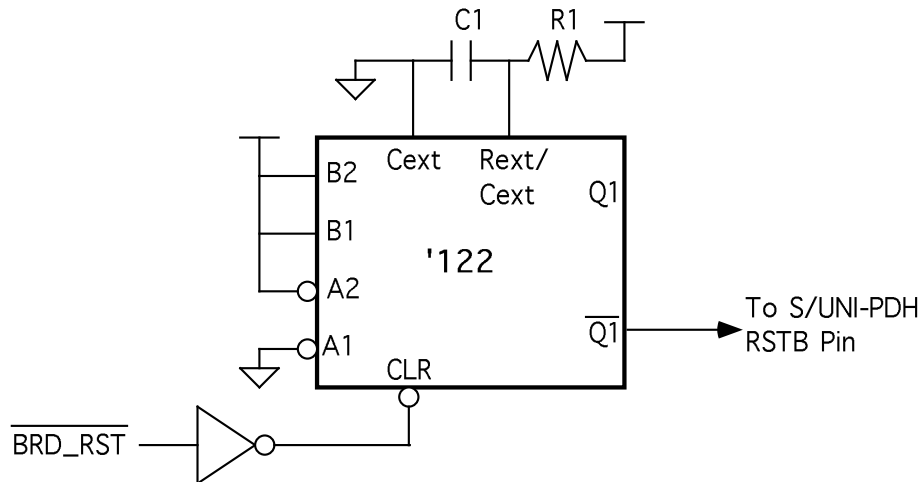
Note: Because the reset on the S/UNI-PDH is asynchronous, the minimum duration of the reset pulse is only 10 ns to ensure that the registers and state machines are returned to their default states.

EXAMPLE CIRCUIT TO LIMIT RESET DURATION

This section contains a suggestion for converting a board-level reset signal into a signal compatible with the 1.0 ms reset pulse width restriction.

The board reset signal can be passed through an monstable multivibrator circuit, the output of which will provide the hardware reset signal to the RSTB pin of the S/UNI-PDH. The multivibrator will convert the board reset signal into a pulse of limited duration. This latter signal would assert RSTB for durations much less than the 1.0 ms maximum.

An retriggerable monstable multivibrator is required. The 74LS122 is a suitable device.^[4] The circuit in Figure 1 can be used:

Figure 1. A Monostable Multivibrator Circuit

The duration of the reset pulse to the S/UNI-PDH is set by the time constant C_1R_1 .

For the 74LS122, the values could be: $R_1 = 5\text{ k}\Omega$, $C_1 = 100\text{ pF}$. This will produce a reset pulse width of approximately 300 ns.

REFERENCES

- [1] Sze, S. M., "Physics of Semiconductor Devices"
- [2] Mil-Std-M-38510H, paragraph 3.5.5.3
- [3] Wolf & Tauber, "Silicon Processing for the VLSI Era"
- [4] Motorola, 1993, "Fast and LS TTL Data"

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