

PM7322

**RCMP
REFERENCE DESIGN**

Issue 2: September 9, 1996

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REFERENCE

- [1] PM7322 RCMP-800 Long Form Datasheet, PMC-940904, Issue 5
- [2] PM7323 RCMP-200 Long Form Datasheet, PMC-960543, Issue 1
- [3] PM5346 S/UNI-155-LITE Databook
- [4] PM5347 S/UNI-155-PLUS Long Form Datasheet, PMC-941033, Issue 4
- [5] PM5348 S/UNI-DUAL Long Form Datasheet, PMC-960338, Issue 1
- [6] PM5355 S/UNI-622-LITE Databook
- [7] PM7344 S/UNI-MPH Databook
- [8] PM7345 S/UNI-PDH Databook
- [9] SCI-PHY Level 2, PMC-940212, Issue 3
- [10] UTOPIA Level 2 Specification, Version 0.8, ATM Forum
- [11] "RCMP Frequently Asked Questions" appnote, PMC-951043, Issue 1
- [12] "RCMP Software Driver Detailed Design" appnote, PMC-960345, Issue 2
- [13] "RCMP in Egress Operation" appnote, PMC-951205, Issue 2
- [14] "Asynchronous SRAM For RCMP-200" appnote, PMC-960338, Issue 1
- [15] Broadband Switching System (BSS) Generic Requirements, GR-1110-CORE, Issue 1
- [16] Motorola MC68340 Integrated Processor with DMA User's Manual, MC68340UM/AD, Rev.1

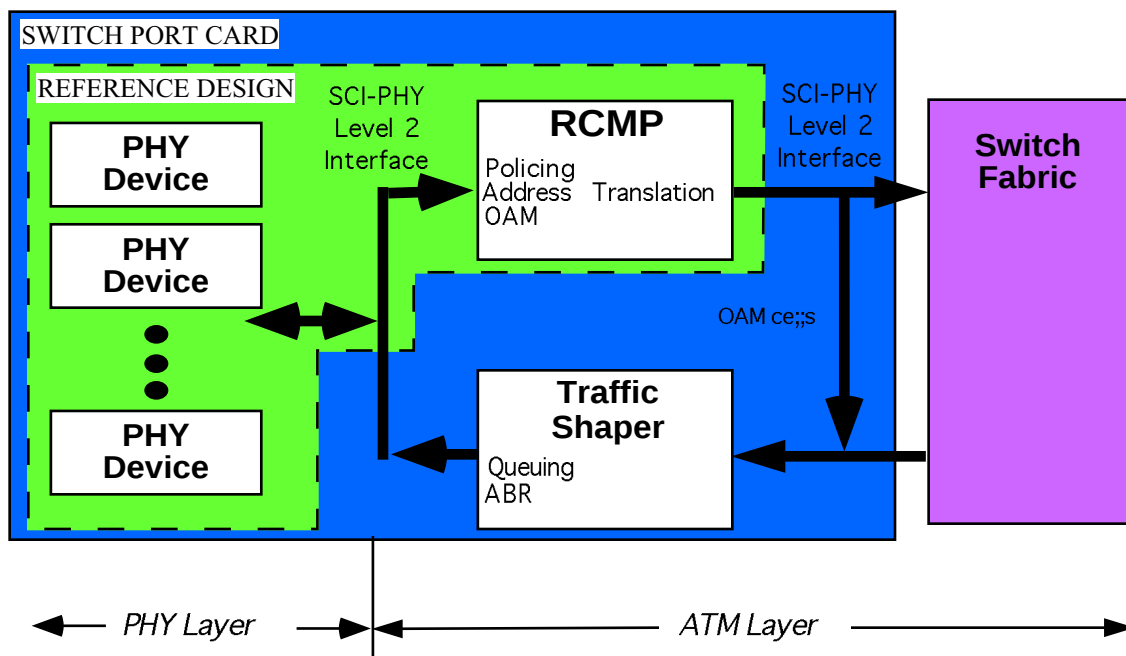
OVERVIEW

The RCMP performs ATM Layer functions: 1) Header translation and cell append for Routing, 2) Policing, 3) Cell counting and 4) OAM cell processing and routing, for up to 64K VC's. It provides UTOPIA interface at both the physical and the switch sides. The RCMP also provides cell insert/extract through the microprocessor interface.

The RCMP is ideally suited for both UNI and NNI ATM Interfaces, in the WAN and WAN access equipment: 1) Edge Switches, 2) Enterprise Switches, 3) Core Switches and 4) Access Muxes and Residential Broadband Switches. As shown in Fig. 1 below, the RCMP typically reside in the Ingress direction, providing the complete set of ATM Layer functions.

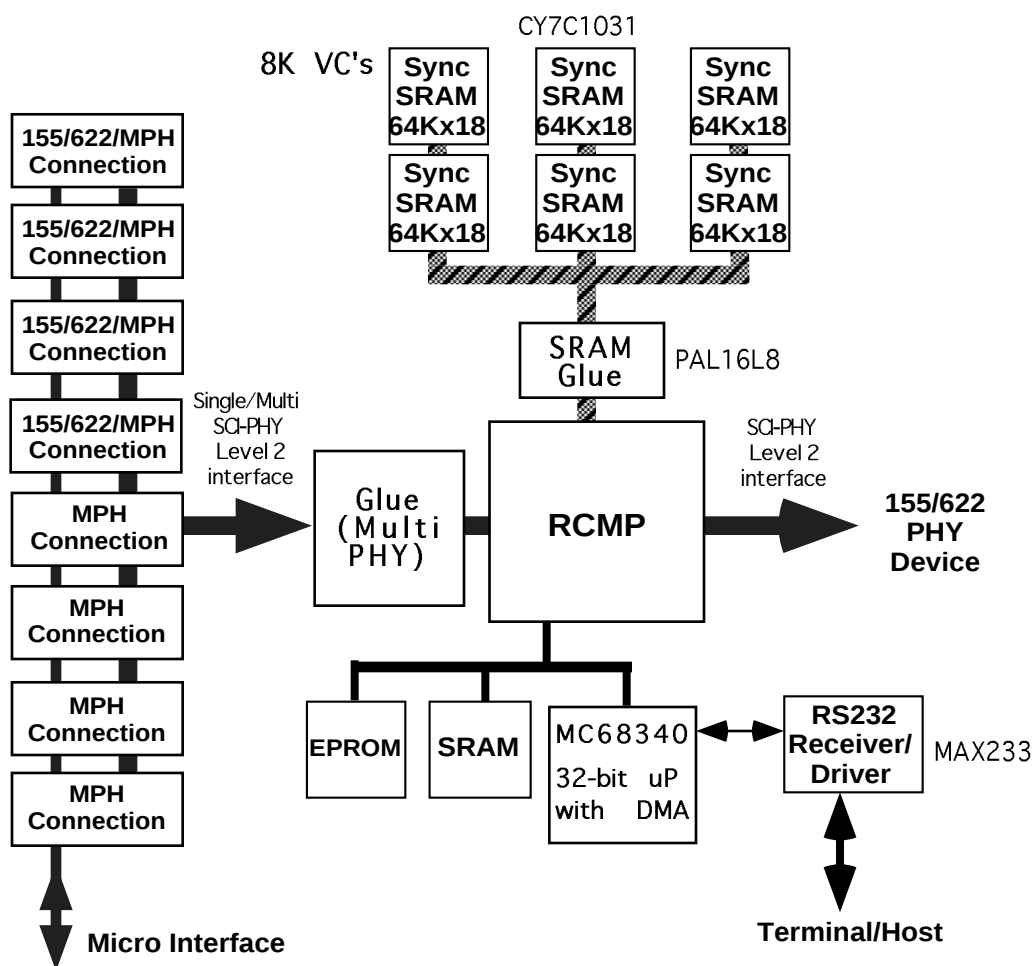
The primary purpose of this reference design is to demonstrate the Ingress application of the RCMP in a typical switch port environment. In particular, the multi-PHY interface to 8 PHY devices (eg. S/UNI-MPH's (PM7344)), and the direct interface to up to 4 PHY devices (eg. S/UNI-PLUS (PM5347), S/UNI-622 (PM5355)) are shown. The static RAM configuration and interface logic are included. Microprocessor control is performed using the Motorola 68340 32-bit CPU with DMA. Software drivers written in C are available from PMC (please refer to [12]).

Fig. 1 Typical Switch Port Architecture



FUNCTIONAL DESCRIPTION

Fig. 2 Reference Design Block Diagram



RCMP

The RCMP is the central processing unit for the cell traffic in this reference design. The following is a brief description of the RCMP functions.

The PM7322 Routing Control, Monitoring and Policing (RCMP) device is a monolithic integrated circuit that implements ATM layer functions that include fault and performance monitoring, header translation and cell rate policing. The RCMP is intended to be situated between a switch core and the physical layer devices in the ingress direction. The RCMP uses external SRAM to store per-VPI/VCI data structures. The device is capable of supporting up to 65536 connections.

There are two versions of this device that are available: the RCMP-800 (PM7322), which has 16-bit bus interfaces that have a throughput of 800 Mbps; and the RCMP-200 (PM7323), which has 8-bit bus interfaces that have a throughput of 200 Mbps, and is pin-compatible with the RCMP-800. This reference design applies to both devices, except for cases where the throughput is greater than 200 Mbps, which apply to the RCMP-800 only.

The Input Cell Interface can be connected to up to 32 physical layer devices through a SCI-PHY Level 2¹ compatible bus. The 53 byte ATM cell is encapsulated in a data structure which can contain pre-pended or post-pended routing information. Received cells are buffered in a four cell deep FIFO. All Physical Layer and unassigned cells are discarded. For the remaining cells, a subset of ATM header and appended bits are used as a search key to find the VC table entry for the virtual connection. If a connection is not provisioned and the search terminates unsuccessfully as a result, the cell is discarded and a count of invalid cells is incremented. If the search is successful, subsequent processing of the cell is dependent on contents of the cell and configuration fields in the VC table entry.

The RCMP performs header translation if so configured. The ATM header is replaced by contents of fields in the table entry for the connection. The VCI contents are passed through transparently for VPCs. Appended bytes can be replaced, added or removed.

If the RCMP is the end point for a F4 or F5 OAM stream, the OAM cells are dropped and processed. If the RCMP is not the end point, the OAM cells are passed to the Output Cell Interface with an optional copy passed to the Microprocessor Cell Buffer. The reception of an AIS or RDI cell results in the appropriate alarm. Upon the arrival of a Forward Monitoring or Monitoring/Reporting cell, error counts are updated and a Backward Reporting cell is optionally generated. Activate/Deactivate cells are passed to the Microprocessor Cell Buffer for external processing. Continuity Check cells can be generated if no user cells have been received in the latest 2 seconds.

¹See PMC-940102, "SATURN Compatible Interface for ATM PHY Layer and ATM Layer Devices, Level 2", Oct. 15, 1995, Issue 3. It provides functional extensions on UTOPIA2 interface by ATM Forum.

Cell rate policing is supported through two approximations of the Generic Cell Rate Algorithm (GCRA) for each connection. Each cell that violates the traffic contract can be tagged (CLP bit set high) or discarded. To allow full flexibility, each GCRA instance can be programmed to police any combination of user cells, OAM cells, Resource Management, high priority cells or low priority cells.

The RCMP supports multicasting. A single received cell can result in an arbitrary number of cells presented on the Output Cell Interface, each with its own unique VPI/VCI value and appended bytes. The ATM cell payload is duplicated without modification.

The Output Cell Interface can be connected to the switch core through a SCI-PHY Level 2 compatible bus. Cells are stored in a four cell deep FIFO until the downstream devices are ready to accept them. The details of how cells are handled in this FIFO depends on the particular application of the RCMP and are presented in "Operational Modes" section.

The Microprocessor Interface is provided for device configuration, control and monitoring by an external microprocessor. This interface provides access to the external SRAM to allow creation of the data structure, configuration of individual connections and monitoring of the connections. The Microprocessor Cell Buffer gives access to the cell stream, either directly or through intervention by a DMA controller. Programmed cell types can be routed to a microprocessor readable sixteen cell FIFO. The microprocessor can send cells over the Output Cell Interface.

The RCMP is implemented in low power, 0.6 micron, +5 Volt CMOS technology. It has TTL compatible inputs and outputs and is packaged in a 240 pin copper slugged plastic QFP package.

PHY Interface

The RCMP can interface with up to 32 PHY devices. The maximum aggregate bandwidth is 622Mb/s², or STS-12/STM-4 rate. Three most common modes of operations are demonstrated in this reference design. They all share common circuitry on board that can be programmed to one of the three modes. The interface to each PHY device is SCI-PHY compatible, although the RCMP can support SCI-PHY Level 2 interfacing, with the difference being the support for cell byte appends. The RCMP acts as the PHY master (ie. RDENB is controlled by the RCMP).

²This refers to the physical line rate that the RCMP can effectively support. The RCMP-800 supports a 800 Mbps bus at the input, but the effective data rate limitation comes in two forms: 1. The number of prepend and postpend words per cell and the number of dead cycles in between cell transfers; and 2. the cell processing speed internal to the RCMP, which is dependent on the number of address bits used for the binary search (for instance, a maximum of 18 bits can be used for the search to guarantee a 622 Mbps line rate). Either one of these two limitations can be dominant.

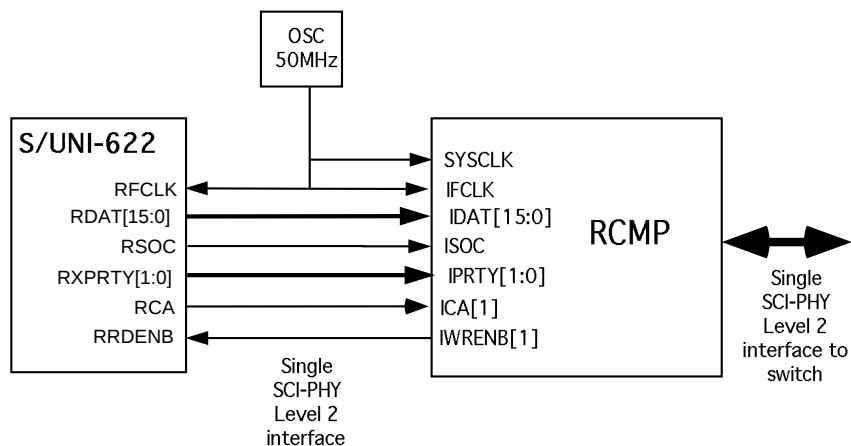
As shown in the block diagram on page 2, multi-purpose connectors are used for the PHY interfaces. The top four connectors interface to either a S/UNI-LITE (PM5346), a S/UNI-PLUS (PM5347), a S/UNI-622 (PM5355), a S/UNI-DUAL (PM5348), a S/UNI-PDH (PM7345), or a S/UNI-MPH (PM7344). The bottom four connectors interface to S/UNI-MPH's. Each PHY port card is controlled through a common microprocessor interface.

The following sections describe the single-PHY direct mode, quad-PHY direct mode, and multi-PHY address polling mode operations. Please refer to references [1], [2] for more detailed information.

Single-PHY Operation

In single-PHY operation, the RCMP interfaces with a PHY device at up to 622Mb/s. The device chosen in this reference design is the S/UNI-622, which is an SONET/SDH OC-12/STM-4 PHY interface. No external logic is necessary. The data bus operates in 16-bit mode at 50MHz. Note that, although ICA1 and IWRENB[1] is shown in Fig. 3, any one of the four ICA/IWRENB control lines can be used to interface with the S/UNI-622.

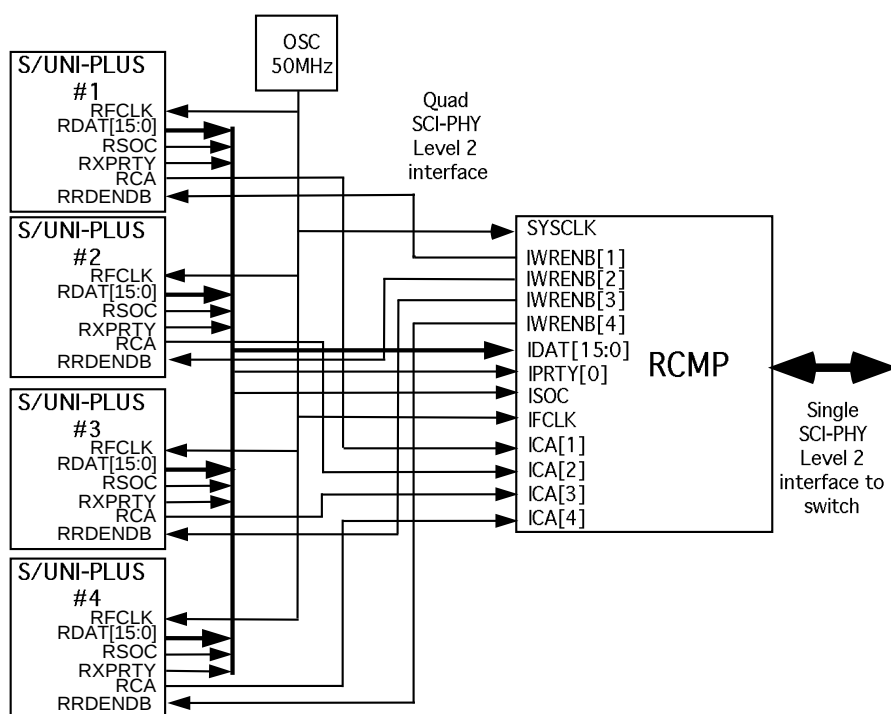
Fig. 3 Single-PHY System diagram



Quad-PHY Operation

In quad-PHY operation, the RCMP interfaces with up to four PHY devices, with a maximum aggregate bandwidth of 622Mb/s. An example would be interfacing with four 155Mb/s devices³. The device chosen in this reference design is the S/UNI-PLUS, which is an SONET/SDH OC-3/STM-1 PHY interface. No external logic is required. The RCMP handles the bus arbitration (RDAT, RSOC, RPRTY from the four S/UNI-PLUS's share the same bus), and handshakes with each PHY device directly using dedicated cell-available (RCA) and read-enable (RRDENB) signals. The data bus can operate in either 8-bit or 16-bit mode, depending on the bandwidth of the PHY device.

Fig. 4 Quad-PHY System diagram



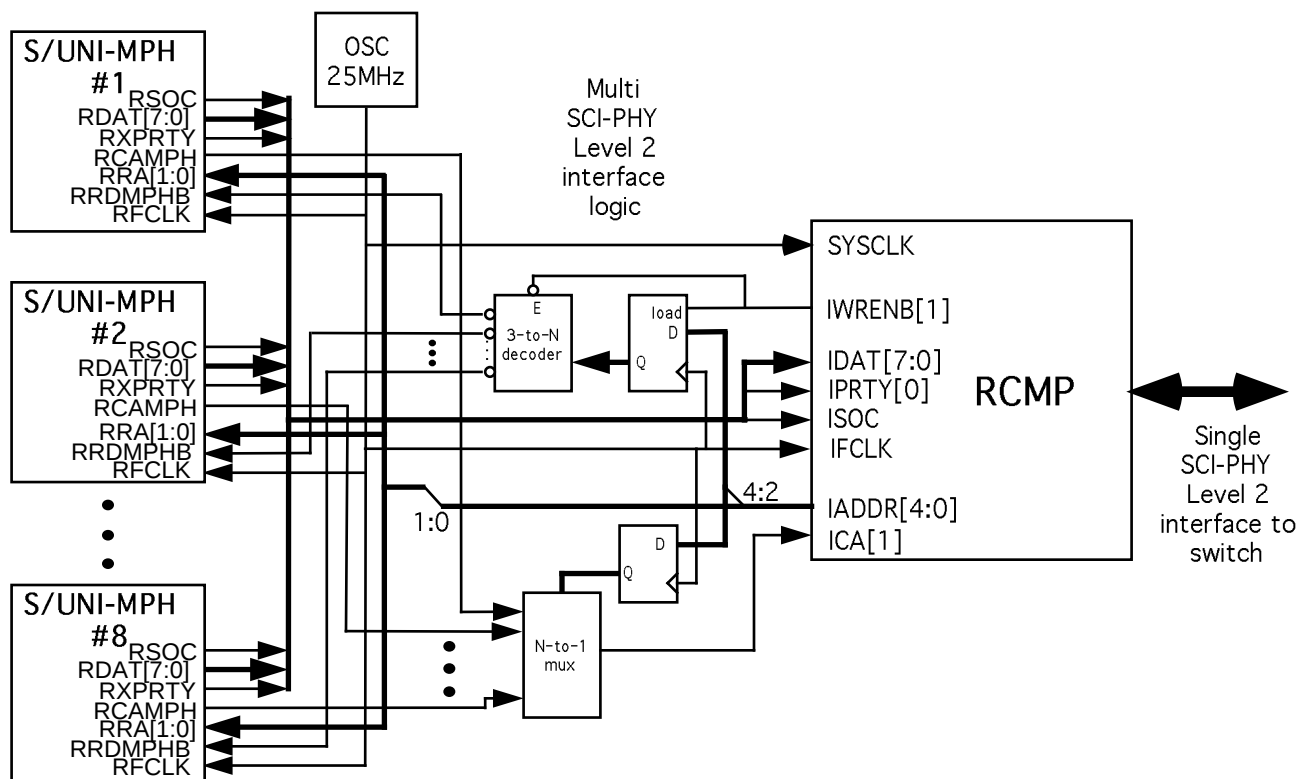
³Another example would be interfacing to 4 S/UNI-PDH's (PM7345), which function as an ATM interface for DS3, DS1, E1, E3 Pleisiochronous Digital Heirarchy applications. The maximum aggregate data rate will be 4 x 44.7 Mbs (DS3) = 178 Mbps.

Multi-PHY Operation

In multi-PHY operation, the RCMP interfaces with up to 32 PHY ports using address polling. In this reference design, a maximum of 8 PHY devices can be connected. Each device is a S/UNI-MPH, which contains 4 logical PHY ports, each being a DS-1/E1 connection. The maximum aggregate bandwidth is therefore 32 x 2.048Mbps, or 65.5Mbps.

External logic is required to perform the multi-PHY bus arbitration. The system diagram below shows the interface signals and logic. The 8-bit data, parity and start-of-cell signals from different PHY devices share a common bus. Address decoding is required to generate the individual read-enable signals, which controls which PHY device can drive the bus. RCA's are selected by the address decoding circuit to be read by the RCMP.

Fig. 5 Multi-PHY System diagram



PHY Interface Clock Frequency

The clock frequency with which the PHY interface operates in are 50MHz and 25MHz as mentioned in the above. However, these are only nominal frequencies. The minimum operating frequencies for the 3 different modes are as follows:

Mode	Aggregate Bandwidth	Bus Width	Minimum Frequency
Multi-PHY	65.5Mbps	8 bits	8.65MHz
Quad-PHY	622Mbps	16 bits	41.1MHz
Single-PHY	622Mbps	16 bits	41.1MHz

The minimum clock frequency is found by dividing the aggregate bandwidth by the bus width, and including the minimum of 3 dead clock cycles between cell transfers into the RCMP. Note that the maximum clock frequency that the RCMP can operate in is 52MHz. In any particular modes, if the frequency is to be increased, one has to consider the delays of the PHY devices and any glue logic in between.

Multi/Single PHY Interface Connectors

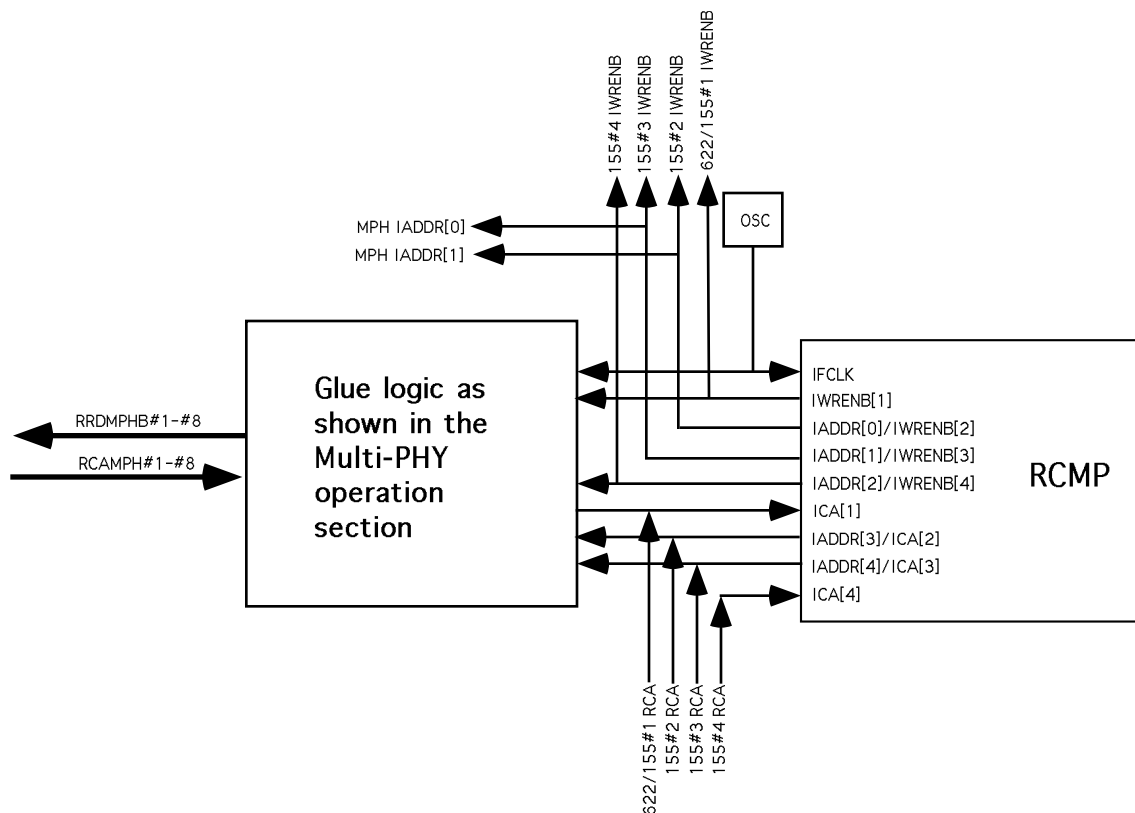
Two types of PHY connections are used for the input interface. For the connection that interfaces to the S/UNI-MPH only, an 8-bit SCI-PHY bus interface in a 120-pin connector is used. For the ones that interface to the S/UNI-LITE, the S/UNI-622, the S/UNI-PLUS, the S/UNI-DUAL, or S/UNI-MPH, a 16-bit SCI-PHY 140-pin is used. (Refer to the Layout description diagram)

For the output interface, which can be connected to the S/UNI-LITE, S/UNI-622 or the S/UNI-PLUS, a 16-bit SCI-PHY 120-pin is used (the 20 pins for S/UNI-MPH interface are not needed).

Multi/Single PHY Interface Logic

Fig. 6 shows the PHY interface that supports the 3 operational modes: Multi-PHY, Quad-PHY and Single-PHY. In particular, the multi-PHY interface requires address decoding, RCA muxing logic.

This multi-PHY logic is implemented with two PAL's (eg. 22V10's).

Fig. 6 PHY Interface Logic Diagram

SRAM Requirements for VC Tables

Synchronous SRAM's are used to provide storage of the VC tables. Each VC requires one table to store information on header translation, policing, and cell counts. Each table has a maximum size of 16x40 bits. This can be reduced if certain functions are not required (eg. particular cell counts might be unnecessary for some applications).

The SRAM data bus is 40-bit wide, plus 5 bits of parity, one for each data byte, making a total of 45 bits. The address bus is 20-bit wide (1M address space), to support a total of 64K VC's.

64K x18 synchronous (non-pipelined) SRAM's⁴ were used to construct a basic memory block for 8K VC's, as follows: 1K VC's require 1Kx16x45 bits, or 16Kx45bits. Therefore, 8K VC's require 128Kx45 bits of memory. The 45-bit word can be partitioned into 3 sections. The first section is 128Kx18 bits, so using two 64Kx18 SRAM's is sufficient. The second section is also 128Kx18 bits, using two 64Kx18 SRAM's. The third section

⁴At the time of writing, these SRAM's were the largest size that were readily available. It is expected to see larger sizes to appear in the market, such as 128Kx18.

is 128Kx9 bits, and two 64Kx18 SRAM's are used. Only half of each SRAM is used in this section.

It is possible to use one fewer SRAM for the third section, but only in applications where the clock is below 40MHz. This is explained in detail in Appendix 1. Furthermore, low cost, asynchronous SRAM's can be used for applications using the RCMP-200 which runs at 25MHz. Please refer to reference [14] for further information.

Bellcore's (GR1110-CORE, Issue 1) requirement on the number of VC's to be supported on the UNI interface rates most typical for the RCMP is as follows:

UNI rate	Min. # VC's	# VC's for RCMP
DS1	256	8K (32 PHY's)
STS-3c	4K	16K (4 PHY's)
STS-12c	8K	8K (1 PHY)

The worst case is therefore 16K VC's in the quad-PHY operation. This reference design supports only 8K VC's. The reason is that the memory space for 8K VC's is conveniently provided by the basic block of 6 64Kx18 SRAM's, and this is sufficient to demonstrate the necessary glue logic and timing considerations.

Note that cache modules containing 4 64Kx18 SRAM can be used to save board space. For designs required to support more than 8K VC's, it is advantageous to use these cache modules. For example, 6 of these modules provide enough memory for 32K VC's (recall that 6 64Kx18 SRAM's are needed for 8K VC's).

SRAM Interface Logic

This interface is very time-critical, since it runs at a maximum rate of 50MHz (20ns period). The timing diagram (Fig. 7) and the interface diagram (Fig. 8) is shown in the next 2 pages.

Address decoding is required to generate 16 chip selects to the SRAM's. Each chip select correspond to a bank of memory for 4K VC's. The prop delay for this function has to be less than 5.5ns, considering the address line prop delay of 12ns in the RCMP and the 2.5ns setup time (on CSB) required by the SRAM. Thus, a very fast PAL (PAL16L8-4, <4.5ns delay) is used. For SADSb, SOEB and SRWB, fast (FCT) buffers with delays less than 5.5ns are needed to meet the setup time of 2.5ns at the SRAM.

The SRAM data input has a C_{in} of 5pF and a setup time of 2.5ns. Therefore, the RCMP data lines (with a maximum propagation delay of 15ns with a load of 50pF) can be connected directly to the 2 banks of SRAM's and still meet the setup requirement. The maximum configuration at 50MHz operation, using 64K x 18 SRAM's, is determined as follows: With the output capacitance of the RCMP being 5pF and assuming the capacitance of the signal traces to be at most 15pF, the RCMP can drive a maximum of

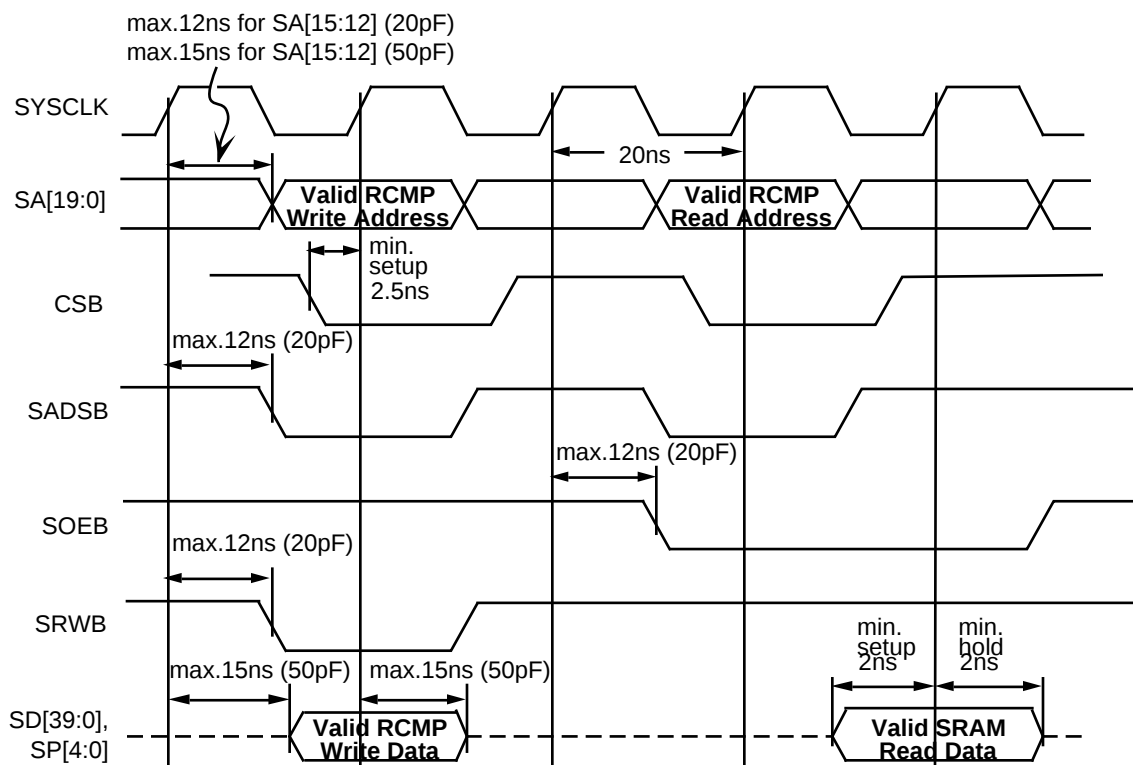
6 banks of SRAM, or a total of 24K VC's. This is a very conservative estimate, since there is 2.5ns of margin left. Therefore, it is very likely that the RCMP can drive an extra 10pF, for a total of 8 banks of SRAM, or 32KVC's.

For larger SRAM configurations, data transceivers will be needed to buffer the load. Unfortunately, it is not possible to use data transceivers in 50MHz operation due to timing constraints⁵. Therefore, the next generation SRAM technology (128K word) is needed for the RCMP to support a larger number of VC's in 50MHz operation. However, data transceivers can be used for lower speed applications such as at 25MHz.

It is very important to have low clock skew in this 50MHz operation. A clock driver (74FCT807) is therefore used, which guarantees less than 0.5ns skew with a maximum of 50pF load.

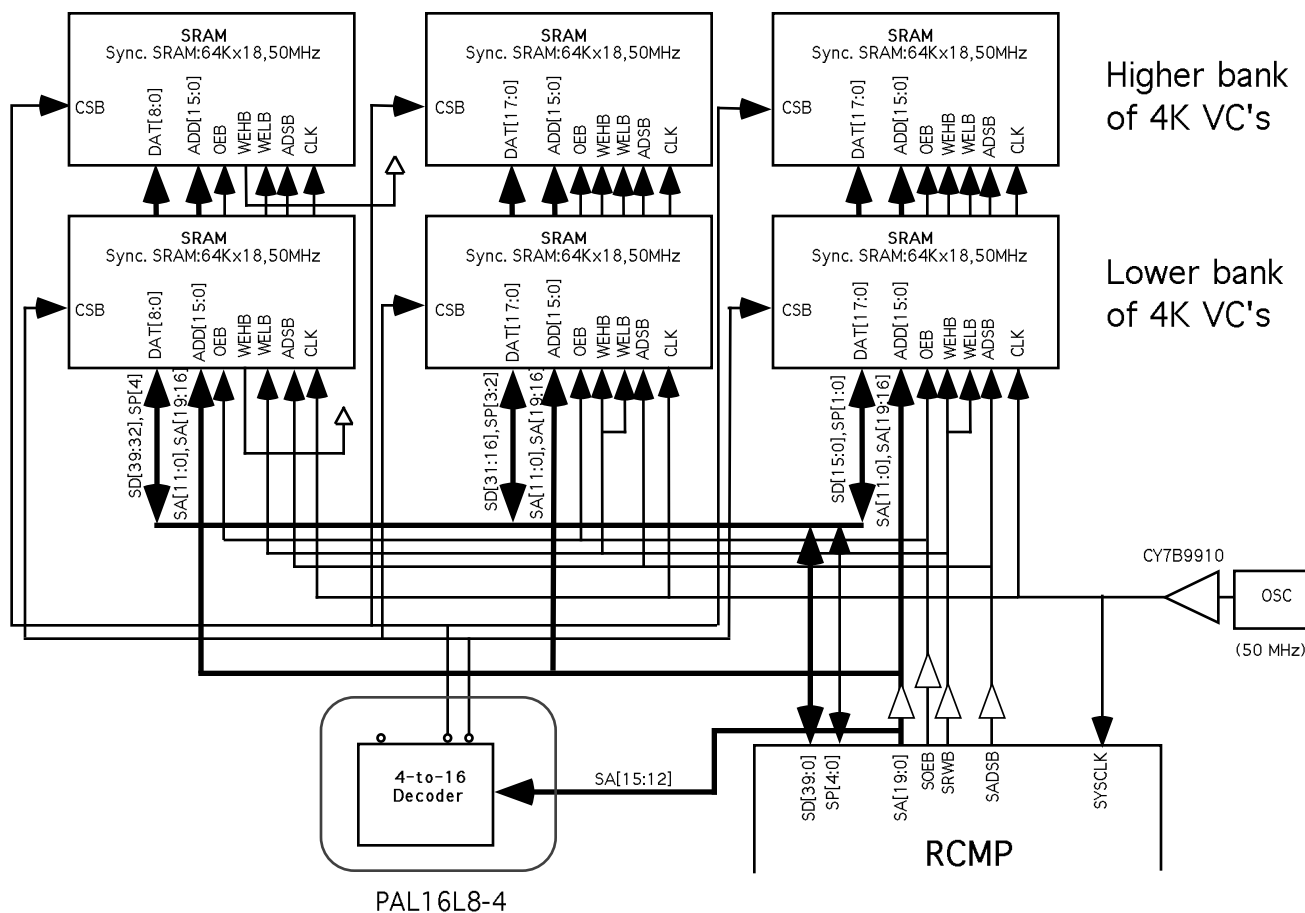
For the use of 3V SRAM's, please refer to reference [11].

Fig. 7 SRAM Interface Timing Diagram



⁵The read-write control signal (SRWB) from the RCMP is needed to control the output enable of the transceiver in a WRITE operation. Using the fastest glue logic components available, the sum of the delays ($t_{PD}(\text{RCMP})$ of 12ns with 20pF load + $t_{PD}(\text{buffer})$ of 4ns + $t_{PD}(\text{transceiver})$ of 5ns + $t_{SETUP}(\text{SRAM})$ of 2.5ns = 23.5ns) is greater than the 20ns period.

Fig. 8 SRAM Interface Block Diagram

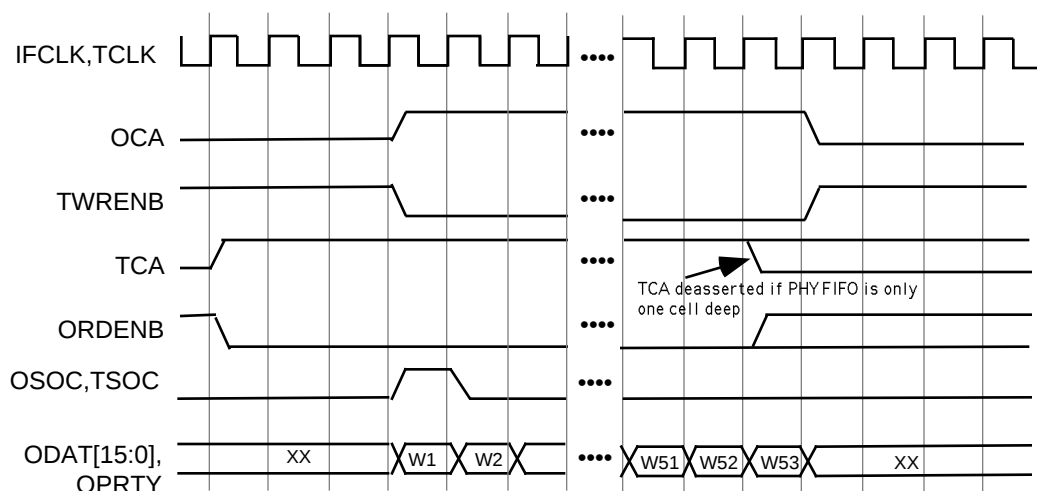


Switch Interface

The output of the RCMP is a SCI-PHY Level 2 compatible single-PHY interface. Typically, it is connected, either directly or through an intermediate processing (for routing of OAM cells) device, to the switch core via a backplane. The RCMP acts as a slave device (ie. ORDENB is an input). The data bus can be either 8 bits or 16 bits.

In this reference design, a PHY device (eg. S/UNI-PLUS or S/UNI-622) is connected to this interface, which sends the ATM traffic out onto a physical link. This simulates the case where the effect of the switch core is transparent, allowing the users to form a closed-loop system from physical link to physical link, so as to focus on the functions of the RCMP.

Note that if the RCMP slave output is connected to a PHY transmit input that is also a slave, it results in a *slave-slave SCI-PHY interface*, whose timing is illustrated in Fig. 9.

Fig. 9 Slave-slave Interface Timing Diagram

The ORDENB signal at the RCMP is generated from the inverted TCA signal from the PHY device. The TWRENB signal at the PHY device is generated from the inverted OCA signal from the RCMP. This scheme works as follows: TCA is asserted when the PHY device has space for at least one cell. This causes ORDENB to be asserted which signals the RCMP to output a cell. However, the RCMP only outputs a cell if the cell is available, in which case OCA is asserted. At the same time, TWRENB is also asserted, and the first word of the cell is sent out. At the end of the cell transfer, OCA is deasserted, causing TWRENB to be deasserted also. *It is important to ensure that OCA is only deasserted at the end of the cell transfer, not 4 words before the end.* There is a programmable option for OCA deassertion in the RCMP (Register 38, Bit 1). This bit is set to 1 by default, indicating OCA deassertion at the end of cell transfer.

Note that in the scenario just described, we have assumed that there is always space available on the PHY device, and the actual transfer is determined by the cell availability at the RCMP. The other scenario is when the space availability on the PHY device is the determining factor. In this scenario, OCA is asserted with a cell waiting to be sent out by the RCMP, and TWRENB is also asserted. No cell transfer takes place until the PHY device has cell space, and TCA gets asserted, which causes ORDENB to be asserted. With TWRENB asserted but no space in the PHY device to receive a cell, the PHY device will likely indicate an input FIFO over-run condition. Note that the PHY device should not allow data to be written in when TCA is deasserted. *It is important to ensure that TCA is only deasserted at the end of the cell transfer, not 4 words before the end.* There is a programmable option for TCA deassertion in all S/UNI PHY devices.

In general, this scenario will not occur if the PHY device has enough bandwidth for the cell traffic from the RCMP. The first scenario in the previous paragraph is a more likely case, since the RCMP can be dropping cells due to policing, thus reducing the rate of cells being sent out. In this case, TCA will always be asserted, indicating that the PHY device always has space.

Note that the RCMP can be programmed to output an inverted OCA, thus avoiding the use of the inverter. Refer to Register 38, Bit 14, which is set to 0 by default, indicating no inversion on OCA.

For a detailed description of this slave-slave interface, please refer to reference [13].

Micro Interface

The Motorola 68340 is used to control the RCMP. It provides the following features:

- 16-bit data bus
- DMA controller that interfaces directly to the RCMP
- Interrupt controller
- Address decoder
- Timer
- Serial interface

The 68340 is commonly used in many embedded applications, and its main advantage is that it requires a very small number of external components to be operational. These components include: clock circuitry, RAM, ROM, and a serial interface (RS232). It also has an abundance of third-party software support, such as real-time operating systems and C-compilers. In addition, the 68340 has a built-in background debug function, which greatly simplifies the code debugging operation.

A set of software drivers are provided for the RCMP working with the 68340. Please refer to reference [12].

SCHEMATICS DESCRIPTION

The following is a detailed description on the key functional components in the schematics. The actual schematics are included in Appendix B.

Sheet 1: RCMP and PHY Interface Logic

This sheet shows the RCMP interfaces and the associated glue logic.

- Input PHY interface: Decode logic for multi-PHY application is implemented by two 22V10 PAL's (U19 and U25) (Refer to the system diagram on page 7). U19 has to have a delay of less than 11ns to generate the ICA1 signal that will satisfy the setup time of 4ns at the RCMP, since the S/UNI-MPH has a prop delay of 25ns. U25 needs to have a delay of less than 15ns.
- The clock (IFCLK) is distributed using a 74FCT807 clock driver (U7) to the RCMP, the input PHY (a maximum of 8) devices, and to one of the 22V10's. IFCLK can be either 50MHz or 25MHz, depending on the PHY interface. These interface signals go to the connectors on Sheets 2-5.
- Clock termination is used at the destination pins for all clocks and is implemented by 130 ohm to VCC and 91 ohm to ground. Note that source resistors are added for each clock output from the clock driver. They are all zero ohms currently, but any resistance values can be substituted, in case there is a need to correct overshoot problems.
- Jumper (JP1) is used to enable ICA to be sourced from the multi-PHY glue logic (U19), instead of ICA1 from Input PHY connector #1. In multi-PHY mode, the direct ICA signals from the PHY connectors are not used; ICA comes from the mux (implemented by U19) that selects one out of a maximum of 8 input PHY devices.
- SYSCLK for the RCMP is sourced from Sheet 2, since it is also used by the synchronous SRAM's.
- Output PHY interface: These interface signals go to the connector on Sheet 6. Clock (OFCLK) is sourced from Sheet 2. OFCLK can be either 50MHz or 25MHz, depending on the PHY interface.
- The interrupt signal, INTB, from the RCMP to the 68340 microprocessor need to be pulled-up to VCC (through a 10K resistor) since it is an open-drain output.
- The address latch signal, ALE, into the RCMP is pulled-up to VCC (through a 10K resistor) since non-multiplexed address and data buses are used with the MC68340.
- Jumpers are used to configure the RCMP for different interfaces: IPOLL (J1) which enables multi-PHY; IBUS8 (J3) which selects 8-bit SCI-PHY bus vs 16-bit for the RCMP input; OBUS8 (J2) which selects 8-bit SCI-PHY bus vs 16-bit for the RCMP output.
- Test points (TP1, TP2) are for signal insertion to test CONG, and ONESEC.
- The signals with the "M_" prefix (and the signal RCMP_CSB) are for interfacing to the 68340 micro on Sheet 9.

- Decoupling cap's are on Sheet 10. 0.01uF caps are used for each power (VDD or VCC) pin on the IC's.

Sheet 2: VC Table SRAM

This sheet contains the synchronous SRAM used by the RCMP for the VC Table, and associated glue logic.

- The synchronous SRAM's (U5, U24, U12 for 4K VC's; U23, U22, U21 for the other 4K VC's) implement the VC Table to handle 8K VC's. Associated glue logic (U20, PAL16L8) is used for address decoding, and U2, U3, U6 are fast buffers (74FCT541) used for the address buffering. U20 has to have a delay of less than 5.5ns.
- For the SRAM's used in this design, 3 64Kx18 SRAM's are used for 4K VC's, but only 2.5 SRAM's are actually used. Half of the "most significant" SRAM's, U12 and U21 are unused. (write-enable low (WLB) of U12, U21 are tied high (inactive)) Unused burst control signals, ADSPB and ADVB are tied high (inactive) on each SRAM.
- A clock driver for SYSCLK(U28, 74FCT807) is used to reduce skew between the synchronous SRAM's and the RCMP, so as to improve the timing margins in this interface which can run at 50MHz. Clock terminations are used and are implemented by 130 ohm to VCC and 91 ohm to ground. Note source resistors are added for each clock output from the clock driver. They are all zero ohms currently, but any value can be substituted, in case there is a need to correct overshoot problems.
- OFCLK is buffered by an fast buffer (U6, 74FCT541). This is sufficient since the clock is only connected to 2 devices, which are the RCMP and the output PHY device.
- Jumper (JP4) is included for shorting IFCLK to OFCLK, for cases where only one oscillator is used for both PHY interfaces.
- Decoupling cap's are on Sheet 10. 0.01uF caps are used for each power (VDD or VCC) pin on the IC's.

Sheet 3-6: Input PHY Interface Connectors

These four sheets show the input PHY connectors that can interface with the S/UNI-LITE (on the SORD board reference design⁶), the S/UNI-622 (on the 622 multi-mode reference design board⁷), the S/UNI-PLUS (on a future S/UNI-PLUS reference design board), the S/UNI-DUAL (on a future S/UNI-DUAL reference design board) or the S/UNI-MPH (on a future MPH reference design board).

⁶Please refer to the reference design documentation, PMC-950112, Issue 3.

⁷Please refer to the reference design documentation, PMC-950860, Issue 2.

- The 100-pin connector (P11 to P81) is used for the 8-bit SCI-PHY interface and the microprocessor bus. The upper 20-pin connector (P10 to P40) is used for the bus extension to handle 16-bit interfaces. The lower 20-pin connector (P12 to P82) is used for MPH multi-PHY control signals.
- Note that only the Ingress direction (Receive) signals are connected.
- Pull-down resistors (10K ohm) are provided for RCAMP1-8 and ICA1-4, so as to indicate to the RCMP that there are no cells available from the PHY connections that are not present.
- Common microprocessor control bus used. Microprocessor (Motorola 6811) on the EVBD⁸ is used to control the input PHY devices (see connector to Micro EVBD on Sheet 8)
- Connector #1- 4 connect to the S/UNI-LITE, the S/UNI-622, the S/UNI-PLUS, the S/UNI-DUAL, the S/UNI-PDH, or the S/UNI-MPH.
- Connector #5-8 connect only to the S/UNI-MPH.
- This board provides power (+5V) to the input PHY reference design boards.

Sheet 7: Output PHY Interface Connector

This sheet shows the output PHY connectors that can interface with the S/UNI-LITE, the S/UNI-622, and the S/UNI-PLUS.

- The main 100-pin connector (P11 to P81) is for the 8-bit interface and the micro control bus. The lower 20-pin connector (P12 to P82) is for MPH multi-PHY control signals.
- Only the Transmit PHY signals are connected.
- The inverting buffer (U14) is to provide the slave-slave interface control signals.
- Common micro control bus used. Micro (MC6811) EVBD is used to control the output PHY (see connector to Micro EVBD on Sheet 8)
- This board provides power (+5V) to the output PHY reference design board.

Sheet 8: Micro EVBD Connector and Decode Logic for PHY Devices

This sheet contains the connector to the Micro EVBD and the associated glue logic for address decoding to control the input and output PHY devices. The EVBD also resets the PHY devices.

- The chip_selects for the Input PHY devices and the Output PHY device are generated.
- Note the address latch enable, ALE, is pulled-up. It is not needed by the PHY devices since addresses are already latched on this sheet.
- Reset from EVBD to all PHY devices
- Address space allocation for PHY devices is shown in the following table:

⁸The EVBD is an internal PMC test evaluation board that contains the Motorola 6811 processor.

	A15	A14	A13	A12	A[11:8]	A[7:0]	
Input PHY	0	1	y	y	yxxx	XX	ie. (4+yy)(yxxx)XX
Output PHY	0	0	1	1	F	XX	ie. 3FXX

where the 3 bits of y indicates which PHY, x is 1 bit of don't care, and X is 4 bits of don't care.

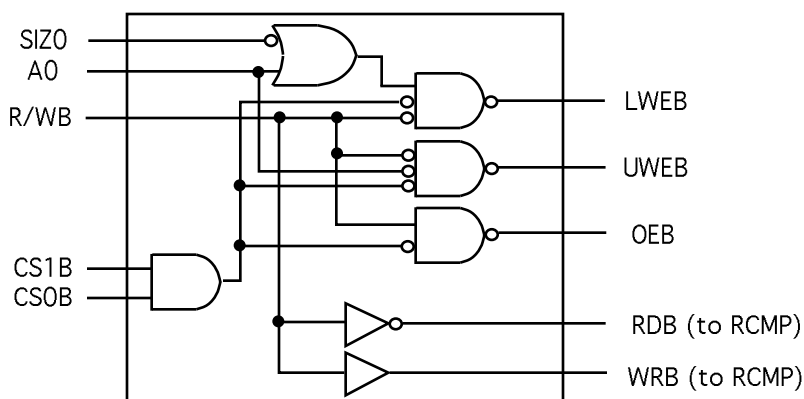
Note that INPUT_PHY_SELB, OUTPUT_PHY_SELB and BOARD_SELB are used to ensure that the MC6811 does not access these devices when not intended (ie. upper address range are fully decoded).

Sheet 9: MC68340 Microprocessor and Associated Circuits

This sheet contains the 25MHz MC68340 microprocessor, the SRAM, the EPROM and the serial interface, together with the support circuitry, such as the reset circuit.

- 7-bit address (A07 to A01) from the MC68340 are connected to A[6:0] of the RCMP, since the MC68340 increments the address by 2 for 16-bit accesses, whereas the RCMP increments by 1.
- A pair of 128Kx8 SRAM's is used, which is deemed sufficient for the amount of code needed to exercise the RCMP. Both 8-bit and 16-bit accesses are supported by the glue logic (implemented in the PAL22V10, U27). This glue logic is illustrated in Fig. 10 (please refer to reference [16]⁹). The PAL has to have less than 10ns delay to generate WEB signals that would satisfy the Write data hold time at the SRAM, which specifies 10ns of data valid time after the WEB signals are de-asserted. RAM chip-selects are hard-wired to be active to reduce access time (although power dissipation is higher). Access is gated by WEB or OEB only.

Fig. 10 Micro-SRAM Glue Logic



⁹Please refer to the Item #63 in the Addendum to Rev. 1 of the MC68340 User's Manual

Note that CS1B and CS0B are AND'ed together (ie. either CS0B or CS1B asserted) since the MC68340 always asserts CS0B during code download into SRAM using the background debug monitor, while it asserts CS1B during normal SRAM accesses. This applies to the case where only the SRAM is being used (typically during code development). If the EPROM is used (which is selected by CS0B), then this AND gate should be removed, and only CS1B should be used here.

- A 32Kx8 EPROM is used. Pins 1, 2 of jumper J4 should be connected if the EPROM is used. One has the option to replace it with a 32Kx8 Non-volatile SRAM (with jumper JP2 connected, and pin 2, 3 of jumper J4 connected).
- 74HC393, U34, (4-bit binary counter, falling-edge triggered) is used to generate DSACK0B for EPROM during boot-up (to indicate 8-bit device with 2 wait states). This is optionally enabled by jumper JP3.
- Jumpers for DSACK0B and DSACK1B (J5 and J6) for future RAM variations. In any case, both DSACK's can be programmed to be generated internally in the MC68340.
- MAX203 (U35) (+5V supply only, and no external capacitors needed) is used for the RS232 interface. A 3.6864MHz oscillator is used for the RS232 interface.
- The reset circuit, controlled by switch, SW1, resets the MC68340 and RCMP.
- Background Debug Monitor (BDM) connector, J10, is used for software development. Note that pin BKPTB must be pulled-up to VCC (through 10K). It is recommended that pin BERRB be pulled up also in a similar fashion. CLKOUT from the MC68340 needs to be connected to a test point to be used by the BDM connector. XFC pin of the MC68340 needs to be decoupled with 0.1uF to ground.
- Other details on the MC68340:
 - XTAL must be left open if external oscillator used for SYSCLK, which is the case in this reference design
 - VCCSYN needs to be pulled up to VCC
 - All unused inputs are pulled up through 10K
- Decoupling caps (0.01uF) are used for each power pin.

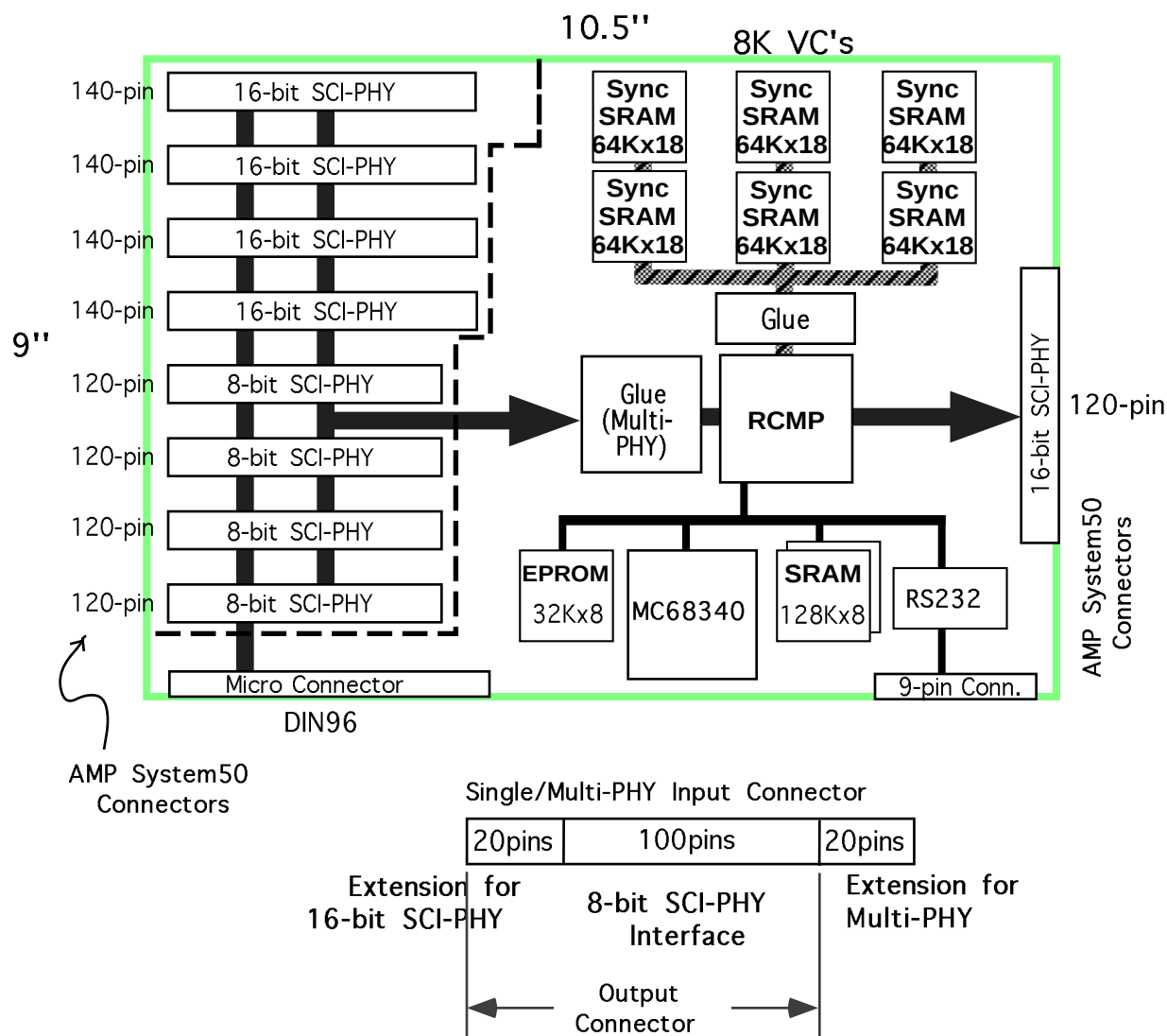
Sheet 10: Power Supply and Decoupling Capacitors

This sheet contains the 5V power supply block for the reference design board. It also includes the decoupling capacitors (0.01uF) for the RCMP and the SRAM's on Sheet 1 and 2.

- Power supply block (J9) supplies the +5V (VCC), +5 (VDD_D) and GND. The two +5 power supply sources are: VDD_D for Input PHY device boards and the 6811 EVBD, and VCC for the rest.
- 68uF power supply decoupling capacitors are distributed all over the board.
- Ground testpoints are included for probing use.
- HP logic analyzer adapter (J8) is included in schematic for future use.

LAYOUT DESCRIPTION

Fig. 11 Reference Design Board Layout

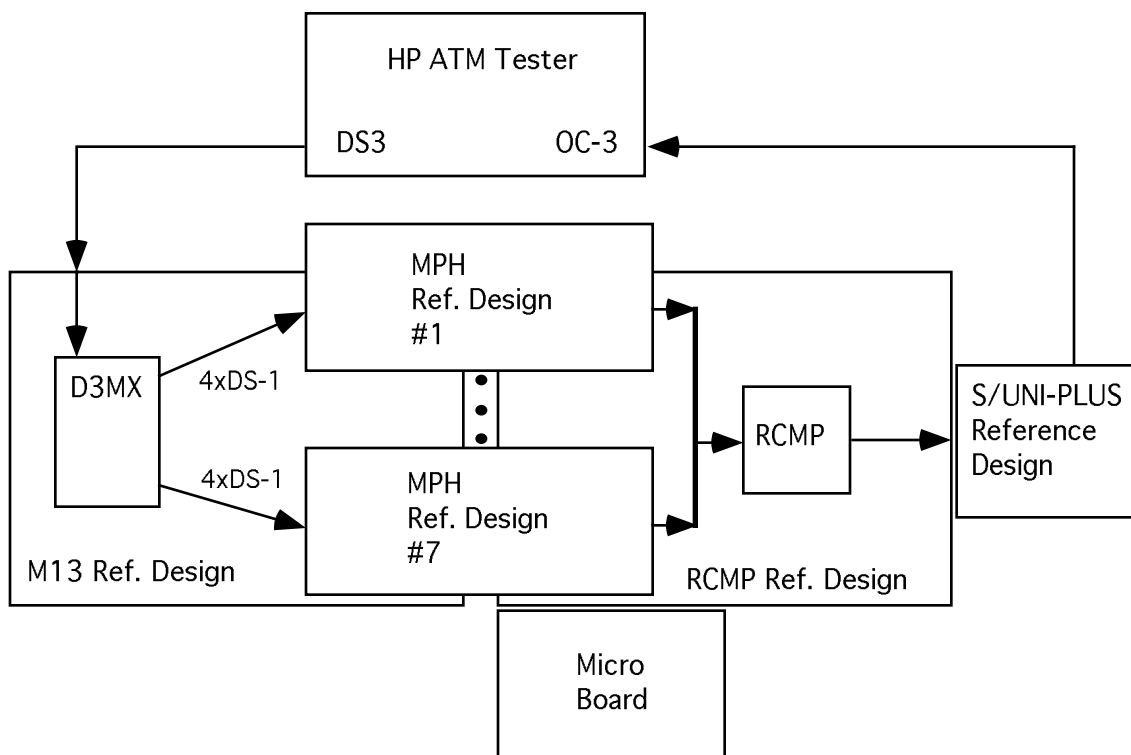


The layout is mainly constrained by the number and size of the connectors, which together take up more than one third of the board space. The PHY boards will be standing vertically. Some space is required between the PHY connectors and the rest of the circuitry to accommodate for some PHY boards that extend to the right side of the connectors. The power plane is divided into two sections (VCC and VDD_D) as indicated by the dashed line, such that the input PHY devices will have their own power

supply. The VC Table SRAM's, the RCMP, and associated glue logic and clock driver are placed as close to each other as possible to minimize wire loading and clock skew.

One application of this reference design is to interface with the M13 reference design¹⁰ board set up to the left side of the RCMP board, with MPH boards standing vertically as "bridges" between. The following diagram shows a typical multi-PHY systems configuration.

Fig. 12 Multi-PHY System Configuration

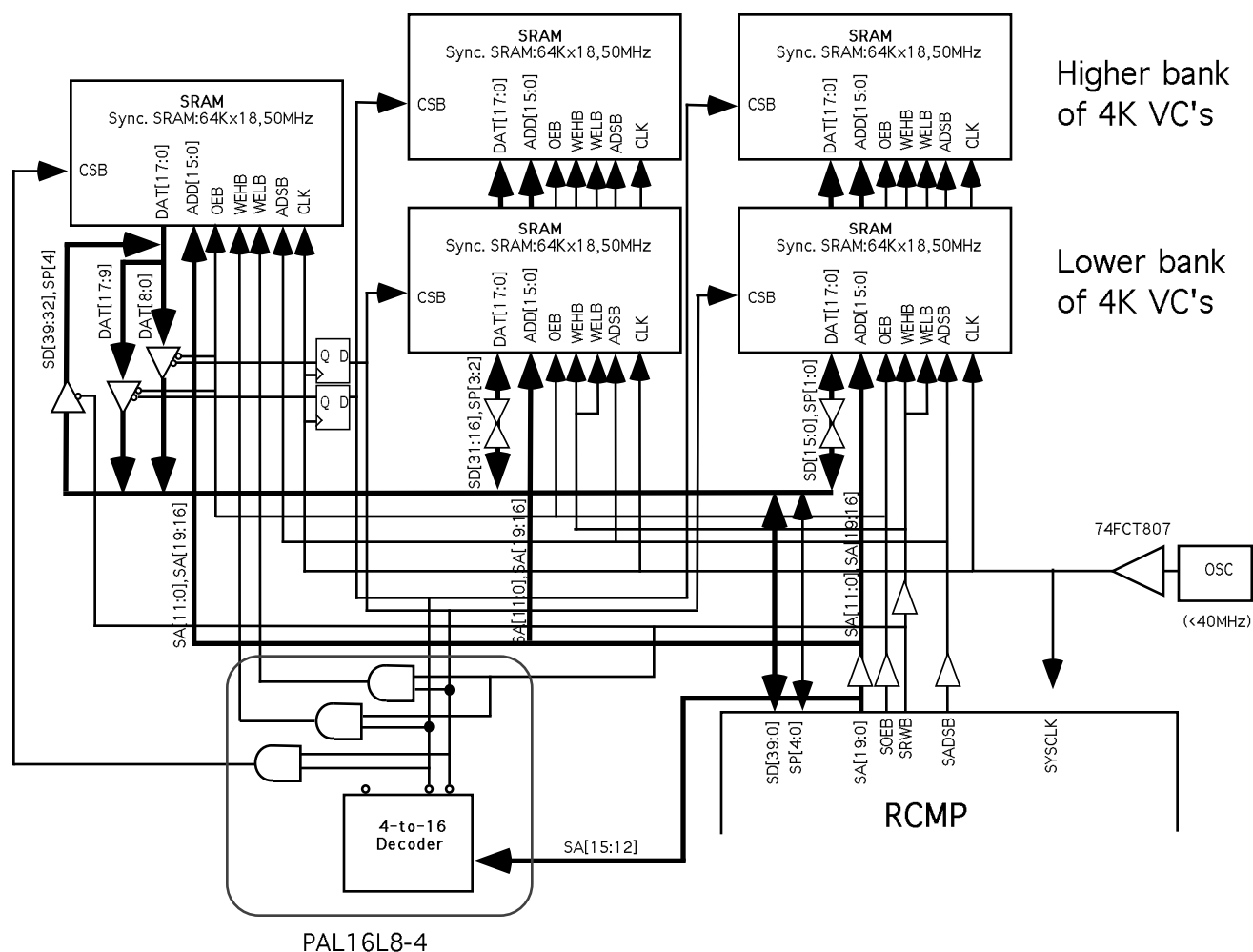


¹⁰In this reference design, a DS-3 signal is demultiplexed down to 28 DS-1's, from which ATM cells are then extracted using the S/UNI-MPH. Using this setup, we can show how T1 trunks can be interfaced to the ATM switch. See document PMC-951045, "D3MX Module of the PM4944 M13 Reference Design", for a detailed description.

APPENDIX 1: SRAM CONFIGURATION FOR LOWER SPEED APPLICATIONS

In this reference design, 6 SRAM's are used to provide storage for 8K VC's. For applications where the SYSCLK to the RCMP is lower than 40MHz (eg. 25MHz operation for 155Mbps throughput for STS-3, using the RCMP-200), one SRAM can be saved. The following diagram illustrates the SRAM configuration and supporting logic.

Fig. 13 SRAM Configuration for 25 MHz Operation

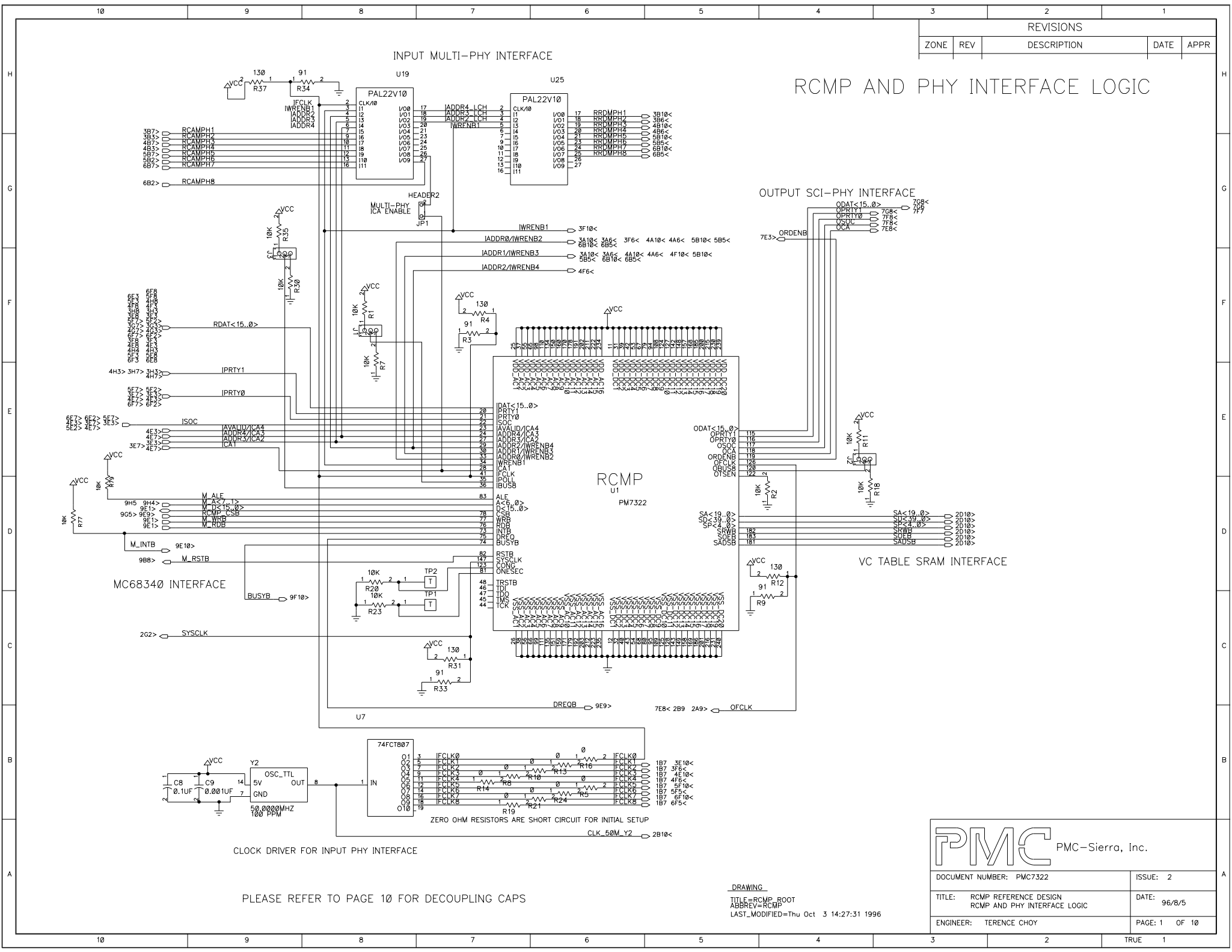


The 45-bit (data+parity) word can be partitioned into 3 sections. The first section is 128Kx18 bits, so using two 64Kx18 SRAM's is sufficient. The second section is also

128Kx18 bits, using two 64Kx18 SRAM's. The third section is 128Kx9 bits, using one 64Kx18 SRAM; this SRAM is divided into two banks of 64Kx9 bits logically.

Consider the SRAM providing storage for SD[39:32] and SP[4]. The SRAM is logically divided into two banks, each corresponding to one chip select. The 18-bit word is therefore partitioned into two 9-bit words, and one of them is selected by external logic to be read by the RCMP. The selection is done using the chip selects for the upper and lower banks, *and* the output enable signal. A flip-flop is required for the chip selects since the data comes out of the RAM one clock cycle later than when the chip selects are asserted. This selection logic can be implemented with a transceiver, but an AND gate would be required for the select control signals.

APPENDIX B: SCHEMATICS AND LAYOUT



REVISIONS				
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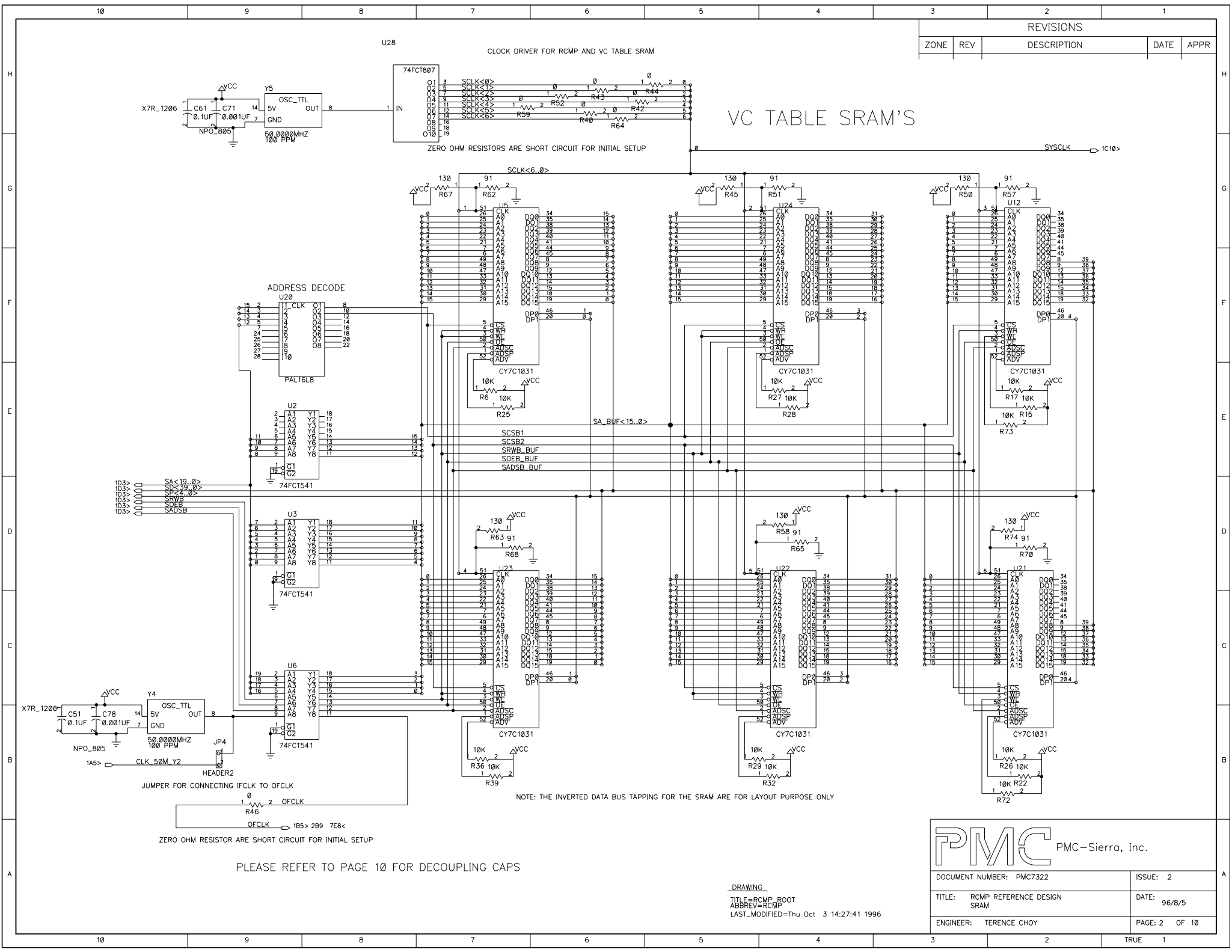


DOCUMENT NUMBER: PMC7322	ISSUE: 2
TITLE: RCMP REFERENCE DESIGN RCMP AND PHY INTERFACE LOGIC	DATE: 96/8/5
ENGINEER: TERENCE CHOY	PAGE: 1 OF 10

CLOCK DRIVER FOR INPUT PHY INTERFACE

PLEASE REFER TO PAGE 10 FOR DECOUPLING CAPS

DRAWING
TITLE=RCMP ROOT
ABBREV=RCMP
LAST_MODIFIED=Thu Oct 3 14:27:31 1996



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DOCUMENT NUMBER: PMC7322	ISSUE: 2
TITLE: RCMP REFERENCE DESIGN SRAM	DATE: 96/8/5
ENGINEER: TERENCE CHOY	PAGE: 2 OF 10

DRAWING
TITLE=RCMP ROOT
ABBREV=RCMP
LAST_MODIFIED=Thu Oct 3 14:27:41 1996

PLEASE REFER TO PAGE 10 FOR DECOUPLING CAPS

NOTE: THE INVERTED DATA BUS TAPPING FOR THE SRAM ARE FOR LAYOUT PURPOSE ONLY

ZERO OHM RESISTOR ARE SHORT CIRCUIT FOR INITIAL SETUP

CLOCK DRIVER FOR RCMP AND VC TABLE SRAM

ZERO OHM RESISTORS ARE SHORT CIRCUIT FOR INITIAL SETUP

VC TABLE SRAM'S

SYSCLK 1C10>

SA_BUF<15..0>

JUMPER FOR CONNECTING IFCLK TO OFCLK

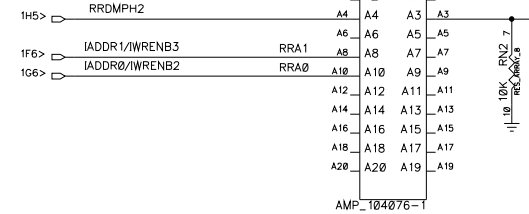
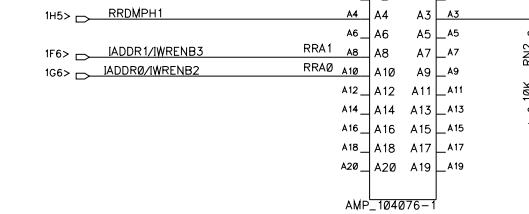
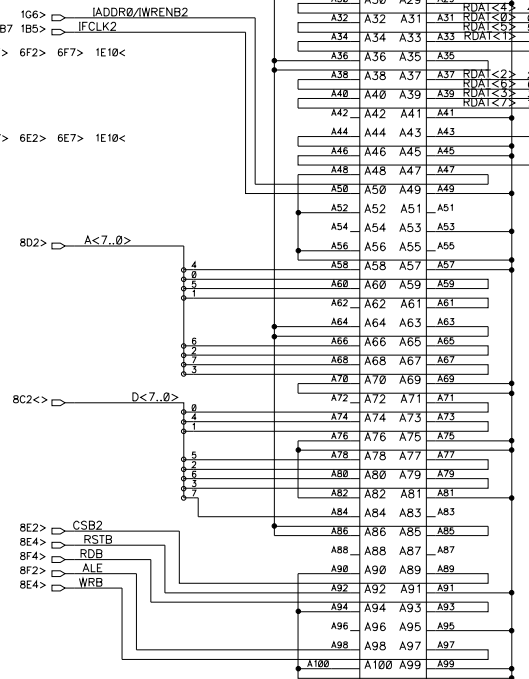
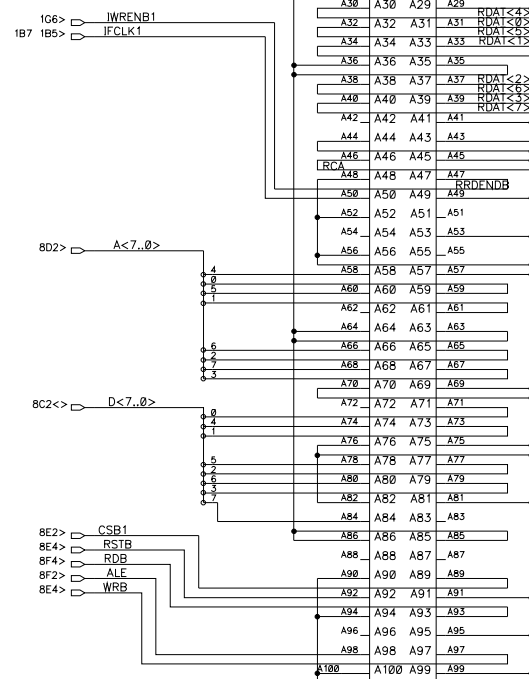
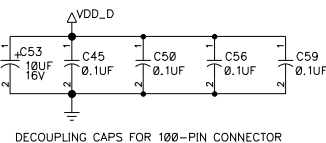
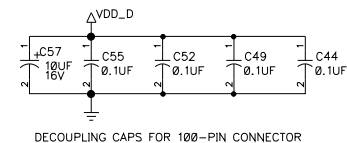
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CONNECTOR #1 (622/155/MPH)

CONNECTOR #2 (622/155/MPH)

REVISIONS

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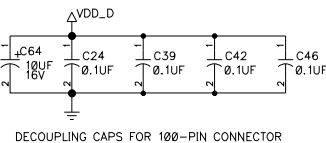
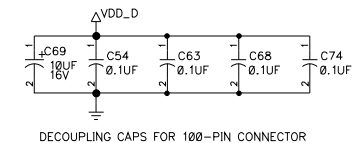
DOCUMENT NUMBER: PMC7322	ISSUE: 2
TITLE: RCMP REFERENCE DESIGN INPUT SCI-PHY CONNECTORS 1,2	DATE: 96/8/5
ENGINEER: TERENCE CHOY	PAGE: 3 OF 10

CONNECTOR #3 (622/155/MPH)

CONNECTOR #4 (622/155/MPH)

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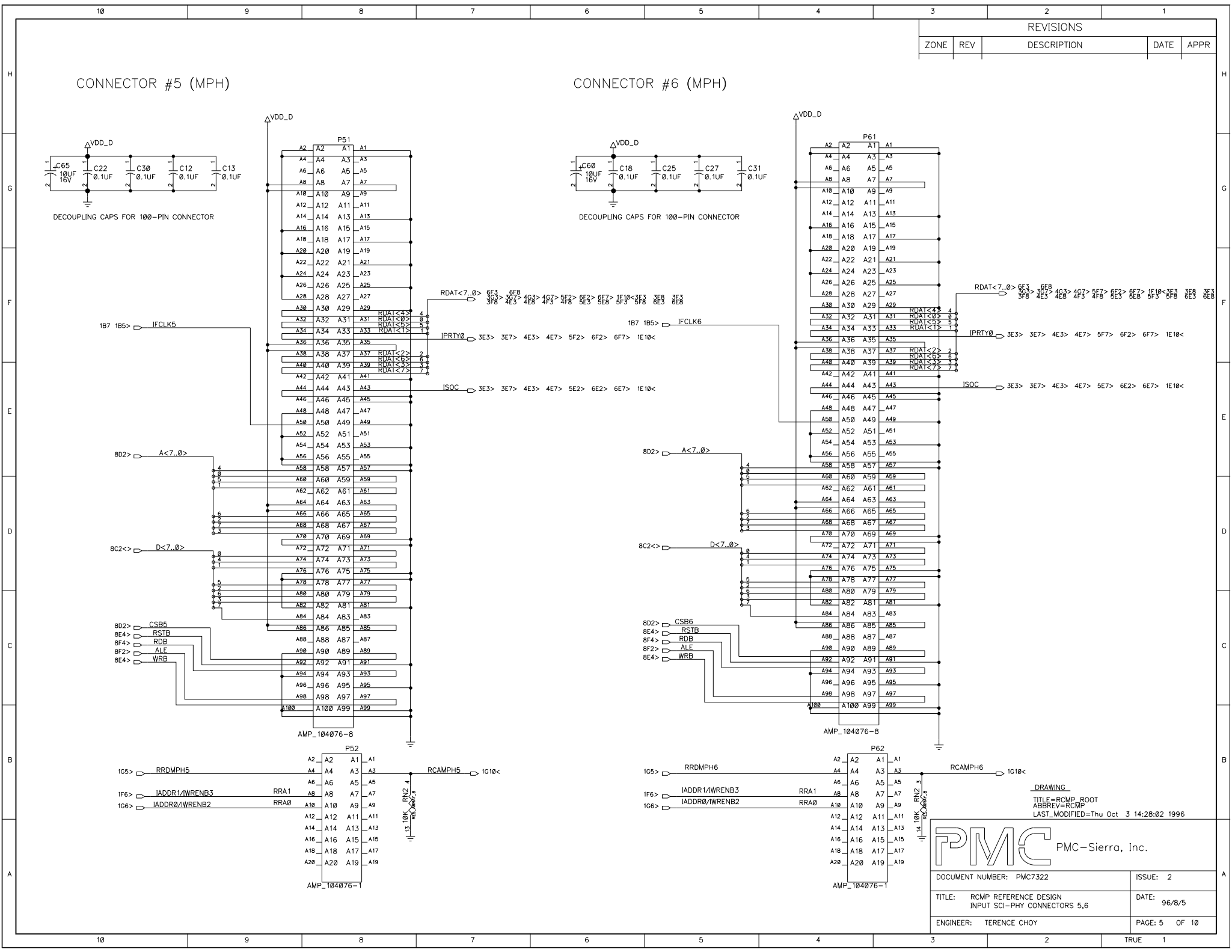


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ENGINEER: TERENCE CHOY	PAGE: 4 OF 10

TRUE 1

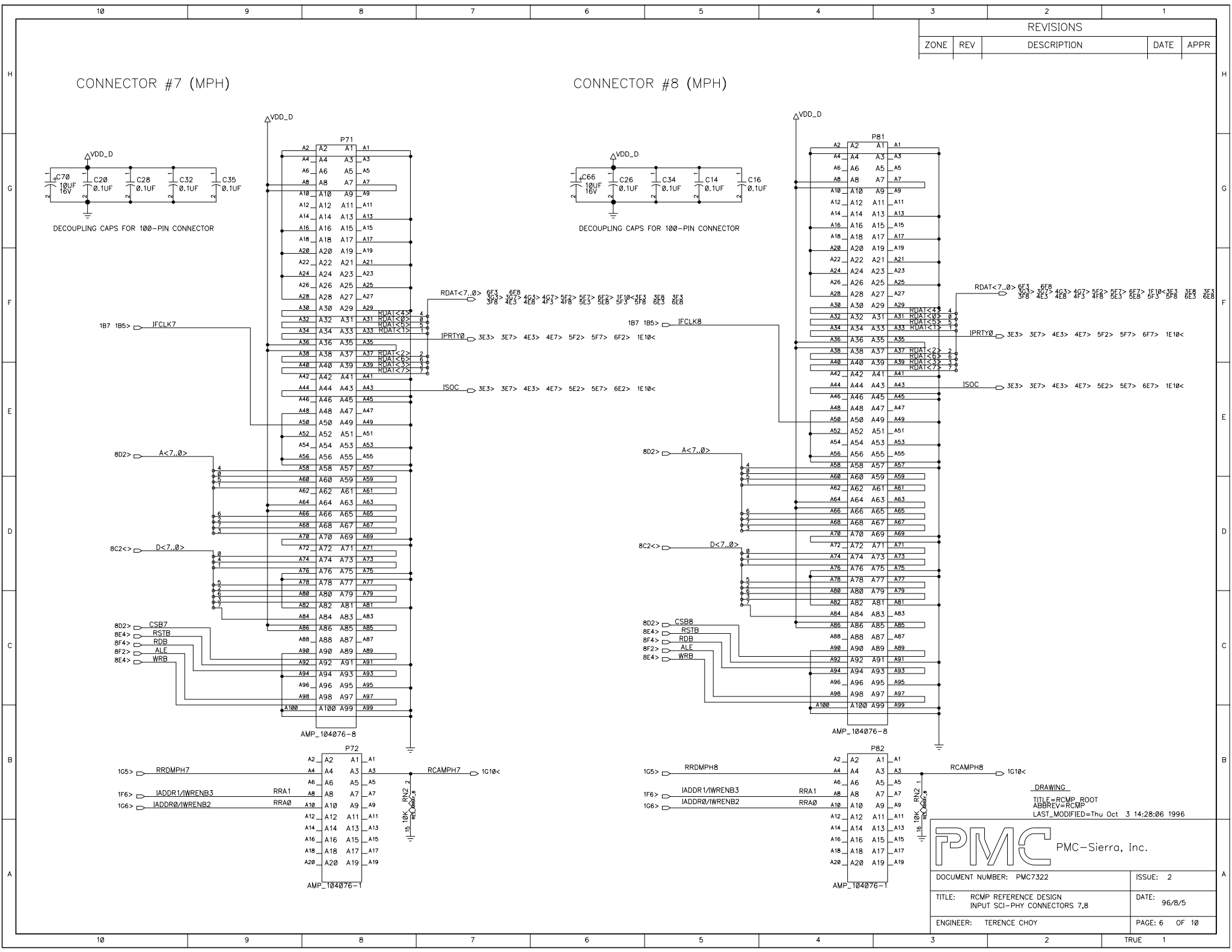


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ENGINEER: TERENCE CHOY	PAGE: 5 OF 10

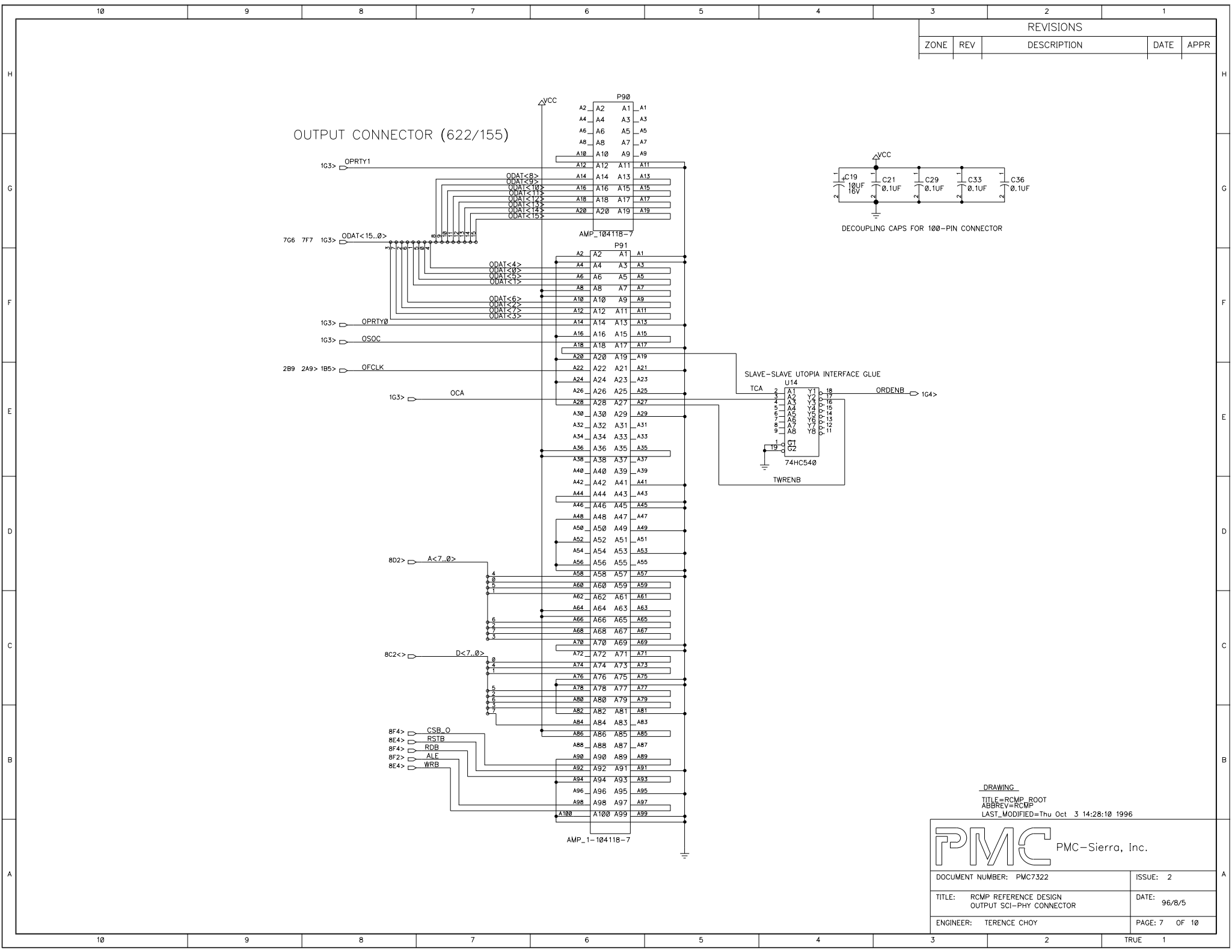


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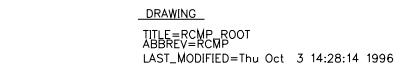
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ENGINEER: TERENCE CHOY	PAGE: 6 OF 10



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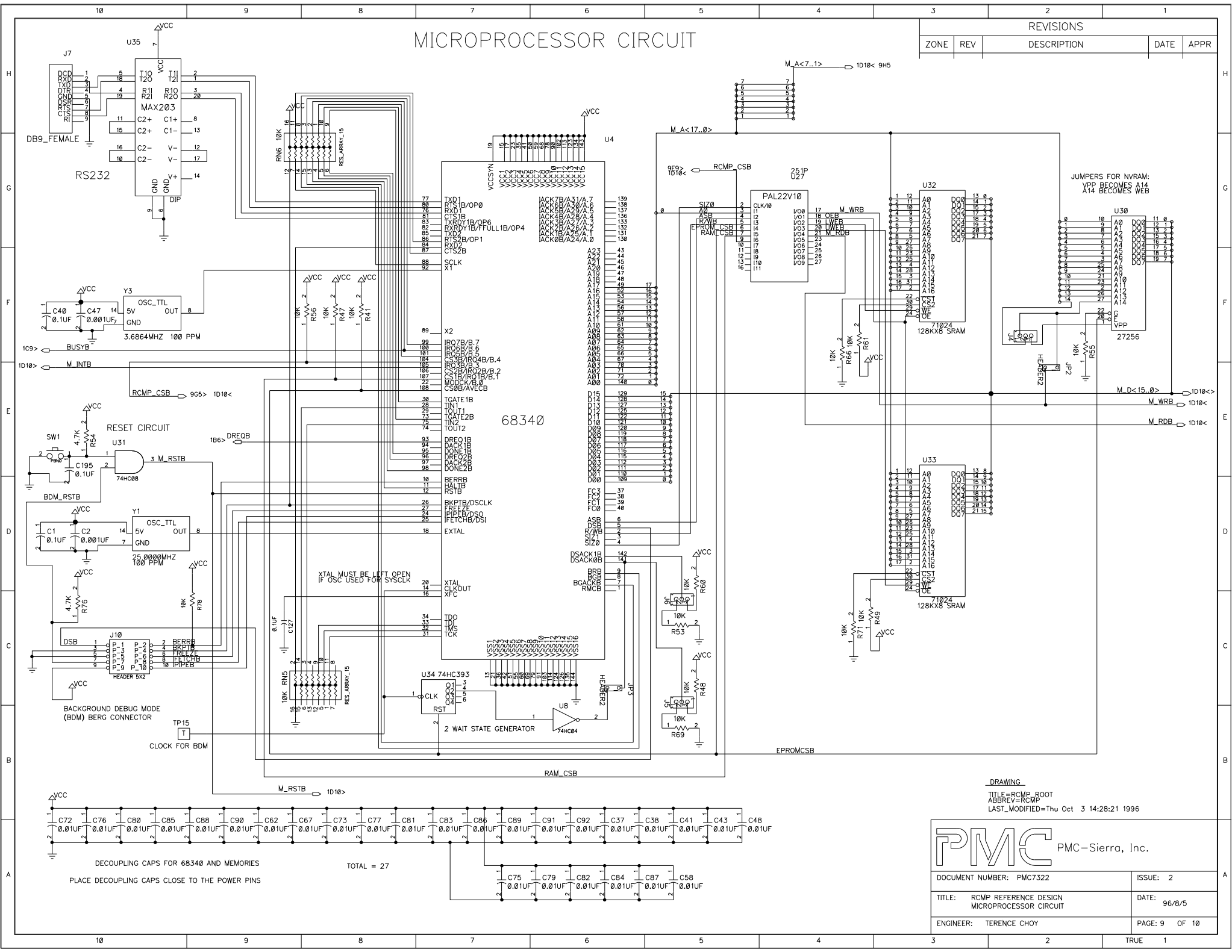
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ENGINEER: TERENCE CHOY		PAGE: 7 OF 10

6811 DECODE LOGIC

DOCUMENT NUMBER: PMC7322	ISSUE: 2
TITLE: RCMP REFERENCE DESIGN DECODE LOGIC FOR PHY DEVICES	DATE: 96/8/5
ENGINEER: TERENCE CHOY	PAGE: 8 OF 10

MICROPROCESSOR CIRCUIT

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



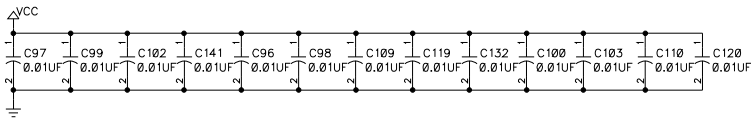
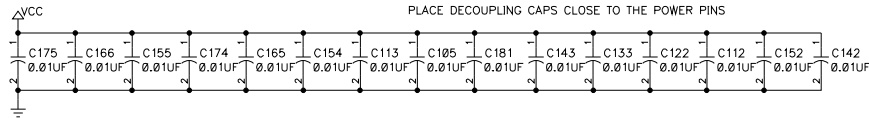
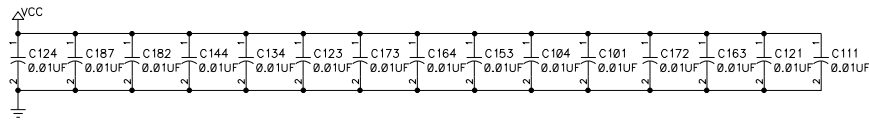
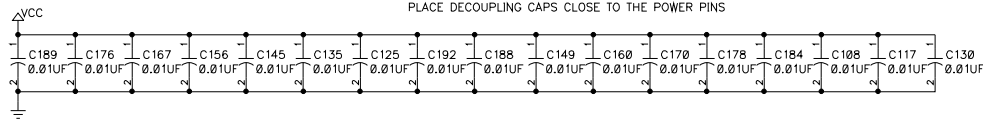
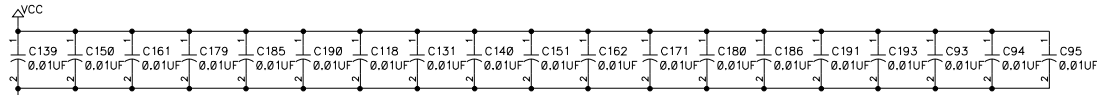
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ENGINEER: TERENCE CHOY	PAGE: 9 OF 10

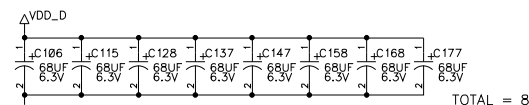
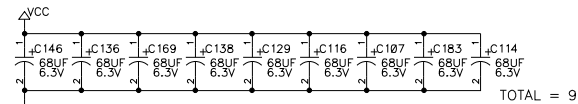
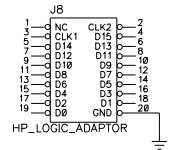
POWER SUPPLY AND DECOUPLING CAPS

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ZONE	REV	DESCRIPTION	DATE	APPR



HP LOGIC ADAPTOR

LOGIC ANALYZER CONNECTOR
FOR FUTURE USE



DRAWING
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ABBREV=RCMP
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PMC
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC7322	ISSUE: 2
TITLE: RCMP REFERENCE DESIGN DECOUPLING CAPS FOR RCMP AND SRAMS	DATE: 96/8/5
ENGINEER: TERENCE CHOY	PAGE: 10 OF 10

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*** Unit Cross-Reference *** --- for the entire design ---														REVISIONS																																																			
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C1 CAP 9D10 C2 CAP 9D10 C3 CAP 8B7 C4 CAP 8B7 C5 CAP 8B7 C6 CAP 8B6 C7 CAP 8B6 C8 CAP 1B10 C9 CAP 1B9 C10 CAP 8B5 C11 CAP 8B5 C12 CAP 5G10 C13 CAP 5G9 C14 CAP 5G5 C15 CAP 8B10 C16 CAP 6G5 C17 CAP 8C10 C18 CAP 5G6 C19 CAPACITOR POL 7G4 C20 CAP 6G10 C21 CAP 7G3 C22 CAP 5G10 C23 CAPACITOR POL 8C10 C24 CAP 4G6 C25 CAP 5G5 C26 CAP 6G6 C27 CAP 5G5 C28 CAP 6G10 C29 CAP 7G3 C30 CAP 5G10 C31 CAP 5G5 C32 CAP 6G10 C33 CAP 7G3 C34 CAP 6G5 C35 CAP 6G9 C36 CAP 7G2 C37 CAP 9A6 C38 CAP 9A5 C39 CAP 4G6 C40 CAP 9F10 C41 CAP 9A5 C42 CAP 4G5 C43 CAP 9A5 C44 CAP 3G9 C45 CAP 3G6 C46 CAP 4G5 C47 CAP 9F10 C48 CAP 9A5 C49 CAP 3G10 C50 CAP 3G6 C51 CAP 2B10 C52 CAP 3G10 C53 CAPACITOR POL 3G7 C54 CAP 4G10 C55 CAP 3G10 C56 CAP 3G5 C57 CAPACITOR POL 3G10 C58 CAP 9A5 C59 CAP 3G5 C60 CAPACITOR POL 5G6 C61 CAP 2H9 C62 CAP 9A9 C63 CAP 4G10 C64 CAPACITOR POL 4G7 C65 CAPACITOR POL 5G10 C66 CAPACITOR POL 6G6 C67 CAP 9A9 C68 CAP 4G10 C69 CAPACITOR POL 4G10 C70 CAPACITOR POL 6G10 C71 CAP 2H9 C72 CAP 9A10 C73 CAP 9A8 C74 CAP 4G9 C75 CAP 9A7 C76 CAP 9A10 C77 CAP 9A8 C78 CAP 2B10 C79 CAP 9A6 C80 CAP 9A10 C81 CAP 9A8 C82 CAP 9A6 C83 CAP 9A7 C84 CAP 9A6 C85 CAP 9A10 C86 CAP 9A7 C87 CAP 9A5 C88 CAP 9A9 C89 CAP 9A7 C90 CAP 9A9 C91 CAP 9A6 C92 CAP 9A6 C93 CAP 10G5 C94 CAP 10G5 C95 CAP 10G5 C96 CAP 10D9 C97 CAP 10D10 C98 CAP 10D9 C99 CAP 10D10 C100 CAP 10D7 C101 CAP 10F7 C102 CAP 10D9 C103 CAP 10D7 C104 CAP 10F7 C105 CAP 10E8												C106 CAPACITOR POL 10B5 C107 CAPACITOR POL 10C4 C108 CAP 10G6 C109 CAP 10D8 C110 CAP 10D7 C111 CAP 10F6 C112 CAP 10E6 C113 CAP 10E8 C114 CAPACITOR POL 10C3 C115 CAPACITOR POL 10B5 C116 CAPACITOR POL 10C4 C117 CAP 10G6 C118 CAP 10G8 C119 CAP 10D8 C120 CAP 10D6 C121 CAP 10F6 C122 CAP 10E7 C123 CAP 10F9 C124 CAP 10F10 C125 CAP 10G8 C127 CAPACITOR 9C9 C128 CAPACITOR POL 10B5 C129 CAPACITOR POL 10C4 C130 CAP 10C5 C131 CAP 10G8 C132 CAP 10D8 C133 CAP 10E7 C134 CAP 10F9 C135 CAP 10G9 C136 CAPACITOR POL 10C5 C137 CAPACITOR POL 10B5 C138 CAPACITOR POL 10C5 C139 CAP 10G10 C140 CAP 10G8 C141 CAP 10D9 C142 CAP 10E6 C143 CAP 10E7 C144 CAP 10F9 C145 CAP 10G9 C146 CAPACITOR POL 10C5 C147 CAPACITOR POL 10B4 C149 CAP 10G7 C150 CAP 10G10 C151 CAP 10G7 C152 CAP 10E6 C153 CAP 10F8 C154 CAP 10E9 C155 CAP 10E9 C156 CAP 10G9 C157 CAPACITOR POL 10B7 C158 CAPACITOR POL 10B4 C160 CAP 10G7 C161 CAP 10G9 C162 CAP 10G7 C163 CAP 10F6 C164 CAP 10F8 C165 CAP 10E9 C166 CAP 10E10 C167 CAP 10G9 C168 CAPACITOR POL 10B4 C169 CAPACITOR POL 10C5 C170 CAP 10G7 C171 CAP 10G7 C172 CAP 10F7 C173 CAP 10F8 C174 CAP 10E9 C175 CAP 10E10 C176 CAP 10G10 C177 CAPACITOR POL 10B3 C178 CAP 10G6 C179 CAP 10G9 C180 CAP 10G6 C181 CAP 10E8 C182 CAP 10F9 C183 CAPACITOR POL 10C3 C184 CAP 10G6 C185 CAP 10G9 C186 CAP 10G6 C187 CAP 10F10 C188 CAP 10G8 C189 CAP 10G10 C190 CAP 10G9 C191 CAP 10G6 C192 CAP 10G8 C193 CAP 10G6 C194 CAPACITOR POL 10A9 C195 CAP 9E10 D1 DIODEZENER 10B9 D2 DIODEZENER 10B7 F1 FUSE3A1 10B8 F2 FUSE3A1 10B9 J1 HEADER_3 1F8 J2 HEADER_3 1E4 J3 HEADER_3 1F9 J4 HEADER_3 9F2 J5 HEADER_3 9C5 J6 HEADER_3 9C5 J7 DB9 9H10 J8 HP_LOGIC_ADAPTOR 10E2 J9 PWRBLOCK 10C8 J10 HEADERSX2 9C10 JP1 HEADER2 1G7 JP2 HEADER2 9E2 JP3 HEADER2 9C6 JP4 HEADER2 2B9 P1 DIN96 8E9 P10 CONN20_MALE 3H8 P11 CONN100_MALE 3G8												P12 CONN20_MALE 3B8 P20 CONN20_MALE 3H4 P21 CONN100_MALE 3G4 P22 CONN20_MALE 3B4 P30 CONN20_MALE 4H8 P31 CONN100_MALE 4G8 P32 CONN20_MALE 4B8 P40 CONN20_MALE 4H4 P41 CONN20_MALE 4G4 P42 CONN20_MALE 4B4 P51 CONN100_MALE 5G8 P52 CONN20_MALE 5B8 P61 CONN100_MALE 5G3 P62 CONN20_MALE 5B3 P71 CONN100_MALE 6G8 P72 CONN20_MALE 6G8 P81 CONN100_MALE 6G3 P82 CONN20_MALE 6B3 P90 CONN20_MALE 7H6 P91 CONN100_MALE 7G6 R1 RESISTOR 1F8 R2 RESISTOR 1D4 R3 RESISTOR 1F7 R4 RESISTOR 1F7 R5 RESISTOR 1B6 R6 RESISTOR 2E7 R7 RESISTOR 1E8 R8 RESISTOR 1B7 R9 RESISTOR 1C5 R10 RESISTOR 1B7 R11 RESISTOR 1E4 R12 RESISTOR 1D4 R13 RESISTOR 1B6 R14 RESISTOR 1B7 R15 RESISTOR 2E2 R16 RESISTOR 1B6 R17 RESISTOR 2E2 R18 RESISTOR 1D3 R19 RESISTOR 1B7 R20 RESISTOR 1C8 R21 RESISTOR 1B7 R22 RESISTOR 2B2 R23 RESISTOR 1C8 R24 RESISTOR 1B6 R25 RESISTOR 2E7 R26 RESISTOR 2B2 R27 RESISTOR 2E4 R28 RESISTOR 2E4 R29 RESISTOR 2B5 R30 RESISTOR 1F9 R31 RESISTOR 1C7 R32 RESISTOR 2B4 R33 RESISTOR 1C7 R34 RESISTOR 1H9 R35 RESISTOR 1G9 R36 RESISTOR 2B7 R37 RESISTOR 1H9 R38 RESISTOR 8F3 R39 RESISTOR 2B7 R40 RESISTOR 2H6 R41 RESISTOR 9F8 R42 RESISTOR 2H6 R43 RESISTOR 2H6 R44 RESISTOR 2H5 R45 RESISTOR 2G5 R46 RESISTOR 2B9 R47 RESISTOR 9F8 R48 RESISTOR 9C5 R49 RESISTOR 9C3 R50 RESISTOR 2G3 R51 RESISTOR 2C4 R52 RESISTOR 2H6 R53 RESISTOR 9C5 R54 RESISTOR 9E10 R55 RESISTOR 9F2 R56 RESISTOR 9F8 R57 RESISTOR 2G2 R58 RESISTOR 2D4 R59 RESISTOR 2H7 R60 RESISTOR 9C5 R61 RESISTOR 9F4 R62 RESISTOR 2G7 R63 RESISTOR 2D7 R64 RESISTOR 2H6 R65 RESISTOR 2D4 R66 RESISTOR 9E4 R67 RESISTOR 2G7 R68 RESISTOR 2D7 R69 RESISTOR 9B5 R70 RESISTOR 2D2 R71 RESISTOR 9C4 R72 RESISTOR 2B2 R73 RESISTOR 2E2 R74 RESISTOR 2D2 R75 RESISTOR 8C6 R76 RESISTOR 9C10 R77 RESISTOR 1D10 R78 RESISTOR 9C9 R79 RESISTOR 1D10 RN1 RES_ARRAY_15 8C6 RN2 RES_ARRAY_8 3A3 3A8 4A4 4A8 5B3 5B8 6B3 6B8 RN3 RES_ARRAY_15 8G8 RN4 RES_ARRAY_8 3E3 3E7 4E3 4E7 RN5 RES_ARRAY_15 9C9 RN6 RES_ARRAY_15 9G9 SW1 PBNO TP1 TST_PT 1C7 TP2 TST_PT 1D7												TP3 TST_PT 10A3 TP4 TST_PT 10A4 TP5 TST_PT 10A5 TP6 TST_PT 10A4 TP7 TST_PT 10A4 TP8 TST_PT 10A4 TP9 TST_PT 10A5 TP10 TST_PT 10A5 TP11 TST_PT 10A6 TP12 TST_PT 10A5 TP13 TST_PT 10A6 TP14 TST_PT 10A6 TP15 TST_PT 9B9 U1 RCMP 1D6 U2 74FCT541 2E9 U3 74FCT541 2D9 U4 MC68340 9G6 U5 CY7C1031 2G7 U6 74FCT541 2C9 U7 74FCT807 1B8 U8 74HC84 9B6 U9 74XXX245 8D5 U10 74XXX573 8D4 U11 74XXX138 8E4 U12 CY7C1031 2G2 U13 74XXX04 8F5 8G6 U14 74XXX540 7E4 U15 74HC88 8E8 8H4 U16 74XXX541 8E6 U17 74XXX00 8G5 U18 74XXX30 8G5 U19 PAL22V10 1H8 U20 PAL16L8_ 2F9 U21 CY7C1031 2D2 U22 CY7C1031 2D4 U23 CY7C1031 2D7 U24 CY7C1031 2C4 U25 PAL22V10 1H6 U27 PAL22V10 9G4 U28 74FCT807 2H8 U30 27256_ 9G1 U31 74XXX08 9E10 U32 71024 9G3 U33 71024 9E3 U34 74XXX393 9C7 U35 MAX203 9H10 Y1 OSC_TTL 9D10 Y2 OSC_TTL 1B9 Y3 OSC_TTL 9F10 Y4 OSC_TTL 2C10 Y5 OSC_TTL 2H9																													

NOTES

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